

**a-Si TFT LCD Single-Chip Driver
480(RGB) x 864 Resolution
16.7M-color with Internal GRAM**

Specification
Preliminary

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Table of Contents

SECTION	PAGE
1. Introduction.....	19
2. Features	20
3. Device Overview	22
3.1. Block Diagram	22
3.2. Block Function Description.....	23
3.2.1. System Interface.....	23
3.2.2. Parallel RGB Interface.....	23
3.2.3. Address Counter (AC)	24
3.2.4. Graphic RAM (GRAM).....	24
3.2.5. Grayscale Voltage Generating Circuit	24
3.2.6. Timing Generating	24
3.2.7. Oscillator.....	24
3.2.8. Source Driver Circuit	25
3.2.9. Panel Control Circuit.....	25
3.2.10. Power Supply Circuit	25
3.2.11. MIPI DSI Controller Circuit	25
3.2.12. MDDI.....	25
3.2.13. CABC (Content Adaptive Brightness Control)	25
3.3. Pin Descriptions	26
3.4. Pin Assignment.....	33
3.5. Bump Arrangement	36
3.6. Pad Coordination.....	37
System Interface	46
3.7. DBI Type B Parallel Interface	46
3.7.1. Write Cycle Sequence	47
3.7.2. Read Cycle Sequence.....	48
3.7.3. DBI Type B Interface Set Table	49
3.8. DBI Type C Serial Interface.....	52
3.8.1. Write Cycle Sequence	52
3.8.2. Read Cycle Sequence.....	54
3.9. Data Transfer Break and Recovery.....	55
3.10. Data Transfer Pause	57
3.10.1. Serial Interface Pause	58
3.10.2. Parallel Interface Pause	59
3.10.3. Data Transfer Mode.....	60

3.10.4. Method 1	60
3.10.5. Method 2	60
3.11. DPI (RGB) Interface	61
3.11.1. DPI Interface Selection	61
3.11.2. DPI Interface Timing	63
3.12. DSI System Interface	64
3.12.1. General Description	64
3.12.2. Interface Level Communication	64
3.12.3. General	64
3.12.4. DSI-CLK Lanes	65
3.12.5. Low Power Mode (LPM)	66
3.12.6. Ultra Low Power Mode (ULPM)	68
3.12.7. High-Speed Clock Mode (HSCM)	69
3.12.8. DSI-D1 and DSI-D0 Data Lanes	71
3.12.9. General	71
3.12.10. Escape Modes	71
3.12.11. Low-Power Data Transmission (LPDT)	73
3.12.12. Ultra-Low Power State (ULPS)	74
3.12.13. Remote Application Reset (RAR)	75
3.12.14. Tearing Effect (TEE)	76
3.12.15. Acknowledge (ACK)	77
3.12.16. High-Speed Data Transmission (HSDT)	78
3.12.17. Entering High-Speed Data Transmission (TSOT of HSDT)	78
3.12.18. Leaving High-Speed Data Transmission (TEOT of HSDT)	79
3.12.19. Burst of the High-Speed Data Transmission (HSDT)	80
3.12.20. Bus Turnaround (BTA)	83
3.12.21. Packet Level Communication	84
3.12.22. Short Packet (SPa) and Long Packet (LPa) Structures	84
3.12.23. Bit Transmission Order of Bytes in Packets	85
3.12.24. Byte Transmission Order of Multiple-Byte Information in Packets	85
3.12.25. Packet Header (PH)	86
3.12.26. Data Identification (DI)	87
3.12.27. Virtual Channel (VC)	88
3.12.28. Data Type (DT)	89
3.12.29. Packet Data (PD) of a Short Packet (SPa)	91
3.12.30. Word Count (WC) of a Long Packet (LPa)	92
3.12.31. Error Correction Code (ECC)	93
3.12.32. Packet Data (PD) of a Long Packet (LPa)	97

3.12.33.	Packet Footer (PF) of a Long Packet (LPa).....	98
3.12.34.	Packet Transmissions	100
3.12.35.	Packet from the MPU to the Display Module	100
3.12.36.	Display Command Set (DCS)	100
3.12.37.	Display Command Set (DCS) Write, No Parameter (DCSWN-S)	101
3.12.38.	Display Command Set (DCS) Write, 1 Parameter (DCSW1-S).....	102
3.12.39.	Display Command Set (DCS) Write Long (DCSW-L)	103
3.12.40.	Display Command Set (DCS) Read, No Parameter (DCSRN-S)	107
3.12.41.	Null Packet, No Data (NP-L)	109
3.12.42.	End of Transmission Packet (EoTP)	111
3.12.43.	Packet from the Display Module to the MPU	113
3.12.44.	Used Packet Types	113
3.12.45.	Acknowledge with Error Report (AwER)	115
3.12.46.	DCS Read Long Response (DCSRR-L)	118
3.12.47.	DCS Read Short Response, 1 Byte Returned (DCSRR1-S).....	120
3.12.48.	DCS Read Short Response, 2 Bytes Returned (DCSRR2-S)	121
3.12.49.	Communication Sequences	122
3.12.50.	General	122
3.12.51.	Sequences	123
3.12.52.	DCS Write, 1 Parameter Sequence	123
3.12.53.	DCS Write, No Parameter Sequence	124
3.12.54.	DCS Write Long Sequence	125
3.12.55.	DCS Read, No Parameter Sequence	127
3.12.56.	Null Packet, No Data Sequence	129
3.12.57.	End of Transmission Packet	129
3.12.58.	16 Bit/Pixel Writing	130
3.12.59.	24 Bit/Pixel Writing	131
3.12.60.	24 bit/pixel Reading	133
3.13.	MDDI (Mobile Display Digital Interface)	137
3.14.	Display Data Format.....	147
3.14.1.	3-line Serial Interface.....	147
3.14.2.	SPI Data for 3-bit/pixel (RGB 1-1-1 bits input), 8-color	147
3.14.3.	SPI Data for 16-bit/pixel (RGB 5-6-5 bits input), 65K-color	148
3.14.4.	SPI Data for 18-bit/pixel (RGB 6-6-6 bits input), 262K-color	148
3.14.5.	SPI Data for 24-bit/pixel (RGB 8-8-8 bits input), 16.7M-color	149
3.14.6.	8-bit Parallel MPU Interface.....	150
3.14.7.	8-bit Data Bus for 16-bit/pixel (RGB 5-6-5 bits input), 65K-color.....	151
3.14.8.	8-bit Data Bus for 18-bit/pixel (RGB 6-6-6 bits input), 262K-color	152

3.14.9.	8-bit Data Bus for 24-bit/pixel (RGB 8-8-8 bits input), 16.7M-color	153
3.14.10.	9-bit Parallel MPU Interface	154
3.14.11.	9-bit Data Bus for 16-bit/pixel (RGB 5-6-5 bits input), 65K-color	155
3.14.12.	9-bit Data Bus for 18-bit/pixel (RGB 6-6-6 bits input), 262K-color	156
3.14.13.	9-bit Data Bus for 24-bit/pixel (RGB 8-8-8 bits input), 16.7M-color	157
3.14.14.	16-bit Parallel MPU Interface	158
3.14.15.	16-bit Data Bus for 16-bit/pixel (RGB 5-6-5 bits input), 65K-color	159
3.14.16.	16-bit Data Bus for 18-bit/pixel (RGB 6-6-6 bits input), 262K-color	160
3.14.17.	16-bit Data Bus for 24-bit/pixel (RGB 8-8-8 bits input), 16.7M-color	161
3.14.18.	18-bit Parallel MPU Interface	162
3.14.19.	18-bit Data Bus for 16-bit/pixel (RGB 5-6-5 bits input), 65K-color	163
3.14.20.	18-bit Data Bus for 18-bit/pixel (RGB 6-6-6 bits input), 262K-color	164
3.14.21.	18-bit Data Bus for 24-bit/pixel (RGB 8-8-8 bits input), 16.7M-color	165
3.14.22.	24-bit Parallel MPU Interface	166
3.14.23.	24-bit Data Bus for 24-bit/pixel (RGB 8-8-8 bits input), 16.7M-color	167
3.14.24.	DPI (RGB) Interface	168
3.14.25.	16-bit/pixel 65K colors order on the DPI Interface	168
3.14.26.	18-bit/pixel 262K Colors Order on the DPI Interface	169
3.14.27.	24-bit/pixel 16.7M colors order on the DPI Interface	170
3.14.28.	16/18-bit Color Data Mapping to 24-bit Pixel Data Operation.....	171
3.14.29.	DSI Transmission Data Format.....	173
3.14.30.	16-bit per Pixel, Long Packet, Data Type 00 1110 (0Eh)	173
3.14.31.	18-bit per Pixel, Long Packet, Data Type = 01 1110 (1Eh)	174
3.14.32.	18-bit per Pixel, Long Packet, Data Type = 10 1110 (2Eh)	175
3.14.33.	24-bit per Pixel, Long Packet, Data Type = 11 1110 (3Eh)	176
4.	Command.....	177
4.1.	Command List	177
4.1.1.	Standard Command List	177
4.1.2.	Extended Command List	184
4.2.	Command Description.....	190
4.2.1.	NOP (00h).....	190
4.2.2.	Software Reset (01h).....	191
4.2.3.	Read display identification information (04h)	192
4.2.4.	Read Number of the Errors on DSI (05h)	193
4.2.5.	Get Red Channel (06h)	194
4.2.6.	Get Green Channel (07h)	195
4.2.7.	Get Blue Channel (08h)	196
4.2.8.	Read Display Status (09h)	197

4.2.9. Read Display Power Mode (0Ah)	199
4.2.10. Read Display MADCTL (0Bh).....	201
4.2.11. Read Display Pixel Format (0Ch)	203
4.2.12. Read Display Image Mode (0Dh)	204
4.2.13. Read Display Signal Mode (0Eh)	206
4.2.14. Read Display Self-Diagnostic Result (0Fh)	208
4.2.15. Sleep In (10h)	209
4.2.16. Sleep Out (11h).....	210
4.2.17. Partial Mode On (12h)	211
4.2.18. Normal Display Mode On (13h)	212
4.2.19. Display Inversion Off (20h)	213
4.2.20. fDisplay Inversion On (21h)	214
4.2.21. All Pixel Off (22h).....	215
4.2.22. All Pixel On (23h).....	216
4.2.23. Gamma Set (26h)	217
4.2.24. Display Off (28h).....	218
4.2.25. Display ON (29h)	219
4.2.26. Column Address Set (2Ah).....	220
4.2.27. Page Address Set (2Bh)	222
4.2.28. Memory Write (2Ch)	224
4.2.29. Memory Read (2Eh)	225
4.2.30. Partial Area (30h).....	226
4.2.31. Vertical Scrolling Definition (33h).....	228
4.2.32. Tearing Effect Line OFF (34h)	232
4.2.33. Tearing Effect Line ON (35h)	233
4.2.34. Memory Access Control (36h)	235
4.2.35. Vertical Scrolling Start Address (37h)	238
4.2.36. Idle Mode Off (38h).....	240
4.2.37. Idle Mode On (39h).....	241
4.2.38. Interface Pixel Format (3Ah).....	242
4.2.39. Memory Write Continue (3Ch)	243
4.2.40. Memory Read Continue (3Eh).....	244
4.2.41. Write Tear Scan Line (44h).....	245
4.2.42. Read Scan Line (45h).....	246
4.2.43. Write Display Brightness Value (51h)	247
4.2.44. Read Display Brightness Value (52h).....	248
4.2.45. Write CTRL Display Value (53h).....	249
4.2.46. Read CTRL Display Value (54h).....	251

4.2.47. Write Content Adaptive Brightness Control Value (55h).....	252
4.2.48. Read Content Adaptive Brightness Control Value (56h)	254
4.2.49. Write CABC Minimum Brightness (5Eh).....	256
4.2.50. Read CABC Minimum Brightness (5Fh).....	257
4.2.51. Read Automatic Brightness Control Self-diagnostic Result (68h)	258
4.2.52. Read Black/White Low Bits (70h)	259
4.2.53. Read Bkx (71h).....	260
4.2.54. Read Bky (72h).....	261
4.2.55. Read Wx (73h).....	262
4.2.56. Read Wy (74h).....	263
4.2.57. Read Red/Green Low Bits (75h)	264
4.2.58. Read Rx (76h)	265
4.2.59. Read Ry (77h)	266
4.2.60. Read Gx (78h)	267
4.2.61. Read Gy (79h)	268
4.2.62. Read Blue/A Color Low Bits (7Ah).....	269
4.2.63. Read Bx (7Bh)	270
4.2.64. Read By (7Ch)	271
4.2.65. Read Ax (7Dh)	272
4.2.66. Read Ay (7Eh)	273
4.2.67. Read DDB Start (A1h)	274
4.2.68. Read DDB Continue (A8h)	276
4.2.69. Read First Checksum (AAh).....	277
4.2.70. Read Continue Checksum (AFh).....	278
4.2.71. Read Device Code (D3h)	279
4.2.72. Read ID1 (DAh)	280
4.2.73. Read ID2 (DBh)	281
4.2.74. Read ID3 (DCh)	282
4.3. Extend Command (EXTC) Description	283
4.3.1. Interface Mode Control (B0h)	283
4.3.2. Frame Rate Control 1 (In Normal Mode/Full Colors) (B1h).....	284
4.3.3. Frame Rate Control 2 (In Idle Mode/8 colors) (B2h)	286
4.3.4. Frame Rate control 3 (In Partial Mode/Full Colors) (B3h)	288
4.3.5. Display Inversion Control (B4h).....	290
4.3.6. Blanking Porch Control (B5h)	292
4.3.7. Display Function Control (B6h).....	293
4.3.8. Entry Mode Set (B7h)	294
4.3.9. DBI Type B Interface Setting (B8h)	295

4.3.10. Panel Control (B9h)	296
4.3.11. SPI Interface Setting (BAh)	298
4.3.12. Power Control 1 (C0h)	299
4.3.13. Power Control 2 (C1h)	301
4.3.14. Power Control 3 (C2h)	303
4.3.15. VCOM Control 1 (C7h)	305
4.3.16. Backlight Control 1 (C8h)	306
4.3.17. Backlight Control 2 (C9h)	307
4.3.18. Backlight Control 3 (CAh)	309
4.3.19. Backlight Control 4 (CBh)	310
4.3.20. Backlight Control 5 (CCh)	312
4.3.21. Backlight Control 6 (CDh)	313
4.3.22. Backlight Control 7(CEh)	314
4.3.23. Backlight Control 8 (CFh)	315
4.3.24. NV Memory Write (D0h)	316
4.3.25. NV Memory Protection Key (D1h)	317
4.3.26. NV Memory Status Read (D2h)	318
4.3.27. Engineering Setting (DFh)	320
4.3.28. Positive Gamma Control (E0h)	321
4.3.29. Negative Gamma Correction (E1h)	322
4.3.30. Digital Gamma Control 1 (E2h)	323
4.3.31. Digital Gamma Control 2 (E3h)	323
4.3.32. Digital 3 Gamma Enable (EAh)	324
4.3.33. VGMP / VGMPN / VGSP / VGSN Voltage Measurement Set (EDh)	325
4.3.34. Panel Timing Control 1 (F1h)	326
4.3.35. Panel Timing Control 2 (F2h)	327
4.3.36. DVDD Voltage Setting (F3h)	329
4.3.37. Power Control 5 (F5h)	330
4.3.38. Panel Resolution Selection Set (F7h)	331
4.3.39. Read EXTC Command In SPI Mode (FBh)	332
4.3.40. LVGL Voltage Setting (FCh)	333
4.3.41. External Power Selection Set (FDh)	334
4.3.42. EXTC Command Set enable register (FFh)	335
5. Source, Gate and Memory Map	336
5.1. Memory Map of the 480 (RGB) x 864 Resolution	336
5.2. Memory Map of the 480 (RGB) x 854 Resolution	337
5.3. Memory Map of the 480 (RGB) x 800 Resolution	338
5.4. Memory Map of the 480 (RGB) x 640 Resolution	339

6. Source Driver	340
7. Display Data RAM	341
7.1. Configuration	341
7.2. Memory to Display Address Mapping	342
7.2.1. Fully Display	342
7.2.2. Vertical Scrolling Display	344
7.2.3. Vertical Scroll 480(RGB) (H) X 864 (V) Example	344
7.2.4. Case1: TFA+VSA+BFA \neq 864	344
7.2.5. Case2: TFA+VSA+BFA = 864 (Rolling Scrolling)	344
7.3. MPU to Memory Write/Read Direction	347
8. Tearing Effect Information	350
8.1. Tearing Effect Line	351
8.1.1. Tearing Effect Line Modes	351
8.1.2. Tearing Effect Line Timing	352
8.2. Tearing Effect Bus Trigger	353
8.2.1. Tearing Effect Bus Trigger Enable	353
8.2.2. Tearing Effect Bus Trigger Disable	354
8.2.3. Tearing Effect Bus Trigger Sequences	355
9. Content Adaptive Brightness Control (CABC) Function	363
10. Color Enhancement Function	364
11. Sleep Out Command and Self-Diagnostic Functions	365
11.1. Register Loading Detection	365
11.2. Functionality Detection	366
12. Power ON/OFF Sequence	367
12.1. Case 1 – RESX Line is Held High or Unstable by Host at Power ON	368
12.2. Case 2 – RESX Line is Held Low by Host at Power ON	369
12.3. Abnormal Power Off	370
13. Power Level Definition	371
13.1. Power Levels	371
13.2. Power Flow Chart	372
13.3. LCM Voltage Generation	373
13.4. Gamma Curves	374
13.4.1. Gamma Curve 1 (GC0), applies the function $y = x^{2.2}$	374
13.4.2. Gamma Curve 2 (GC1), applies the function $y = x^{1.8}$	374
13.4.3. Gamma Curve 3 (GC2), applies the function $y = x^{2.5}$	374
13.4.4. Gamma Curve 4 (GC3), applies the function $y = x^{1.0}$	375
14. Reset	376
14.1. Registers	376

14.2. Driver IC Input and Output pins.....	377
14.2.1. Output Pins, I/O Pins	377
14.2.2. Reset Timing.....	378
15. NV Memory Programming.....	379
15.1. NV Memory Programming Flow	379
16. 3 Gamma Setting Flow.....	380
16.1. 3 Gamma Setting Flow.....	380
17. Gamma Correction	381
18. Deep Standby Mode Setting	399
19. Electrical Characteristics	400
19.1. Absolute Maximum Ratings	400
19.2. DC Characteristics for Panel Driving.....	401
19.3. DSI DC Characteristics	402
19.3.1. DC characteristics for Power Lines	402
19.3.2. DC Characteristics for DSI LP Mode	403
19.3.3. Spike/Glitch Rejection.....	403
19.3.4. DC Characteristics for DSI HS Mode	404
19.3.5. DC Characteristics for MDDI	407
AC Characteristics	408
19.3.6. Display Parallel 24/18/16/9/8-bit Interface Timing Characteristics (8080-series).....	408
19.3.7. Display Serial Interface Timing Characteristics (3-line SPI system)	410
19.3.8. Parallel 24/18/16-bit RGB Interface Timing Characteristics	411
19.3.9. DSI Timing Characteristics	412
19.3.10. High Speed Mode – Clock Channel Timing	412
19.3.11. High Speed Mode – Data Clock Channel Timing.....	412
19.3.12. High Speed Mode – Rising and Falling Timings	413
19.3.13. Low Speed Mode – Bus Turn Around	414
19.3.14. Data Lanes from Low Power Mode to High Speed Mode.....	415
19.3.15. Data Lanes from High Speed Mode to Low Power Mode.....	416
19.3.16. DSI Clock Burst – High Speed Mode to/from Low Power Mode.....	417
19.3.17. MDDI Timing Characteristics	418
20. Application Circuit.....	419
20.1. Reference Circuit.....	419
20.2. External Component	420
21. Revision History	421

List of Figures

Figure 1: Block Diagram	22
Figure 2: DBI Type B Write Cycle	47
Figure 3: DBI Type B Write Cycle Sequence	47
Figure 4: DBI Type B Read Cycle	48
Figure 5: DBI Type B Read Cycle Sequence	48
Figure 6: DBI Type B 24-bit Data Bus	49
Figure 7: DBI Type B 18-bit Data Bus	49
Figure 8: DBI Type B 16-bit Data Bus	50
Figure 9: DBI Type B 9-bit Data Bus	50
Figure 10: DBI Type B 8-bit Data Bus	51
Figure 11: DBI Type C Data Format	52
Figure 12: DBI Type C Protocol	53
Figure 13: DBI Type C Read Cycle Sequence	54
Figure 14: Data Transfer Break and Recovery	55
Figure 15: Data Transfer Break - Case 1	55
Figure 16: Data Transfer Break - Case 2	56
Figure 17: Data Transfer Pause	57
Figure 18: DBI Type C Data Transfer Pause	58
Figure 19: DBI Type B Data Transfer Pause	59
Figure 20: Data Transfer Mode - Method 1	60
Figure 21: Data Transfer Mode - Method 2	60
Figure 22: DPI Interface 16/18/24-bit Pixel Format Selection	61
Figure 23: General DPI Timing Diagram	62
Figure 24: DPI Interface Timing diagram	63
Figure 25: DSI System Interface Diagram	64
Figure 26: Power Modes of Clock Lanes	65
Figure 27: From ULPM to LPM	66
Figure 28: From High Speed Clock Mode (HSCM) to LPM	66
Figure 29: All the Changes of the Three Modes to the LPM	67
Figure 30: From LPM to ULPM	68
Figure 31: Mode Change from LPM to ULPM	68
Figure 32: From LPM to HSCM	69
Figure 33: Mode Change from LPM to HSCM	69
Figure 34: High Speed Clock Burst	70
Figure 35: General Escape Mode Sequence	72
Figure 36: Low-Power Data Transmission (LPDT)	73
Figure 37: Pause (Example)	73

Figure 38: Ultra-Low Power State (ULPS)	74
Figure 39: Remote Application Reset (RAR)	75
Figure 40: Tearing Effect (TEE)	76
Figure 41: Acknowledge (ACK).....	77
Figure 42: Entering High-Speed Data Transmission (TSOT of HSDT)	78
Figure 43: Leaving High-Speed Data Transmission (TEOT of HSDT)	79
Figure 44: Single Packet in High-Speed Data Transmissions	80
Figure 45: Multiple Packets in High-Speed Data Transmission – Examples.....	80
Figure 46: Single Packet in HSDT – Even Number of Bytes.....	81
Figure 47: Single Packet in HSDT – Odd Number of Bytes	81
Figure 48: Start of Transmission (SoT) in HSDT for Multiple Packets.....	81
Figure 49: Continuous Multiple Packets in HSDT when Number of Bytes is Equal on Both Data Lanes at the End of the Packet.....	81
Figure 50: Continuous Multiple Packets in HSDT when Number of Bytes is not Equal on Both Data Lanes at the End of the Packet	82
Figure 51: End of Transmission (EoT) in HSDT when Number of Bytes is Equal on Both Data Lanes at the End of the Packet.....	82
Figure 52: End of Transmission (EoT) in HSDT when Number of Bytes is not Equal on Both Data Lanes at the End of the Packet.....	82
Figure 53: Bus Turnaround Procedure	83
Figure 54: Short Packet (SPa) Structure	84
Figure 55: Long Packet (LPa) Structure	84
Figure 56: Bit Transmission Order of Bytes in Packets.....	85
Figure 57: Byte Transmission Order of the Multiple-Byte Information in Packets.....	85
Figure 58: Packet Header (PH) of a Short Packet (SPa)	86
Figure 59: Packet Header (PH) on Long Packet (LPa)	86
Figure 60: Data Identification (DI) Structure	87
Figure 61: Data Identification (DI) in the Packet Header (PH)	87
Figure 62: Virtual Channel (VC) on the Packet Header (PH)	88
Figure 63: Virtual Channel (VC) Configuration	88
Figure 64: Data Type (DT) in the Packet Header (PH).....	89
Figure 65: Packet Data (PD) of a Short Packet (SPa), 2 Bytes Information	91
Figure 66: Packet Data (PD) of a Short Packet (SPa), 1 Byte Information	91
Figure 67: Word Count (WC) of a Long Packet (LPa).....	92
Figure 68: Packet Data in Short and Long Packets.....	92
Figure 69: D [23...0] and P [7...0] of a Short Packet (SPa)	93
Figure 70: D [23...0] and P [7...0] of a Long Packet (LPa)	93
Figure 71: XOR Functionality in a Short Packet (SPa).....	94

Figure 72: XOR Functionality in a Long Packet (LPa).....	95
Figure 73: Internal Error Correction Code (IECC) on the Display Module (the Receiver).....	95
Figure 74: Internal XOR Calculation between ECC and IECC Values – No Error	96
Figure 75: Internal XOR Calculation between ECC and IECC Values - Error	96
Figure 76: 16-bit Cyclic Redundancy Check (CRC) Calculation	98
Figure 77: CRC Calculation – Packet Data (PD) is 01h	98
Figure 78: Packet Footer (PF) Example	99
Figure 79: Display Command Set (DCS) in Short Packet (SPa) and Long Packet (LPa).....	100
Figure 80: Display Command Set (DCS) Write, No Parameter (DCSWN-S) - Example.....	101
Figure 81: Display Command Set (DCS) Write, 1 Parameter (DCSW1-S) – Example	102
Figure 82: Display Command Set (DCS) Write Long (DCSW-L) with DCS Only - Example	104
Figure 83: Display Command Set (DCS) Write Long with DCS and 1 Parameter - Example.....	105
Figure 84: Display Command Set (DCS) Write Long with DCS and 4 Parameters - Example.....	106
Figure 85 Set Maximum Return Packet Size (SMRPS-S) - Example	108
Figure 86 Display Command Set (DCS) Read, No Parameter (DCSRN-S) - Example	109
Figure 87: Null Packet, No Data (NP-L) - Example	110
Figure 88: End of Transmission Packet (EoTP)	112
Figure 89: End of Transmission Packet (EoTP) - Examples	112
Figure 90: Return Bytes in a Single Packet.....	113
Figure 91: Return Bytes in Several Packets – Not Allowed	113
Figure 92: Exception when Return Bytes in Several Packets	114
Figure 93: Acknowledge with Error Report (AwER) – Example	116
Figure 94: Errors Packets	117
Figure 95: Flow Chart for Errors on DSI	117
Figure 96: DCS Read Long Response (DCSRR-L) - Example	119
Figure 97: DCS Read Short Response, 1 Byte Returned (DCSRR1-S) - Example	120
Figure 98: DCS Read Short Response, 2 Bytes Returned (DCSRR2-S) - Example	121
Figure 99: One Pixel Bit and Write Color Orders.....	130
Figure 100: One Pixel Write (DCSW-L) – Example 1	130
Figure 101: Red/Green [0:2] Subpixel Write (DCSW1-S) – Example 2	131
Figure 102: Green [3:5]/Blue Subpixel Write (DCSW1-S) – Example 3.....	131
Figure 103: One Pixel Bit and Color Write Orders.....	131
Figure 104: One Pixel Write (DCSW-L) – Example	132
Figure 105: Blue Subpixel Write (DCSW1-S) – Example 2.....	132
Figure 106: Green Subpixel Write (DCSW1-S) – Example 3	133
Figure 107: Red Subpixel Write (DCSW1-S) – Example 4	133
Figure 108: One Pixel Bit and Color Read Order	133
Figure 109: One Pixel Read Response (DCSRR-L) – Example 1	134

Figure 110: Red Subpixel Response (DCSRR1-S) – Example 2	134
Figure 111: Green Subpixel Response (DCSRR1-S) – Example 3	135
Figure 112: Blue Subpixel Response (DCSRR1-S) – Example 4	135
Figure 113: Red and Green Subpixels Response (DCSRR2-S) – Example 5	135
Figure 114: Green and Blue Subpixels Response (DCSRR2-S) – Example 6	136
Figure 115: Blue and Red Subpixels Response (DCSRR2-S) – Example 7	136
Figure 116: Forward Link Structure	139
Figure 117: Sub-Frame Header Packet.....	139
Figure 118: Example of Video Stream Packet Fields	140
Figure 119: Video Data Format	141
Figure 120: Register Access Packet	142
Figure 121: Example of Register Access Packet (write to the ILI9806G)	143
Figure 122: Link Shutdown Packet.....	144
Figure 123: Filler Packet.....	144
Figure 124: Hibernation Mode Sequence	145
Figure 125: Host Initiated Wake-up without Contention	146
Figure 126: 3-line Serial Interface	147
Figure 127: SPI Data for 3-bit/pixel (RGB 1-1-1 bits input), 8-color	147
Figure 128: SPI Data for 16-bit/pixel (RGB 5-6-5 bits input), 65K-color	148
Figure 129: SPI Data for 18-bit/pixel (RGB 6-6-6 bits input), 262K-color	148
Figure 130: SPI Data for 24-bit/pixel (RGB 8-8-8 bits input), 16.7M-color	149
Figure 131: 3-line SPI Mode Read Data.....	150
Figure 132: 8-bit Parallel MPU Interface	150
Figure 133: 8-bit Data Bus for 16-bit/pixel (RGB 5-6-5 bits input), 65K-color	151
Figure 134: 8-bit Data Bus for 18-bit/pixel (RGB 6-6-6 bits input), 262K-color	152
Figure 135: 8-bit Data Bus for 24-bit/pixel (RGB 8-8-8 bits input), 16.7M-color	153
Figure 136: 9-bit Parallel MPU Interface	154
Figure 137: 9-bit Data Bus for 16-bit/pixel (RGB 5-6-5 bits input), 65K-color	155
Figure 138: 9-bit Data Bus for 18-bit/pixel (RGB 6-6-6 bits input), 262K-color	156
Figure 139: 9-bit Data Bus for 24-bit/pixel (RGB 8-8-8 bits input), 16.7M-color	157
Figure 140: 16-bit Parallel MPU Interface	158
Figure 141: 16-bit Data Bus for 16-bit/pixel (RGB 5-6-5 bits input), 65K-color	159
Figure 142: 16-bit Data Bus for 18-bit/pixel (RGB 6-6-6 bits input), 262K-color	160
Figure 143: 16-bit Data Bus for 24-bit/pixel (RGB 8-8-8 bits input), 16.7M-color	161
Figure 144: 18-bit Parallel MPU Interface	162
Figure 145: 18-bit Data Bus for 16-bit/pixel (RGB 5-6-5 bits input), 65K-color	163
Figure 146: 18-bit Data Bus for 18-bit/pixel (RGB 6-6-6 bits input), 262K-color	164
Figure 147: 18-bit Data Bus for 24-bit/pixel (RGB 8-8-8 bits input), 16.7M-color	165

Figure 148: 24-bit Parallel MPU Interface	166
Figure 149: 24-bit Data Bus for 24-bit/pixel (RGB 8-8-8 bits input), 16.7M-color	167
Figure 150: 16-bit/pixel 65K Colors Order on the DPI Interface	168
Figure 151: 18-bit/pixel 262K colors order on the DPI Interface	169
Figure 152: 24-bit/pixel 16.7M Colors Order on the DPI Interface	170
Figure 153: EPF [1:0] = 10, 16-bit data mapping to 24-bit	172
Figure 154: EPF [1:0] = 10, 18-bit data mapping to 24-bit	172
Figure 155: 16-bit per Pixel, Data Type 00 1110 (0Eh)	173
Figure 156: 18-bit per Pixel, Data Type = 01 1110 (1Eh)	174
Figure 157: 18-bit per Pixel, Data Type = 10 1110 (2Eh)	175
Figure 158: 24-bit per Pixel, Data Type = 11 1110 (3Eh)	176
Figure 159: Memory Map of the 480 (RGB) x 864 Resolution, R36h MV bit D5 = 0	336
Figure 160: Memory Map of the 480 (RGB) x 854 Resolution, R36h MV bit D5 = 0	337
Figure 161: Memory Map of the 480 (RGB) x 800 resolution, R36h MV bit D5 = 0	338
Figure 162: Memory Map of the 480 (RGB) x 640 Resolution, R36h MV bit D5 = 0	339
Figure 163: Vertical Scroll Mode Function	344
Figure 164: MV, MX, MY setting (480 (RGB) x 864)	347
Figure 165: Tearing Effect Line Mode 1	351
Figure 166: Tearing Effect Line Mode 2	351
Figure 167: CABC Block Diagram	363
Figure 168: PWM OUT on/off period	363
Figure 169: Saturation Enhancement Image	364
Figure 170: Register Loading Detection	365
Figure 171: Functionality Detection	366
Figure 172: Case 1 – RESX Line is Held High or Unstable by Host at Power ON	368
Figure 173: Case 2 – RESX Line is Held Low by Host at Power ON	369
Figure 174: Power Mode Flow Chart	372
Figure 175: Power Stage Diagram	373
Figure 176: Gamma Curve 1 (GC0)	374
Figure 177: Gamma Curve 2 (GC1)	374
Figure 178: Gamma Curve 3 (GC2)	374
Figure 179: Gamma Curve 4 (GC3)	375
Figure 180: Reset Timing	378
Figure 181: Positive Noise Pulse during Reset Low	378
Figure 182: NV Memory Programming Flow	379
Figure 183: Positive Gamma Control (E0h)	381
Figure 184: Negative Gamma Control (E1h)	382
Figure 185: Deep Standby Mode Entry/Exit	399

Figure 186: Noise on Power Supply Lines	402
Figure 187: Spike/Glitch Rejection	403
Figure 188: Differential Inputs Logical 0 and 1, Threshold High/Low, Differential Voltage Range	405
Figure 189: Common Mode Voltage on Clock and Data Channels	405
Figure 190: Differential Pair Termination Resistor on the Receiver Side	406
Figure 191: DSI Clock Channel Timing	412
Figure 192: DSI Data to Clock Channel Timings	412
Figure 193: Rising and Falling Timings on Clock and Data Channels	413
Figure 194: BTA from the MPU to the Display Module	414
Figure 195: BTA from the Display Module to the MPU	414
Figure 196: Data Lanes - Low Power Mode to High Speed Mode Timings.....	415
Figure 197: Data Lanes - High Speed Mode to Low Power Mode Timings.....	416
Figure 198: Clock Lanes - High Speed Mode to/from Low Power Mode Timings	417
Figure 199: Reference Circuit.....	419

List of Tables

Table 1: System Operating Mode	23
Table 2: Bus Interface Pins	26
Table 3: Driver Output Pins	29
Table 4: Charge Pump Relative Pins	30
Table 5: DC/DC Converter Pins	30
Table 6: Power Pins	31
Table 7: Test Pins	32
Table 8: DBI Type B Parallel Interface	46
Table 9: DBI Type C Serial Interface	52
Table 10: DPI Interface Selection	61
Table 11: High Speed and Low-Power Lane Pair State Codes	65
Table 12: Entering and Leaving Sequences	71
Table 13: Escape Commands	72
Table 14: Abbreviations	80
Table 15: Data Types (DT) from the MPU to the Display Module (ILI9806G)	89
Table 16: Data Types (DT) from the Display Module (ILI9806G) to the MPU	90
Table 17: One Bit Error Value of the Error Correction Code (ECC)	97
Table 18: Display Command Set (DCS) Write, No Parameters (DCSWN-S)	101
Table 19: Display Command Set (DCS) Write, 1 Parameter (DCSW1-S)	102
Table 20: Display Command Set (DCS) Write Long (DCSW-L)	103
Table 21: Display Command Set (DCS) Read, No Parameter (DCSRN-S)	107
Table 22: Receiving and Transmitting EoTP during LPDT	111
Table 23: Acknowledge with Error Report (AwER) for Long Packet (LPa) Response	115
Table 24: Acknowledge with Error Report (AwER) for Short Packet (SPa) Response	115
Table 25: Interface Level Communication	122
Table 26: Packet Level Communication	122
Table 27: DCS Write, 1 Parameter Sequence – Example 1	123
Table 28: DCS Write, 1 Parameter Sequence – Example 2	123
Table 29: DCS Write, 1 Parameter Sequence – Example 3	123
Table 30: DCS Write, No Parameter Sequence – Example 1	124
Table 31: DCS Write, No Parameter Sequence – Example 2	124
Table 32: DCS Write, No Parameter Sequence – Example 3	124
Table 33: DCS Write Long Sequence – Example 1	125
Table 34: DCS Write Long Sequence – Example 2	125
Table 35: DCS Write Long Sequence – Example 3	125
Table 36: DCS Write Long Sequence – Example 4	127
Table 37: DCS Read, No Parameter Sequence – Example 1	127

Table 38: DCS Read, No Parameter Sequence – Example 2	128
Table 39: Null Packet, No Data Sequence - Example	129
Table 40: End of Transmission Packet – Example	129
Table 41: List of Supported MDDI Packets	138
Table 42: Pixel Data Attributes	141
Table 43: 16/18-bit Color Data Mapping to 24-bit Pixel Data Operation.....	171
Table 44: Tearing Effect Line Timing	352
Table 45: Initial Values of Registers	376
Table 46: Output and I/O Pins.....	377
Table 47: Reset Timing	378
Table 48: Reset Description	378
Table 49: Absolute Maximum Ratings	400
Table 50: Spike/Glitch Rejection	403
Table 51: DSI Clock Channel Timing	412
Table 52: DSI Data to Clock Channel Timings.....	412
Table 53: Rising and Falling Timings on Clock and Data Channels	413
Table 54: Low Power State Period Timings – A	414
Table 55: Low Power State Period Timings – B.....	414
Table 56: Data Lanes - Low Power Mode to High Speed Mode Timings	415
Table 57: Data Lanes - High Speed Mode to Low Power Mode Timings	416
Table 58: Clock Lanes - High Speed Mode to/from Low Power Mode Timings.....	417
Table 59: External Component Table.....	420

1. Introduction

The ILI9806G is a 16.7M single-chip SOC driver for a-Si TFT liquid crystal display panels with a resolution of up to 480 (RGB) x 864 memory size. The ILI9806G is comprised of a 1440-channel source driver, a gate-IC-less level shifter, a 1,244,160-byte GRAM for graphic data of 480 (RGB) x 864 dots, and a power supply circuit.

The ILI9806G supports parallel MPU 8-/9-/16-/18-/24-bit data bus interfaces and a 3-line serial peripheral interface to input commands. The ILI9806G supports a RGB (16-/18-/24-bit) data bus for video image display. For high-speed serial interface, the MIPI DSI and MDDI (Mobile Display Digital Interface) interface mode, the ILI9806G supports two data lanes and one clock lane for high-speed and low power transmission in both directions with low EMI noise.

The ILI9806G operates with a wide range of an analog power supply. The ILI9806G supports 8-color display, sleep mode and deep standby power management functions, ideal for medium or small size portable products where battery power conservation is desirable, such as digital cellular phones, smart phones, MP3 players, personal media players, and similar devices with color graphics display. Additionally, it has an internal DC/DC converter that generates the LCD driving voltage and the voltage follower circuit for LCD driver.

2. Features

- ◆ Display resolution options:
 - 480 (RGB) (H) x 864 (V) with GRAM
 - 480 (RGB) (H) x 854 (V) with GRAM
 - 480 (RGB) (H) x 800 (V) with GRAM
 - 480 (RGB) (H) x 720 (V) with GRAM
 - 480 (RGB) (H) x 640 (V) with GRAM

- ◆ Display color modes
 - Full color mode:
 - 16.7M colors (24-bit data, R: 8-bit, G: 8-bit, B: 8-bit)
 - Reduced color modes:
 - 262K colors (18-bit data, R: 6-bit, G: 6-bit, B: 6-bit)
 - 65K colors (16-bit data, R: 5-bit, G: 6-bit, B: 5-bit)
 - 8 colors (Idle Mode On): 8 colors (3-bit data, R: 1-bit, G: 1-bit, B: 1-bit)

- ◆ Display module:
 - On-chip Frame Memory size 1,244,160 bytes, 480 (RGB) (H) x 864 (V) x 24 bits
 - Supports 1440 source channel outputs
 - Supports gate control signals to gate driver in the panel
 - Supports 1-dot/2-dot/3-dot/4-dot/column
 - Gamma correction (1 preset Gamma curve)
 - On module VCOM control (VCL+0.2V to 0V common electrode output voltage range)

- ◆ Display interface types:
 - MPU mode:
 - MIPI-DBI Type B (Display Bus Interface, 80 System) interface, 8/9/16/18/24-bit bus
 - MIPI-DBI Type C (Serial data transfer interface, 3-line SPI) interface
 - MIPI-DSI (Display Serial Interface) interface:
 - Supports one data lane/maximum speed 850Mbps or
 - Supports two data lanes/maximum speed 500Mbps
 - Supports DSI version 1.01.00
 - Supports D-PHY version 1.00.00
 - Supports DCS version 1.02.00
 - MDDI (Mobile Display Serial Interface):
 - Supports one data lane/maximum speed 800Mbps or
 - Supports two data lanes/maximum speed 400Mbps
 - Supports MDDI V1.2 1 strobe
 - MIPI-DPI (Display Pixel Interface) interface:
 - 16 bit/pixel (R: 5-bit, G: 6-bit, B: 5-bit)
 - 18 bit/pixel (R: 6-bit, G: 6-bit, B: 6-bit)
 - 24 bit/pixel (R: 8-bit, G: 8-bit, B: 8-bit)

- ◆ Power saving modes:
 - Deep-standby mode
 - Sleep mode

- ◆ Other on-chip functions/Miscellaneous
 - Supports inversion mode
 - Software programmable color depth mode
 - Oscillator for display clock generation
 - Supports DC VCOM driving
 - DC VCOM voltage generator and adjustment
 - OTP (One-Time Programming) memory store initialization register settings
 - Provide 3 times to store DC VCOM value setting, ID setting
 - Supports CABC (Content Adaptive Brightness Control) function
 - Supports 3-Gamma DGC (Digital Gamma Correction) function
 - Color enhancement function
 - DC/DC converter
 - VGH/VGLO voltage generator for gate control signal in panel
 - Supports gate control signals to gate driver in panel (GIP)

- ◆ Input power:
 - I/O supply voltage range : $VDDI - VSSI = 1.65V \sim 3.3V$ (VDDI)
 - Analog supply voltage range : $Vddb - VSSB/VDDA - VSSA/VDDR - VSSR = 2.5V \sim 3.3V$
 - MIPI/MDDI regulator range : $VDDAM - VSSAM = 2.5V \sim 3.3V$
 - OTP programming voltage, $VPP = 7.5V$

- ◆ Source/VCOM/Gate power supply voltage:
 - $AVDD-AVSS = 4.75$ to $6.5V$ (Step-up 1 output voltage range)
 - $AVEE-AVSS = -6.5$ to $-4.75V$ (Step-up 2 output voltage range)
 - $VCL-GND = -VCI$ to $-1.8V$ (Step-up 3 output voltage range)
 - $DC VCOM = VCL+0.2V$ to $0V$, a step $12.5mV$ (Common electrode voltage range)
 - $VGMP = 3.0V$ to $6.1875V$ ($AVDD-0.3V$) (Positive gamma high voltage range)
 - $VGSP = 0.0V$ to $3.475V$ (Positive gamma low voltage range)
 - $VGMPN = -3.0V$ to $-6.1875V$ ($AVEE+0.3V$) (Negative gamma high voltage range)
 - $VGSN = 0.0V$ to $-3.475V$ (Negative gamma low voltage range)
 - $VGH-AVSS = 12V$ to $20V$ (Positive gate driver output voltage range)
 - $VGL-AVSS = -7V$ to $-15V$ (Negative gate driver output voltage range)
 - $LVGL-AVSS = -7V$ to $-15V$ (Negative gate driver output voltage range)
 - $VRGH = 1.0V \sim 6.0V$ ($AVDD-0.3V$) (Panel voltage range)

3. Device Overview

3.1. Block Diagram

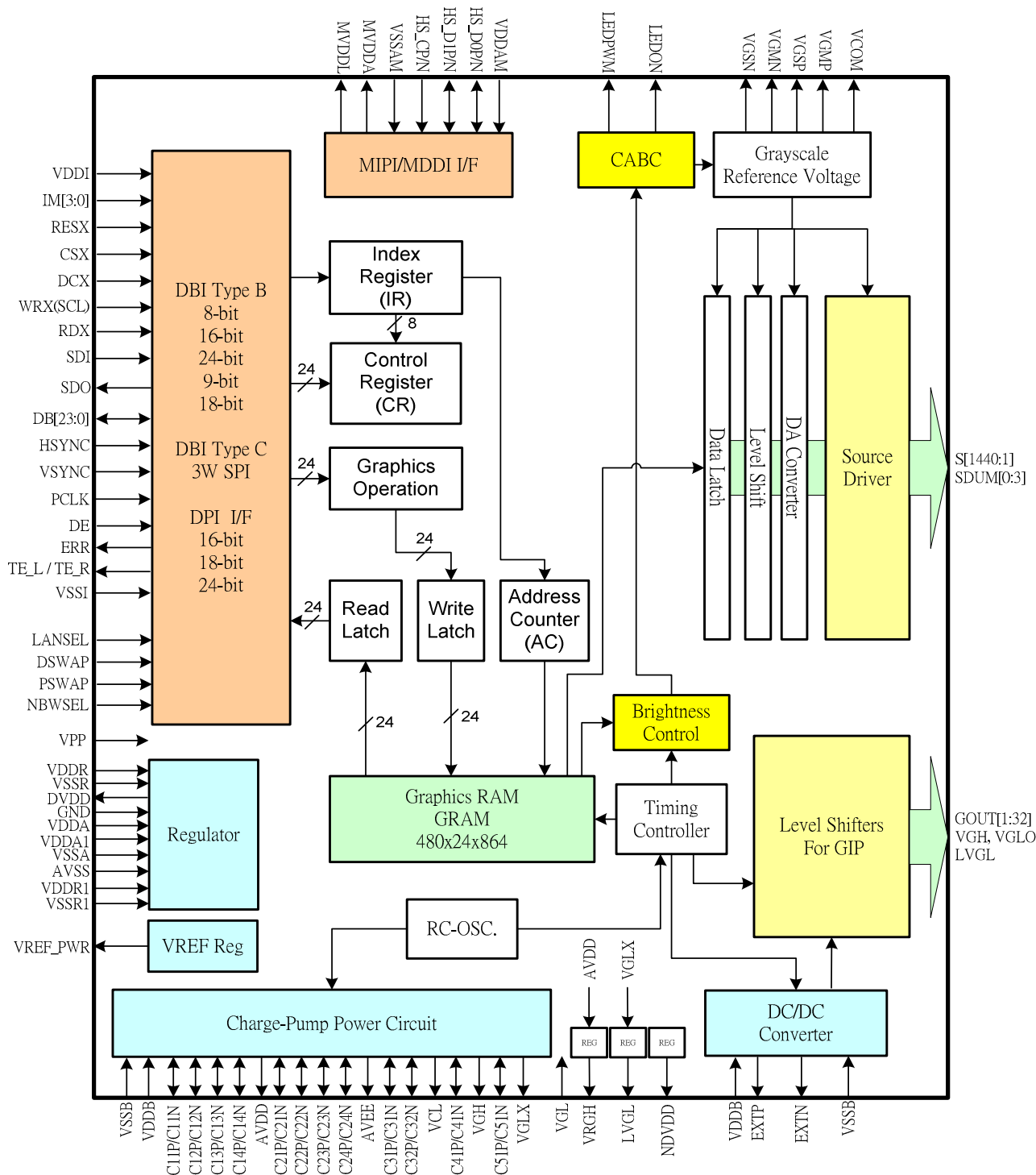


Figure 1: Block Diagram

3.2. Block Function Description

3.2.1. System Interface

The interface operating mode (DBI, DPI or DSI) is selected by hardware pins IM [3:0], as shown in Table 1 below.

Table 1: System Operating Mode ^{Note 1}

IM3	IM2	IM1	IM0	Interface	IO Pin in Use
0	0	0	0	DBI Type B 8-bit bus interface	DB [7:0], WRX, RDX, CSX, DCX
0	0	0	1	DBI Type B 16-bit bus interface	DB [15:0], WRX, RDX, CSX, DCX
0	0	1	0	DBI Type B 24-bit bus interface	DB [23:0], WRX, RDX, CSX, DCX
1	1	0	0	DBI Type B 9-bit bus interface	DB [8:0], WRX, RDX, CSX, DCX
1	1	0	1	DBI Type B 18-bit bus interface	DB [17:0], WRX, RDX, CSX, DCX
X	0	1	1	DPI with DBI Type C 3-line 9-bit	DB [23:0], SDI, SDO, SCL, CSX
0	1	0	1	MIPI DSI Interface	HS_D0P, HS_D0N, HS_D1P, HS_D1N, HS_CP, HS_CN
0	1	1	0	MDDI Interface	HS_D0P, HS_D0N, HS_D1P, HS_D1N, HS_CP, HS_CN

3.2.2. Parallel RGB Interface

The RGB interface is used as the external interface for displaying moving pictures. When the RGB interface is selected, display operations are synchronized with the externally supplied signals, VSYNC, HSYNC, and PCLK. In the RGB interface mode, data (DB23-0) are written in synchronization with these signals according to the polarity of the Enable Signal (DE). This is done in order to prevent flicker on the display while updating display data.

The RGB interface allows transferring data only when updating the frames of a moving picture by writing all display data to the internal RAM. This method is a contributing factor for the low power requirement of moving picture display.

The ILI9806G includes an IR (index register) which stores the index data of internal control register and GRAM. When DCX = L, the command is written into the driver IC via the DBI interface. When DCX = H, GRAM data via the R2Ch register is written through the data bus. When the data is written into the GRAM from the MPU, it is first written into the write-data latch and then automatically written into the GRAM by internal operation. Data is read through the read-data latch when reading display data from the GRAM.

^{Note 1} Set Number of colors using set pixel format: 3Ah.

3.2.3. Address Counter (AC)

The address counter (AC) assigns an address for writing pixel data to the GRAM, or for reading pixel data from the GRAM. Each time a pixel data is written into the GRAM, the X address or Y address of the AC is automatically increased by 1 (or decreased by 1), as determined by the register setting (MV, MX and MY bit). To simplify the address control of the GRAM access, the window address function allows writing data only to a window area of the GRAM specified by Column and Row address registers. After data is written to the GRAM, the AC will be increased or decreased within the setting window address range specified by the Column address register (start: SC, end: EC) and the Row address register (start: SP, end: EP). The window address function enables writing data only in the rectangular area set by users on the GRAM.

3.2.4. Graphic RAM (GRAM)

GRAM is the graphic RAM storing bit-pattern data of 1,244,160 bytes with 24 bits per pixel, enabling a maximum of 480(RGB) x 864 dots graphic display.

3.2.5. Grayscale Voltage Generating Circuit

The grayscale voltage generating circuit generates the LCD drive voltage which corresponds to 256 grayscale level set in the Gamma correction register. The ILI9806G can display up to 16.7M colors at maximum.

3.2.6. Timing Generating

The timing generator is used to generate timing signals for operating internal circuits. The timing generator generates timing signals for internal circuits, such as the internal GRAM. Timing for display operations (such as RAM read operation) and timing for internal operations (such as RAM access by the MPU) are outputted separately so that they do not interfere with each other.

3.2.7. Oscillator

The ILI9806G incorporates with an RC oscillator circuit. Command settings are used to change the frame frequency.

3.2.8. Source Driver Circuit

The LCD display driver circuit consists of a 480-output source driver (S1~S1440). The display pattern data is latched when 480RGB pixels of data are input. The voltage is output from the source driver according to the latched data.

3.2.9. Panel Control Circuit

The panel control circuit outputs GOUT [1:32] signals at either the VGH or VGLO or AVDD level.

3.2.10. Power Supply Circuit

The LCD drive power supply circuit generates the voltage levels for driving a panel. Voltage levels are adjusted according to the register setting.

3.2.11. MIPI DSI Controller Circuit

The MIPI DSI controller circuit consists of the D-PHY controller, Protocol Control Unit (PCU), Packet Processing Unit (PPU), ECC generating circuit, internal data/command buffer and analog transceiver. The D-PHY controls communication with the analog block, and the ECC generating circuit generates the ECC to check the outgoing data stream for accuracy of the receiving data packet. The PCU controls outgoing and incoming data streams, and the PPU controls transmitting packet distribution and merging. The internal data and command buffer is used for temporary storage of incoming commands and display data.

3.2.12. MDDI

The ILI9806G supports MDDI as a differential small amplitude serial interface for high-speed data transfer.

3.2.13. CABC (Content Adaptive Brightness Control)

The CABC (Content Adaptive Brightness Control) dynamic backlight control function is used to reduce the power consumption of the luminance source.

3.3. Pin Descriptions

Table 2: Bus Interface Pins

Bus Interface Pins						
Pin Name	I/O	Descriptions				
IM [3:0]	I	- Select the interface mode				
		IM3	IM2	IM1	IM0	Interface
		0	0	0	0	DBI Type B 8-bit
		0	0	0	1	DBI Type B 16-bit
		0	0	1	0	DBI Type B 24-bit
		1	1	0	0	DBI Type B 9-bit
		1	1	0	1	DBI Type B 18-bit
		X	0	1	1	DPI with DBI Type C 3-line 9-bit
		0	1	0	1	MIPI DSI
		0	1	1	0	MDDI
RESX	I	- The external reset input - Initializes the chip with a low input. Be sure to execute a power-on reset after supplying power.				
CSX	I	- A chip select signal. Low: the chip is selected and accessible High: the chip is not selected and not accessible Fix to VDDI or VSSI level when not in use.				
DCX	I	- The DBI Type B interface (DCX): The signal for command or parameter select. Low: Command High: Parameter Fix to VDDI or VSSI level when not in use.				
RDX	I	- Serves as a read signal and read data at the rising edge. Fix to VDDI or VSSI level when not in use.				
WRX (SCL)	I	- The DBI Type B system (WRX): Serves as a write signal and writes data at the rising edge. - Serial interface (SCL): Serial clock input Fix to VDDI or VSSI level when not in use.				
DB [23:0]	I/O	- A 24-bit parallel bi-directional data bus for MPU system				
		Interface Mode		Data Pin in Use		
		DBI Type B 8-bit		DB [7:0]		
		DBI Type B 16-bit		DB [15:0]		
		DBI Type B 24-bit		DB [23:0]		
		DBI Type B 9-bit		DB [8:0]		
		DBI Type B 18-bit		DB [17:0]		
DPI with DBI Type C 3-line 9-bit		DB [23:0], SDI, SDO				
Fix to VSSI level when not in use.						
SDI (SDA)	I/O	Serial data input pin used for the SPI Interface. SDI: Serial data input pin				

		SDA: Serial data input/output bidirectional pin Fix to VDDI or VSSI level when not in use.																																												
SDO	O	Serial data output pin used for the SPI Interface. Leave the pin open when not in use.																																												
TE_L / TE_R	O	-Tearing effect output TE = TE_L= TE_R Leave the pin open when not in use.																																												
PCLK	I	- Dot clock signal for RGB interface operation Fix to VDDI or VSSI level when not in use.																																												
VSYNC	I	- Frame synchronizing signal for RGB interface operation Fix to VDDI or VSSI level when not in use.																																												
HSYNC	I	- Line synchronizing signal for RGB interface operation Fix to VDDI or VSSI level when not in use.																																												
DE	I	- Data enable signal for RGB interface operation Low: access enabled High: access inhibited Fix to VDDI or VSSI level when not in use.																																												
HS_CP HS_CN	I	MIPI DSI differential clock pair (DSI-CLK+/-) If MIPI are not in use, they should be connected to VSSAM. MDDI strobe signal lines (MDDI_Stb_P/M) HS_CP (Stb+) and HS_CN (Stb-) are differential small swing signals. Make the wiring as short as possible so that the COG resistance becomes less than 10 ohm. The specifications of the interface must be compliant with the MDDI specification. If MDDI are not in use, they should be connected to VSSAM.																																												
HS_D0P HS_D0N HS_D1P HS_D1N	I/O	MIPI DSI differential data pair (DSI-D0+/- 、DSI-D1+/-) If MIPI are not in use, they should be connected to VSSAM MDDI data signal lines (MDDI_Data0_P/M 、MDDI_Data1_P/M) HS_D0P (Data+) and HS_D0N (Data-) are differential small swing signals. Make the wiring as short as possible so that the COG resistance becomes less than 10 ohm. The specifications of the interface must be compliant with the MDDI specification. If MDDI are not in use, they should be connected to VSSAM.																																												
ERR	O	- CRC and ECC error output pin for the MIPI interface, activated by S/W command. This pin is output low when it is not activated. When this pin is activated, it is output high if CRC/ECC error is found. Leave the pin open when not in use.																																												
LANSEL	I	- Input pin to select 1 data lane or 2 data lanes in MIPI/MDDI interface. Low: 1 data lane High: 2 data lanes Fix to VSSI level when not in use.																																												
DSWAP PSWAP	I	- Differential clock polarity swap For MIPI interface <table><tr><th rowspan="2">DSWAP</th><th rowspan="2">PSWAP</th><th colspan="6">Pins</th></tr><tr><th>HS_CP</th><th>HS_CN</th><th>HS_D0P</th><th>HS_D0N</th><th>HS_D1P</th><th>HS_D1N</th></tr><tr><td rowspan="2">0</td><td>0</td><td>HS_CP</td><td>HS_CN</td><td>HS_D0P</td><td>HS_D0N</td><td>HS_D1P</td><td>HS_D1N</td></tr><tr><td>1</td><td>HS_CN</td><td>HS_CP</td><td>HS_D0N</td><td>HS_D0P</td><td>HS_D1N</td><td>HS_D1P</td></tr><tr><td rowspan="2">1</td><td>0</td><td>HS_CP</td><td>HS_CN</td><td>HS_D1P</td><td>HS_D1N</td><td>HS_D0P</td><td>HS_D0N</td></tr><tr><td>1</td><td>HS_CN</td><td>HS_CP</td><td>HS_D1N</td><td>HS_D1P</td><td>HS_D0N</td><td>HS_D0P</td></tr></table>	DSWAP	PSWAP	Pins						HS_CP	HS_CN	HS_D0P	HS_D0N	HS_D1P	HS_D1N	0	0	HS_CP	HS_CN	HS_D0P	HS_D0N	HS_D1P	HS_D1N	1	HS_CN	HS_CP	HS_D0N	HS_D0P	HS_D1N	HS_D1P	1	0	HS_CP	HS_CN	HS_D1P	HS_D1N	HS_D0P	HS_D0N	1	HS_CN	HS_CP	HS_D1N	HS_D1P	HS_D0N	HS_D0P
DSWAP	PSWAP	Pins																																												
		HS_CP	HS_CN	HS_D0P	HS_D0N	HS_D1P	HS_D1N																																							
0	0	HS_CP	HS_CN	HS_D0P	HS_D0N	HS_D1P	HS_D1N																																							
	1	HS_CN	HS_CP	HS_D0N	HS_D0P	HS_D1N	HS_D1P																																							
1	0	HS_CP	HS_CN	HS_D1P	HS_D1N	HS_D0P	HS_D0N																																							
	1	HS_CN	HS_CP	HS_D1N	HS_D1P	HS_D0N	HS_D0P																																							

		<div>For MDDI interface</div> <table><tr><th rowspan="2">DSWAP</th><th rowspan="2">PSWAP</th><th colspan="6">Pins</th></tr><tr><th>HS_CP</th><th>HS_CN</th><th>HS_D0P</th><th>HS_D0N</th><th>HS_D1P</th><th>HS_D1N</th></tr><tr><td rowspan="2">0</td><td>0</td><td>HS_CP</td><td>HS_CN</td><td>HS_D0P</td><td>HS_D0N</td><td>HS_D1P</td><td>HS_D1N</td></tr><tr><td>1</td><td>HS_CN</td><td>HS_CP</td><td>HS_D0N</td><td>HS_D0P</td><td>HS_D1N</td><td>HS_D1P</td></tr></table> <div>Fix to VSSI level when not in use.</div>	DSWAP	PSWAP	Pins						HS_CP	HS_CN	HS_D0P	HS_D0N	HS_D1P	HS_D1N	0	0	HS_CP	HS_CN	HS_D0P	HS_D0N	HS_D1P	HS_D1N	1	HS_CN	HS_CP	HS_D0N	HS_D0P	HS_D1N	HS_D1P
DSWAP	PSWAP	Pins																													
		HS_CP	HS_CN	HS_D0P	HS_D0N	HS_D1P	HS_D1N																								
0	0	HS_CP	HS_CN	HS_D0P	HS_D0N	HS_D1P	HS_D1N																								
	1	HS_CN	HS_CP	HS_D0N	HS_D0P	HS_D1N	HS_D1P																								
RGBBP	I	- Test Pin Fix to VSSI level.																													
GPO [3:0]	O	- Test Pin Leave the pin open.																													
EXB1T	I	- Input pin to select the external DC/DC circuit. Low: Using internal DC/DC for AVDD / AVEE High: Using external DC/DC for AVDD / AVEE Fix to VSSI level when not in use.																													
NBWSEL	I	- Input pin to select the gamma voltage level sequence of V0~V255. Low: V0 > V1 >...> V254 > V255, normally white High: V255 > V254 >...> V1 > V0, normally black Fix to VDDI level when not in use.																													
LEDON	O	- Used for turning On/Off external LED backlight control. Leave the pin open when not in use.																													
LEDPWM	O	- The PWM frequency output for LED driver control. Leave the pin open when not in use.																													

Table 3: Driver Output Pins

Driver Output Pins			
Pin Name	I/O	Type	Descriptions
S [1:1440]	O	LCD	- Source output voltage signals applied to a LCD panel
GOUT [1:32]	O	LCD	- Gate control signals and the swing voltage level is VGH to VGLO
SDUM [0:3]	O	LCD	- Dummy Source Leave the pin open when not in use.
VGH	O	LCD	- High voltage level for gate control signals and gate circuit of panel VGH is already connected to VGHO in IC.
VGLO (VGLO_L / VGLO_R)	O	LCD	- Low voltage level for gate control signals and gate circuit of panel
LVGL (LVGL_L / LVGL_R)	O	LCD	- Low voltage level for gate circuit of panel LVGL is already connected to VGL_REG in IC. (VGL_REG is the output voltage generated from VGL. LDO output used for panel voltage.) - Connect a capacitor for stabilization
VGMP (VGMP_PAD)	O	LCD	- Output voltage generated from AVDD. LDO output for positive gamma high voltage generator.
VGSP (VGSP_PAD)	O	LCD	- Output voltage generated from AVDD. LDO output for positive gamma low voltage generator.
VGMN (VGMN_PAD)	O	LCD	- Output voltage generated from AVEE. LDO output for negative gamma high voltage generator.
VGSN (VGSN_PAD)	O	LCD	- Output voltage generated from AVEE. LDO output for negative gamma low voltage generator.

Table 4: Charge Pump Relative Pins

Charge Pump Relative Pins			
Pin Name	I/O	Type	Descriptions
AVDD	O	Stabilizing capacitor	- Output voltage from step-up circuit 1, generated from VDDB. - Connect to a stabilizing capacitor between AVDD and VSSB.
AVEE	O	Stabilizing capacitor	- Output voltage from step-up circuit 2, generated from VDDB. - Connect to a stabilizing capacitor between AVEE and VSSB.
VCL	O	Stabilizing capacitor	- Output voltage from step-up circuit 3, generated from VDDB. - Connect to a stabilizing capacitor between VCL and VSSB.
VGH	O	Stabilizing capacitor	- Output voltage from step-up circuit 4, generated from VDDB. - Connect to a stabilizing capacitor between VGH and VSSB.
VGL	O	Stabilizing capacitor	- Substrate voltage for driver IC - Output voltage from step-up circuit 5, generated from VDDB. - Connect to a stabilizing capacitor between VGL and VSSB.
C11P, C11N C12P, C12N C13P, C13N C14P, C14N	-	Flying capacitor	- Connect the charge-pumping capacitor for generating AVDD level. - Capacitor connection pins for the step-up circuit 1.
C21P, C21N C22P, C22N C23P, C23N C24P, C24N	-	Flying capacitor	- Connect the charge-pumping capacitor for generating AVEE level. - Capacitor connection pins for the step-up circuit 2.
C31P, C31N C32P, C32N	-	Flying capacitor	- Connect the charge-pumping capacitor for generating VCL level. - Capacitor connection pins for the step-up circuit 3.
C41P, C41N	-	Flying capacitor	- Connect the charge-pumping capacitor for generating VGH level. - Capacitor connection pins for the step-up circuit 4.
C51P, C51N	-	Flying capacitor	- Connect the charge-pumping capacitor for generating VGL level. - Capacitor connection pins for the step-up circuit 5.

Table 5: DC/DC Converter Pins

DC/DC Converter Pins			
Pin Name	I/O	Type	Descriptions
EXTN (CTRL_A)	O	Positive NMOS	-PWM control output for gate of NMOS in positive DC/DC converter (for AVDD) -CTRL_A : Control signal for an external charge pump IC (ex: ILI4002)
EXTP (CTRL_B)	O	Negative PMOS	-PWM control output for gate of PMOS in negative DC/DC converter (for AVEE) -CTRL_B : Control signal for an external charge pump IC (ex: ILI4002)

Table 6: Power Pins

Power Pins			
Pin Name	I/O	Type	Descriptions
VRGH (VRGH_L / VRGH_R)	O	LDO Stabilizing Capacitor	- Output voltage generated from AVDD. - Connect a capacitor for stabilization. Leave the pin open when not in use.
VREF_PWR	O	LDO Stabilizing Capacitor	- Reference voltage for regulator output. - Connect a capacitor for stabilization.
VDDA	P	Analog	- Power supply for analog system. - VDDA, VDDR, VDDA1, VDDDB and VDDR1 should be the same input voltage level of 2.5 ~ 3.3V.
VDDA1	P	Analog	- Power supply for analog system. - VDDA, VDDR, VDDA1, VDDDB and VDDR1 should be the same input voltage level of 2.5 ~ 3.3V.
VDDR	P	Regulator	- Power supply for regulator system. - VDDA, VDDR, VDDA1, VDDDB and VDDR1 should be the same input voltage level of 2.5 ~ 3.3V.
VDDR1	P	Regulator	- Power supply for regulator system. - VDDA, VDDR, VDDA1, VDDDB and VDDR1 should be the same input voltage level of 2.5 ~ 3.3V.
VDDDB	P	DC/DC	- Power supply for DC/DC converter. - VDDA, VDDR, VDDA1, VDDDB and VDDR1 should be the same input voltage level of 2.5 ~ 3.3V.
VDDI	P	I/O	- Power supply for I/O block.
DVDD	O	Stabilizing Capacitor	- Internal logic voltage output - Connect a capacitor for stabilization.
NDVDD	O	Stabilizing Capacitor	- Negative internal logic voltage output - Connect a capacitor for stabilization.
VDDAM	P	MIPI/MDDI	- Power supply for MIPI/MDDI analog system.
MVDDA	O	MIPI Stabilizing Capacitor	- Regulator output for internal MIPI / MDDI analog system (1.5V typical) - Connect a capacitor for stabilization.
MVDDL	O	MIPI Stabilizing Capacitor	- Regulator output for internal MIPI low power system (1.2V typical) - Connect a capacitor for stabilization.
VSSA	P	Analog	- System ground for analog circuit.
VSSR	P	Regulator	- System ground for regulator circuit.
VSSR1	P	Regulator	- System ground for regulator circuit.
VSSB	P	DC/DC	- System ground for DC/DC convertor.
VSSI	P	I/O	- System ground for interface system.
GND	P	Digital	- System ground for internal digital system.
AVSS	P	Source OP	- System ground for source OP system.
VSSAM	P	MIPI/MDDI	- System ground for MIPI/MDDI system.
VPP	I	OTP	- OTP programming power.
VCOM (VCOM_L /	O	LDO Stabilizing	- Output voltage generated from VCI / VCL - Connect a capacitor for stabilization.

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VCOM_R)		Capacitor	VCOM=VCOM_L=VCOM_R
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Table 7: Test Pins

Test Pins			
Pin Name	I/O	Type	Descriptions
PADA [1:4] PADB [1:4]	I/O		- Dummy Pin.
CONTACT1A CONTACT1B	I/O		- Test pin, for test bonding quality, IC internal connect CONTACT1A with CONTACT1B.
KBBC	O		- Test pin, It's not accessible to user. MUST be left open.
VSEL	-		- Dummy pin.
TEST [0:3]	I		- Test pin, It's not accessible to user. MUST be left open. (Internal weakly pull low)
OSC_TEST	I		- Test pin, It's not accessible to user, MUST be left open (Internal weakly pull low)
VSSIDUM [0:106]	O		- These are dummy pins with VSSI potential (There are no function inside). - Signal traces cannot pass through on glass under these pads.
DUMMY	-		- Dummy pads. Leave the pin open.

3.4. Pin Assignment

Chip Size : 24360um X 1530um (include scribe line)

Chip Thickness : 280um(typ.)

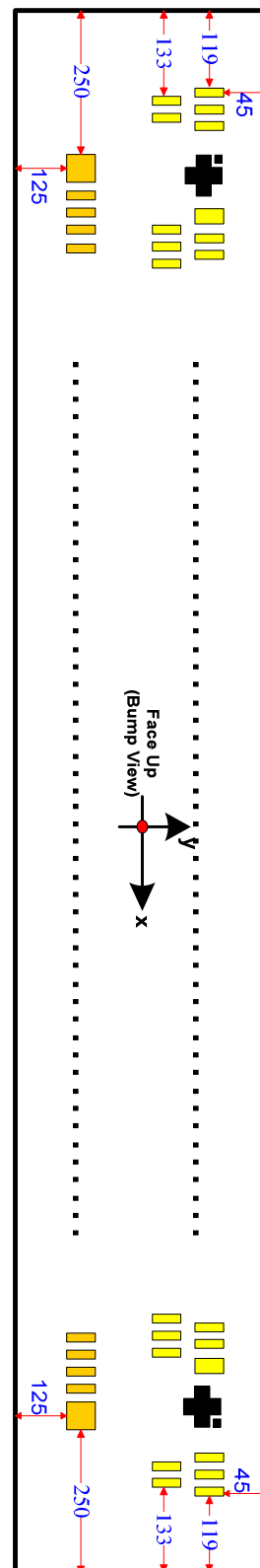
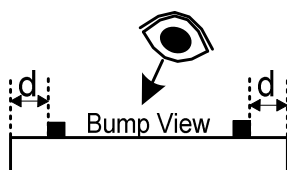
Pad Location : Pad Center

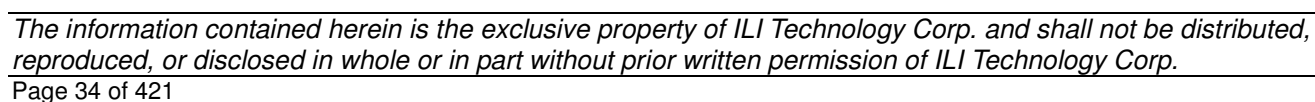
Coordinate Origin : Chip Center

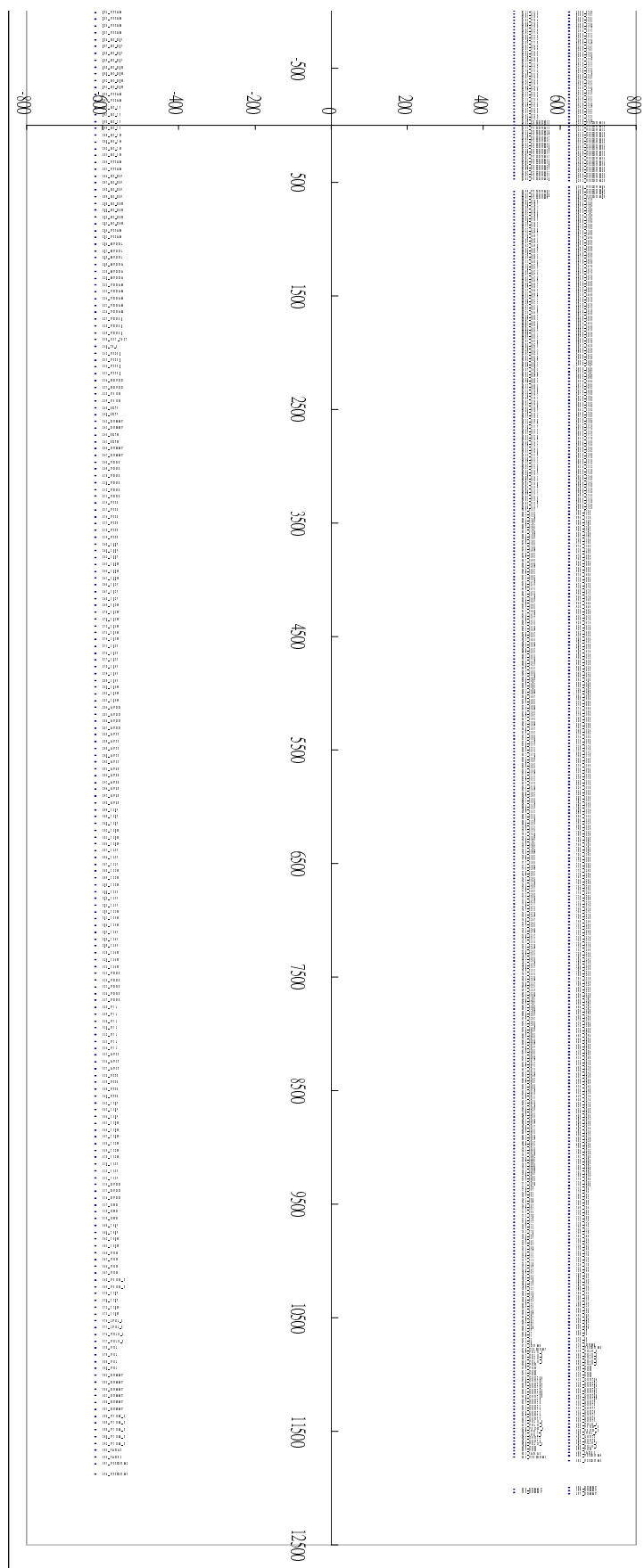
Au Bump Size :

1. 14um X 115um

2. 40um X 120um







3.5. Bump Arrangement

Output PAD	<p>Unit: um</p>
Input PAD	<p>Unit: um</p>
Alignment mark	<p>Unit: um</p> <p>ALMARK_L_T</p> <p>ALMARK_R_T</p>

3.6. Pad Coordination

No.	Text Name	X-axis	Y-axis	No.	Text Name	X-axis	Y-axis	No.	Text Name	X-axis	Y-axis	No.	Text Name	X-axis	Y-axis
1	VSSIDUM0	-11880	-620	61	VGMP_PAD	-8250	-620	121	DB[20]	-4650	-620	181	VSSAM	-1050	-620
2	VSSIDUM1	-11790	-620	62	GND	-8190	-620	122	DB[19]	-4590	-620	182	VSSAM	-990	-620
3	PADA1	-11730	-620	63	GND	-8130	-620	123	DB[18]	-4530	-620	183	VSSAM	-930	-620
4	PADB1	-11670	-620	64	GND	-8070	-620	124	DB[17]	-4470	-620	184	VSSAM	-870	-620
5	VCOM_L	-11610	-620	65	DVDD	-8010	-620	125	DB[16]	-4410	-620	185	VSSAM	-810	-620
6	VCOM_L	-11550	-620	66	DVDD	-7950	-620	126	DB[15]	-4350	-620	186	HS_D1P	-750	-620
7	VCOM_L	-11490	-620	67	DVDD	-7890	-620	127	DB[14]	-4290	-620	187	HS_D1P	-690	-620
8	VCOM_L	-11430	-620	68	VDDDB	-7830	-620	128	DB[13]	-4230	-620	188	HS_D1P	-630	-620
9	VCOM_L	-11370	-620	69	VDDDB	-7770	-620	129	DB[12]	-4170	-620	189	HS_D1P	-570	-620
10	CONTACT1A	-11310	-620	70	VDDDB	-7710	-620	130	DB[11]	-4110	-620	190	HS_D1N	-510	-620
11	CONTACT1B	-11250	-620	71	VCL	-7650	-620	131	DB[10]	-4050	-620	191	HS_D1N	-450	-620
12	VPP	-11190	-620	72	VCL	-7590	-620	132	DB[9]	-3990	-620	192	HS_D1N	-390	-620
13	VPP	-11130	-620	73	VCL	-7530	-620	133	DB[8]	-3930	-620	193	HS_D1N	-330	-620
14	VPP	-11070	-620	74	VCL	-7470	-620	134	DB[7]	-3870	-620	194	VSSAM	-270	-620
15	VPP	-11010	-620	75	VCL	-7410	-620	135	DB[6]	-3810	-620	195	VSSAM	-210	-620
16	VPP	-10950	-620	76	VCL	-7350	-620	136	DB[5]	-3750	-620	196	HS_CP	-150	-620
17	VGL	-10890	-620	77	AVSS	-7290	-620	137	DB[4]	-3690	-620	197	HS_CP	-90	-620
18	VGL	-10830	-620	78	AVSS	-7230	-620	138	DB[3]	-3630	-620	198	HS_CP	-30	-620
19	VGLO_L	-10770	-620	79	AVSS	-7170	-620	139	DB[2]	-3570	-620	199	HS_CP	30	-620
20	VGLO_L	-10710	-620	80	VDDI	-7110	-620	140	DB[1]	-3510	-620	200	HS_CN	90	-620
21	LVGL_L	-10650	-620	81	LANSEL	-7050	-620	141	DB[0]	-3450	-620	201	HS_CN	150	-620
22	LVGL_L	-10590	-620	82	DSWAP	-6990	-620	142	DE	-3390	-620	202	HS_CN	210	-620
23	VRGH_L	-10530	-620	83	PSWAP	-6930	-620	143	PCLK	-3330	-620	203	HS_CN	270	-620
24	VRGH_L	-10470	-620	84	VSSI	-6870	-620	144	HS	-3270	-620	204	VSSAM	330	-620
25	VCL	-10410	-620	85	DUMMY	-6810	-620	145	VS	-3210	-620	205	VSSAM	390	-620
26	VCL	-10350	-620	86	NBWSSEL	-6750	-620	146	LEDPWM	-3150	-620	206	HS_D0P	450	-620
27	VCL	-10290	-620	87	DUMMY	-6690	-620	147	LEDON	-3090	-620	207	HS_D0P	510	-620
28	VCL	-10230	-620	88	DUMMY	-6630	-620	148	KBBC	-3030	-620	208	HS_D0P	570	-620
29	VREF_PWR	-10170	-620	89	DUMMY	-6570	-620	149	ERR	-2970	-620	209	HS_D0P	630	-620
30	VREF_PWR	-10110	-620	90	DUMMY	-6510	-620	150	VDDI	-2910	-620	210	HS_D0N	690	-620
31	VREF_PWR	-10050	-620	91	VDDI	-6450	-620	151	VDDI	-2850	-620	211	HS_D0N	750	-620
32	VREF_PWR	-9990	-620	92	RGBBP	-6390	-620	152	VDDI	-2790	-620	212	HS_D0N	810	-620
33	VSSA	-9930	-620	93	DUMMY	-6330	-620	153	VSSI	-2730	-620	213	HS_D0N	870	-620
34	VSSA	-9870	-620	94	IM3	-6270	-620	154	VSSI	-2670	-620	214	VSSAM	930	-620
35	VSSA	-9810	-620	95	IM2	-6210	-620	155	VSSI	-2610	-620	215	VSSAM	990	-620
36	VSSA	-9750	-620	96	IM1	-6150	-620	156	AVDD	-2550	-620	216	MVDDL	1050	-620
37	VDDA	-9690	-620	97	IM0	-6090	-620	157	AVDD	-2490	-620	217	MVDDL	1110	-620
38	VDDA	-9630	-620	98	GPO3	-6030	-620	158	AVDD	-2430	-620	218	MVDDL	1170	-620
39	VDDA	-9570	-620	99	GPO2	-5970	-620	159	AVDD	-2370	-620	219	MVDDA	1230	-620
40	VDDA	-9510	-620	100	GPO1	-5910	-620	160	AVSS	-2310	-620	220	MVDDA	1290	-620
41	VDDR	-9450	-620	101	GPO0	-5850	-620	161	AVSS	-2250	-620	221	MVDDA	1350	-620
42	VDDR	-9390	-620	102	EXB1T	-5790	-620	162	AVSS	-2190	-620	222	VDDAM	1410	-620
43	VDDR	-9330	-620	103	TE_L	-5730	-620	163	AVSS	-2130	-620	223	VDDAM	1470	-620
44	VDDR	-9270	-620	104	VSEL	-5670	-620	164	AVEE	-2070	-620	224	VDDAM	1530	-620
45	VSSR	-9210	-620	105	SDO	-5610	-620	165	AVEE	-2010	-620	225	VDDAM	1590	-620
46	VSSR	-9150	-620	106	SDI	-5550	-620	166	AVEE	-1950	-620	226	VDDAM	1650	-620
47	VSSR	-9090	-620	107	DCX	-5490	-620	167	AVEE	-1890	-620	227	VDDR1	1710	-620
48	VSSR	-9030	-620	108	WRX	-5430	-620	168	AVEE	-1830	-620	228	VDDR1	1770	-620
49	TEST[0]	-8970	-620	109	RDX	-5370	-620	169	VDDA1	-1770	-620	229	VDDR1	1830	-620
50	TEST[1]	-8910	-620	110	CSX	-5310	-620	170	VDDA1	-1710	-620	230	OSC_TEST	1890	-620
51	TEST[2]	-8850	-620	111	RESX	-5250	-620	171	VDDA1	-1650	-620	231	TE_R	1950	-620
52	TEST[3]	-8790	-620	112	VSSI	-5190	-620	172	VDDA1	-1590	-620	232	VSSR1	2010	-620
53	VDDR	-8730	-620	113	VSSI	-5130	-620	173	GND	-1530	-620	233	VSSR1	2070	-620
54	DUMMY	-8670	-620	114	VSSI	-5070	-620	174	GND	-1470	-620	234	VSSR1	2130	-620
55	DUMMY	-8610	-620	115	VDDI	-5010	-620	175	GND	-1410	-620	235	VSSR1	2190	-620
56	VGSN_PAD	-8550	-620	116	VDDI	-4950	-620	176	GND	-1350	-620	236	NDVDD	2250	-620
57	VGSN_PAD	-8490	-620	117	VDDI	-4890	-620	177	DVDD	-1290	-620	237	NDVDD	2310	-620
58	VGSP_PAD	-8430	-620	118	DB[23]	-4830	-620	178	DVDD	-1230	-620	238	VRGH	2370	-620
59	VGMN_PAD	-8370	-620	119	DB[22]	-4770	-620	179	DVDD	-1170	-620	239	VRGH	2430	-620
60	VGMN_PAD	-8310	-620	120	DB[21]	-4710	-620	180	DVDD	-1110	-620	240	EXTP	2490	-620

No.	Text Name	X-axis	Y-axis	No.	Text Name	X-axis	Y-axis	No.	Text Name	X-axis	Y-axis	No.	Text Name	X-axis	Y-axis
241	EXTP	2550	-620	301	C21P	6150	-620	361	C41P	9750	-620	421	VRGH_R	11480	477.5
242	DUMMY	2610	-620	302	C21N	6210	-620	362	C41N	9810	-620	422	VRGH_R	11466	622.5
243	DUMMY	2670	-620	303	C21N	6270	-620	363	C41N	9870	-620	423	VGLO_R	11452	477.5
244	EXTN	2730	-620	304	C21N	6330	-620	364	VGH	9930	-620	424	VGLO_R	11438	622.5
245	EXTN	2790	-620	305	C22P	6390	-620	365	VGH	9990	-620	425	VGLO_R	11424	477.5
246	DUMMY	2850	-620	306	C22P	6450	-620	366	VGH	10050	-620	426	GOUT3	11410	622.5
247	DUMMY	2910	-620	307	C22P	6510	-620	367	VGH	10110	-620	427	GOUT3	11396	477.5
248	VDDb	2970	-620	308	C22N	6570	-620	368	VRGH_R	10170	-620	428	GOUT4	11382	622.5
249	VDDb	3030	-620	309	C22N	6630	-620	369	VRGH_R	10230	-620	429	GOUT4	11368	477.5
250	VDDb	3090	-620	310	C22N	6690	-620	370	C51P	10290	-620	430	GOUT5	11354	622.5
251	VDDb	3150	-620	311	C23P	6750	-620	371	C51P	10350	-620	431	GOUT5	11340	477.5
252	VDDb	3210	-620	312	C23P	6810	-620	372	C51N	10410	-620	432	GOUT6	11326	622.5
253	VDDb	3270	-620	313	C23P	6870	-620	373	C51N	10470	-620	433	GOUT6	11312	477.5
254	VSSb	3330	-620	314	C23N	6930	-620	374	LVGL_R	10530	-620	434	GOUT7	11298	622.5
255	VSSb	3390	-620	315	C23N	6990	-620	375	LVGL_R	10590	-620	435	GOUT7	11284	477.5
256	VSSb	3450	-620	316	C23N	7050	-620	376	VGLO_R	10650	-620	436	GOUT8	11270	622.5
257	VSSb	3510	-620	317	C24P	7110	-620	377	VGLO_R	10710	-620	437	GOUT8	11256	477.5
258	VSSb	3570	-620	318	C24P	7170	-620	378	VGL	10770	-620	438	GOUT9	11242	622.5
259	VSSb	3630	-620	319	C24P	7230	-620	379	VGL	10830	-620	439	GOUT9	11228	477.5
260	C11P	3690	-620	320	C24N	7290	-620	380	VGL	10890	-620	440	GOUT10	11214	622.5
261	C11P	3750	-620	321	C24N	7350	-620	381	VGL	10950	-620	441	GOUT10	11200	477.5
262	C11P	3810	-620	322	C24N	7410	-620	382	DUMMY	11010	-620	442	GOUT11	11186	622.5
263	C11N	3870	-620	323	VDDb	7470	-620	383	DUMMY	11070	-620	443	GOUT11	11172	477.5
264	C11N	3930	-620	324	VDDb	7530	-620	384	DUMMY	11130	-620	444	GOUT12	11158	622.5
265	C11N	3990	-620	325	VDDb	7590	-620	385	DUMMY	11190	-620	445	GOUT12	11144	477.5
266	C12P	4050	-620	326	VDDb	7650	-620	386	DUMMY	11250	-620	446	GOUT13	11130	622.5
267	C12P	4110	-620	327	VDDb	7710	-620	387	DUMMY	11310	-620	447	GOUT13	11116	477.5
268	C12P	4170	-620	328	VCL	7770	-620	388	VCOM_R	11370	-620	448	GOUT14	11102	622.5
269	C12N	4230	-620	329	VCL	7830	-620	389	VCOM_R	11430	-620	449	GOUT14	11088	477.5
270	C12N	4290	-620	330	VCL	7890	-620	390	VCOM_R	11490	-620	450	GOUT15	11074	622.5
271	C12N	4350	-620	331	VCL	7950	-620	391	VCOM_R	11550	-620	451	GOUT15	11060	477.5
272	C13N	4410	-620	332	VCL	8010	-620	392	VCOM_R	11610	-620	452	GOUT16	11046	622.5
273	C13N	4470	-620	333	VCL	8070	-620	393	PADA2	11670	-620	453	GOUT16	11032	477.5
274	C13N	4530	-620	334	VCL	8130	-620	394	PADB2	11730	-620	454	VGH	11018	622.5
275	C13P	4590	-620	335	AVSS	8190	-620	395	VSSIDUM2	11790	-620	455	VGH	11004	477.5
276	C13P	4650	-620	336	AVSS	8250	-620	396	VSSIDUM3	11880	-620	456	VGH	10990	622.5
277	C13P	4710	-620	337	AVSS	8310	-620	397	DUMMY	12054	622.5	457	VGH	10976	477.5
278	C14P	4770	-620	338	VSSb	8370	-620	398	DUMMY	12040	477.5	458	VGH	10962	622.5
279	C14P	4830	-620	339	VSSb	8430	-620	399	DUMMY	12026	622.5	459	VGH	10948	477.5
280	C14P	4890	-620	340	VSSb	8490	-620	400	DUMMY	12012	477.5	460	VGH	10934	622.5
281	C14N	4950	-620	341	VSSb	8550	-620	401	DUMMY	11998	622.5	461	VGH	10920	477.5
282	C14N	5010	-620	342	C31P	8610	-620	402	VSSIDUM4	11760	622.5	462	VGLO_R	10906	622.5
283	C14N	5070	-620	343	C31P	8670	-620	403	VSSIDUM5	11732	477.5	463	VGLO_R	10892	477.5
284	AVDD	5130	-620	344	C31P	8730	-620	404	VSSIDUM6	11718	622.5	464	VGLO_R	10878	622.5
285	AVDD	5190	-620	345	C31N	8790	-620	405	PADA3	11704	477.5	465	VGLO_R	10864	477.5
286	AVDD	5250	-620	346	C31N	8850	-620	406	PADB3	11690	622.5	466	VGLO_R	10850	622.5
287	AVDD	5310	-620	347	C31N	8910	-620	407	VGH	11676	477.5	467	VGLO_R	10836	477.5
288	AVSS	5370	-620	348	C32N	8970	-620	408	VGH	11662	622.5	468	VGLO_R	10822	622.5
289	AVSS	5430	-620	349	C32N	9030	-620	409	VGH	11648	477.5	469	VGLO_R	10808	477.5
290	AVSS	5490	-620	350	C32N	9090	-620	410	VGLO_R	11634	622.5	470	VGLO_R	10794	622.5
291	AVSS	5550	-620	351	C32P	9150	-620	411	VGLO_R	11620	477.5	471	VSSIDUM7	10780	477.5
292	AVSS	5610	-620	352	C32P	9210	-620	412	VGLO_R	11606	622.5	472	VSSIDUM8	10766	622.5
293	AVEE	5670	-620	353	C32P	9270	-620	413	GOUT1	11592	477.5	473	SDUM0	10752	477.5
294	AVEE	5730	-620	354	DVDD	9330	-620	414	GOUT1	11578	622.5	474	SDUM1	10738	622.5
295	AVEE	5790	-620	355	DVDD	9390	-620	415	GOUT2	11564	477.5	475	S1	10724	477.5
296	AVEE	5850	-620	356	DVDD	9450	-620	416	GOUT2	11550	622.5	476	S2	10710	622.5
297	AVEE	5910	-620	357	GND	9510	-620	417	LVGL_R	11536	477.5	477	S3	10696	477.5
298	AVEE	5970	-620	358	GND	9570	-620	418	LVGL_R	11522	622.5	478	S4	10682	622.5
299	C21P	6030	-620	359	GND	9630	-620	419	LVGL_R	11508	477.5	479	S5	10668	477.5
300	C21P	6090	-620	360	C41P	9690	-620	420	VRGH_R	11494	622.5	480	S6	10654	622.5

No.	Text Name	X-axis	Y-axis	No.	Text Name	X-axis	Y-axis	No.	Text Name	X-axis	Y-axis	No.	Text Name	X-axis	Y-axis
481	S7	10640	477.5	541	S67	9800	477.5	601	S127	8960	477.5	661	S187	8120	477.5
482	S8	10626	622.5	542	S68	9786	622.5	602	S128	8946	622.5	662	S188	8106	622.5
483	S9	10612	477.5	543	S69	9772	477.5	603	S129	8932	477.5	663	S189	8092	477.5
484	S10	10598	622.5	544	S70	9758	622.5	604	S130	8918	622.5	664	S190	8078	622.5
485	S11	10584	477.5	545	S71	9744	477.5	605	S131	8904	477.5	665	S191	8064	477.5
486	S12	10570	622.5	546	S72	9730	622.5	606	S132	8890	622.5	666	S192	8050	622.5
487	S13	10556	477.5	547	S73	9716	477.5	607	S133	8876	477.5	667	S193	8036	477.5
488	S14	10542	622.5	548	S74	9702	622.5	608	S134	8862	622.5	668	S194	8022	622.5
489	S15	10528	477.5	549	S75	9688	477.5	609	S135	8848	477.5	669	S195	8008	477.5
490	S16	10514	622.5	550	S76	9674	622.5	610	S136	8834	622.5	670	S196	7994	622.5
491	S17	10500	477.5	551	S77	9660	477.5	611	S137	8820	477.5	671	S197	7980	477.5
492	S18	10486	622.5	552	S78	9646	622.5	612	S138	8806	622.5	672	S198	7966	622.5
493	S19	10472	477.5	553	S79	9632	477.5	613	S139	8792	477.5	673	S199	7952	477.5
494	S20	10458	622.5	554	S80	9618	622.5	614	S140	8778	622.5	674	S200	7938	622.5
495	S21	10444	477.5	555	S81	9604	477.5	615	S141	8764	477.5	675	S201	7924	477.5
496	S22	10430	622.5	556	S82	9590	622.5	616	S142	8750	622.5	676	S202	7910	622.5
497	S23	10416	477.5	557	S83	9576	477.5	617	S143	8736	477.5	677	S203	7896	477.5
498	S24	10402	622.5	558	S84	9562	622.5	618	S144	8722	622.5	678	S204	7882	622.5
499	S25	10388	477.5	559	S85	9548	477.5	619	S145	8708	477.5	679	S205	7868	477.5
500	S26	10374	622.5	560	S86	9534	622.5	620	S146	8694	622.5	680	S206	7854	622.5
501	S27	10360	477.5	561	S87	9520	477.5	621	S147	8680	477.5	681	S207	7840	477.5
502	S28	10346	622.5	562	S88	9506	622.5	622	S148	8666	622.5	682	S208	7826	622.5
503	S29	10332	477.5	563	S89	9492	477.5	623	S149	8652	477.5	683	S209	7812	477.5
504	S30	10318	622.5	564	S90	9478	622.5	624	S150	8638	622.5	684	S210	7798	622.5
505	S31	10304	477.5	565	S91	9464	477.5	625	S151	8624	477.5	685	S211	7784	477.5
506	S32	10290	622.5	566	S92	9450	622.5	626	S152	8610	622.5	686	S212	7770	622.5
507	S33	10276	477.5	567	S93	9436	477.5	627	S153	8596	477.5	687	S213	7756	477.5
508	S34	10262	622.5	568	S94	9422	622.5	628	S154	8582	622.5	688	S214	7742	622.5
509	S35	10248	477.5	569	S95	9408	477.5	629	S155	8568	477.5	689	S215	7728	477.5
510	S36	10234	622.5	570	S96	9394	622.5	630	S156	8554	622.5	690	S216	7714	622.5
511	S37	10220	477.5	571	S97	9380	477.5	631	S157	8540	477.5	691	S217	7700	477.5
512	S38	10206	622.5	572	S98	9366	622.5	632	S158	8526	622.5	692	S218	7686	622.5
513	S39	10192	477.5	573	S99	9352	477.5	633	S159	8512	477.5	693	S219	7672	477.5
514	S40	10178	622.5	574	S100	9338	622.5	634	S160	8498	622.5	694	S220	7658	622.5
515	S41	10164	477.5	575	S101	9324	477.5	635	S161	8484	477.5	695	S221	7644	477.5
516	S42	10150	622.5	576	S102	9310	622.5	636	S162	8470	622.5	696	S222	7630	622.5
517	S43	10136	477.5	577	S103	9296	477.5	637	S163	8456	477.5	697	S223	7616	477.5
518	S44	10122	622.5	578	S104	9282	622.5	638	S164	8442	622.5	698	S224	7602	622.5
519	S45	10108	477.5	579	S105	9268	477.5	639	S165	8428	477.5	699	S225	7588	477.5
520	S46	10094	622.5	580	S106	9254	622.5	640	S166	8414	622.5	700	S226	7574	622.5
521	S47	10080	477.5	581	S107	9240	477.5	641	S167	8400	477.5	701	S227	7560	477.5
522	S48	10066	622.5	582	S108	9226	622.5	642	S168	8386	622.5	702	S228	7546	622.5
523	S49	10052	477.5	583	S109	9212	477.5	643	S169	8372	477.5	703	S229	7532	477.5
524	S50	10038	622.5	584	S110	9198	622.5	644	S170	8358	622.5	704	S230	7518	622.5
525	S51	10024	477.5	585	S111	9184	477.5	645	S171	8344	477.5	705	S231	7504	477.5
526	S52	10010	622.5	586	S112	9170	622.5	646	S172	8330	622.5	706	S232	7490	622.5
527	S53	9996	477.5	587	S113	9156	477.5	647	S173	8316	477.5	707	S233	7476	477.5
528	S54	9982	622.5	588	S114	9142	622.5	648	S174	8302	622.5	708	S234	7462	622.5
529	S55	9968	477.5	589	S115	9128	477.5	649	S175	8288	477.5	709	S235	7448	477.5
530	S56	9954	622.5	590	S116	9114	622.5	650	S176	8274	622.5	710	S236	7434	622.5
531	S57	9940	477.5	591	S117	9100	477.5	651	S177	8260	477.5	711	S237	7420	477.5
532	S58	9926	622.5	592	S118	9086	622.5	652	S178	8246	622.5	712	S238	7406	622.5
533	S59	9912	477.5	593	S119	9072	477.5	653	S179	8232	477.5	713	S239	7392	477.5
534	S60	9898	622.5	594	S120	9058	622.5	654	S180	8218	622.5	714	S240	7378	622.5
535	S61	9884	477.5	595	S121	9044	477.5	655	S181	8204	477.5	715	S241	7364	477.5
536	S62	9870	622.5	596	S122	9030	622.5	656	S182	8190	622.5	716	S242	7350	622.5
537	S63	9856	477.5	597	S123	9016	477.5	657	S183	8176	477.5	717	S243	7336	477.5
538	S64	9842	622.5	598	S124	9002	622.5	658	S184	8162	622.5	718	S244	7322	622.5
539	S65	9828	477.5	599	S125	8988	477.5	659	S185	8148	477.5	719	S245	7308	477.5
540	S66	9814	622.5	600	S126	8974	622.5	660	S186	8134	622.5	720	S246	7294	622.5

No.	Text Name	X-axis	Y-axis	No.	Text Name	X-axis	Y-axis	No.	Text Name	X-axis	Y-axis	No.	Text Name	X-axis	Y-axis
721	S247	7280	477.5	781	S307	6440	477.5	841	S367	5600	477.5	901	S427	4760	477.5
722	S248	7266	622.5	782	S308	6426	622.5	842	S368	5586	622.5	902	S428	4746	622.5
723	S249	7252	477.5	783	S309	6412	477.5	843	S369	5572	477.5	903	S429	4732	477.5
724	S250	7238	622.5	784	S310	6398	622.5	844	S370	5558	622.5	904	S430	4718	622.5
725	S251	7224	477.5	785	S311	6384	477.5	845	S371	5544	477.5	905	S431	4704	477.5
726	S252	7210	622.5	786	S312	6370	622.5	846	S372	5530	622.5	906	S432	4690	622.5
727	S253	7196	477.5	787	S313	6356	477.5	847	S373	5516	477.5	907	S433	4676	477.5
728	S254	7182	622.5	788	S314	6342	622.5	848	S374	5502	622.5	908	S434	4662	622.5
729	S255	7168	477.5	789	S315	6328	477.5	849	S375	5488	477.5	909	S435	4648	477.5
730	S256	7154	622.5	790	S316	6314	622.5	850	S376	5474	622.5	910	S436	4634	622.5
731	S257	7140	477.5	791	S317	6300	477.5	851	S377	5460	477.5	911	S437	4620	477.5
732	S258	7126	622.5	792	S318	6286	622.5	852	S378	5446	622.5	912	S438	4606	622.5
733	S259	7112	477.5	793	S319	6272	477.5	853	S379	5432	477.5	913	S439	4592	477.5
734	S260	7098	622.5	794	S320	6258	622.5	854	S380	5418	622.5	914	S440	4578	622.5
735	S261	7084	477.5	795	S321	6244	477.5	855	S381	5404	477.5	915	S441	4564	477.5
736	S262	7070	622.5	796	S322	6230	622.5	856	S382	5390	622.5	916	S442	4550	622.5
737	S263	7056	477.5	797	S323	6216	477.5	857	S383	5376	477.5	917	S443	4536	477.5
738	S264	7042	622.5	798	S324	6202	622.5	858	S384	5362	622.5	918	S444	4522	622.5
739	S265	7028	477.5	799	S325	6188	477.5	859	S385	5348	477.5	919	S445	4508	477.5
740	S266	7014	622.5	800	S326	6174	622.5	860	S386	5334	622.5	920	S446	4494	622.5
741	S267	7000	477.5	801	S327	6160	477.5	861	S387	5320	477.5	921	S447	4480	477.5
742	S268	6986	622.5	802	S328	6146	622.5	862	S388	5306	622.5	922	S448	4466	622.5
743	S269	6972	477.5	803	S329	6132	477.5	863	S389	5292	477.5	923	S449	4452	477.5
744	S270	6958	622.5	804	S330	6118	622.5	864	S390	5278	622.5	924	S450	4438	622.5
745	S271	6944	477.5	805	S331	6104	477.5	865	S391	5264	477.5	925	S451	4424	477.5
746	S272	6930	622.5	806	S332	6090	622.5	866	S392	5250	622.5	926	S452	4410	622.5
747	S273	6916	477.5	807	S333	6076	477.5	867	S393	5236	477.5	927	S453	4396	477.5
748	S274	6902	622.5	808	S334	6062	622.5	868	S394	5222	622.5	928	S454	4382	622.5
749	S275	6888	477.5	809	S335	6048	477.5	869	S395	5208	477.5	929	S455	4368	477.5
750	S276	6874	622.5	810	S336	6034	622.5	870	S396	5194	622.5	930	S456	4354	622.5
751	S277	6860	477.5	811	S337	6020	477.5	871	S397	5180	477.5	931	S457	4340	477.5
752	S278	6846	622.5	812	S338	6006	622.5	872	S398	5166	622.5	932	S458	4326	622.5
753	S279	6832	477.5	813	S339	5992	477.5	873	S399	5152	477.5	933	S459	4312	477.5
754	S280	6818	622.5	814	S340	5978	622.5	874	S400	5138	622.5	934	S460	4298	622.5
755	S281	6804	477.5	815	S341	5964	477.5	875	S401	5124	477.5	935	S461	4284	477.5
756	S282	6790	622.5	816	S342	5950	622.5	876	S402	5110	622.5	936	S462	4270	622.5
757	S283	6776	477.5	817	S343	5936	477.5	877	S403	5096	477.5	937	S463	4256	477.5
758	S284	6762	622.5	818	S344	5922	622.5	878	S404	5082	622.5	938	S464	4242	622.5
759	S285	6748	477.5	819	S345	5908	477.5	879	S405	5068	477.5	939	S465	4228	477.5
760	S286	6734	622.5	820	S346	5894	622.5	880	S406	5054	622.5	940	S466	4214	622.5
761	S287	6720	477.5	821	S347	5880	477.5	881	S407	5040	477.5	941	S467	4200	477.5
762	S288	6706	622.5	822	S348	5866	622.5	882	S408	5026	622.5	942	S468	4186	622.5
763	S289	6692	477.5	823	S349	5852	477.5	883	S409	5012	477.5	943	S469	4172	477.5
764	S290	6678	622.5	824	S350	5838	622.5	884	S410	4998	622.5	944	S470	4158	622.5
765	S291	6664	477.5	825	S351	5824	477.5	885	S411	4984	477.5	945	S471	4144	477.5
766	S292	6650	622.5	826	S352	5810	622.5	886	S412	4970	622.5	946	S472	4130	622.5
767	S293	6636	477.5	827	S353	5796	477.5	887	S413	4956	477.5	947	S473	4116	477.5
768	S294	6622	622.5	828	S354	5782	622.5	888	S414	4942	622.5	948	S474	4102	622.5
769	S295	6608	477.5	829	S355	5768	477.5	889	S415	4928	477.5	949	S475	4088	477.5
770	S296	6594	622.5	830	S356	5754	622.5	890	S416	4914	622.5	950	S476	4074	622.5
771	S297	6580	477.5	831	S357	5740	477.5	891	S417	4900	477.5	951	S477	4060	477.5
772	S298	6566	622.5	832	S358	5726	622.5	892	S418	4886	622.5	952	S478	4046	622.5
773	S299	6552	477.5	833	S359	5712	477.5	893	S419	4872	477.5	953	S479	4032	477.5
774	S300	6538	622.5	834	S360	5698	622.5	894	S420	4858	622.5	954	S480	4018	622.5
775	S301	6524	477.5	835	S361	5684	477.5	895	S421	4844	477.5	955	S481	4004	477.5
776	S302	6510	622.5	836	S362	5670	622.5	896	S422	4830	622.5	956	S482	3990	622.5
777	S303	6496	477.5	837	S363	5656	477.5	897	S423	4816	477.5	957	S483	3976	477.5
778	S304	6482	622.5	838	S364	5642	622.5	898	S424	4802	622.5	958	S484	3962	622.5
779	S305	6468	477.5	839	S365	5628	477.5	899	S425	4788	477.5	959	S485	3948	477.5
780	S306	6454	622.5	840	S366	5614	622.5	900	S426	4774	622.5	960	S486	3934	622.5

No.	Text Name	X-axis	Y-axis	No.	Text Name	X-axis	Y-axis	No.	Text Name	X-axis	Y-axis	No.	Text Name	X-axis	Y-axis
961	S487	3920	477.5	1021	S547	3080	477.5	1081	S607	2240	477.5	1141	S667	1400	477.5
962	S488	3906	622.5	1022	S548	3066	622.5	1082	S608	2226	622.5	1142	S668	1386	622.5
963	S489	3892	477.5	1023	S549	3052	477.5	1083	S609	2212	477.5	1143	S669	1372	477.5
964	S490	3878	622.5	1024	S550	3038	622.5	1084	S610	2198	622.5	1144	S670	1358	622.5
965	S491	3864	477.5	1025	S551	3024	477.5	1085	S611	2184	477.5	1145	S671	1344	477.5
966	S492	3850	622.5	1026	S552	3010	622.5	1086	S612	2170	622.5	1146	S672	1330	622.5
967	S493	3836	477.5	1027	S553	2996	477.5	1087	S613	2156	477.5	1147	S673	1316	477.5
968	S494	3822	622.5	1028	S554	2982	622.5	1088	S614	2142	622.5	1148	S674	1302	622.5
969	S495	3808	477.5	1029	S555	2968	477.5	1089	S615	2128	477.5	1149	S675	1288	477.5
970	S496	3794	622.5	1030	S556	2954	622.5	1090	S616	2114	622.5	1150	S676	1274	622.5
971	S497	3780	477.5	1031	S557	2940	477.5	1091	S617	2100	477.5	1151	S677	1260	477.5
972	S498	3766	622.5	1032	S558	2926	622.5	1092	S618	2086	622.5	1152	S678	1246	622.5
973	S499	3752	477.5	1033	S559	2912	477.5	1093	S619	2072	477.5	1153	S679	1232	477.5
974	S500	3738	622.5	1034	S560	2898	622.5	1094	S620	2058	622.5	1154	S680	1218	622.5
975	S501	3724	477.5	1035	S561	2884	477.5	1095	S621	2044	477.5	1155	S681	1204	477.5
976	S502	3710	622.5	1036	S562	2870	622.5	1096	S622	2030	622.5	1156	S682	1190	622.5
977	S503	3696	477.5	1037	S563	2856	477.5	1097	S623	2016	477.5	1157	S683	1176	477.5
978	S504	3682	622.5	1038	S564	2842	622.5	1098	S624	2002	622.5	1158	S684	1162	622.5
979	S505	3668	477.5	1039	S565	2828	477.5	1099	S625	1988	477.5	1159	S685	1148	477.5
980	S506	3654	622.5	1040	S566	2814	622.5	1100	S626	1974	622.5	1160	S686	1134	622.5
981	S507	3640	477.5	1041	S567	2800	477.5	1101	S627	1960	477.5	1161	S687	1120	477.5
982	S508	3626	622.5	1042	S568	2786	622.5	1102	S628	1946	622.5	1162	S688	1106	622.5
983	S509	3612	477.5	1043	S569	2772	477.5	1103	S629	1932	477.5	1163	S689	1092	477.5
984	S510	3598	622.5	1044	S570	2758	622.5	1104	S630	1918	622.5	1164	S690	1078	622.5
985	S511	3584	477.5	1045	S571	2744	477.5	1105	S631	1904	477.5	1165	S691	1064	477.5
986	S512	3570	622.5	1046	S572	2730	622.5	1106	S632	1890	622.5	1166	S692	1050	622.5
987	S513	3556	477.5	1047	S573	2716	477.5	1107	S633	1876	477.5	1167	S693	1036	477.5
988	S514	3542	622.5	1048	S574	2702	622.5	1108	S634	1862	622.5	1168	S694	1022	622.5
989	S515	3528	477.5	1049	S575	2688	477.5	1109	S635	1848	477.5	1169	S695	1008	477.5
990	S516	3514	622.5	1050	S576	2674	622.5	1110	S636	1834	622.5	1170	S696	994	622.5
991	S517	3500	477.5	1051	S577	2660	477.5	1111	S637	1820	477.5	1171	S697	980	477.5
992	S518	3486	622.5	1052	S578	2646	622.5	1112	S638	1806	622.5	1172	S698	966	622.5
993	S519	3472	477.5	1053	S579	2632	477.5	1113	S639	1792	477.5	1173	S699	952	477.5
994	S520	3458	622.5	1054	S580	2618	622.5	1114	S640	1778	622.5	1174	S700	938	622.5
995	S521	3444	477.5	1055	S581	2604	477.5	1115	S641	1764	477.5	1175	S701	924	477.5
996	S522	3430	622.5	1056	S582	2590	622.5	1116	S642	1750	622.5	1176	S702	910	622.5
997	S523	3416	477.5	1057	S583	2576	477.5	1117	S643	1736	477.5	1177	S703	896	477.5
998	S524	3402	622.5	1058	S584	2562	622.5	1118	S644	1722	622.5	1178	S704	882	622.5
999	S525	3388	477.5	1059	S585	2548	477.5	1119	S645	1708	477.5	1179	S705	868	477.5
1000	S526	3374	622.5	1060	S586	2534	622.5	1120	S646	1694	622.5	1180	S706	854	622.5
1001	S527	3360	477.5	1061	S587	2520	477.5	1121	S647	1680	477.5	1181	S707	840	477.5
1002	S528	3346	622.5	1062	S588	2506	622.5	1122	S648	1666	622.5	1182	S708	826	622.5
1003	S529	3332	477.5	1063	S589	2492	477.5	1123	S649	1652	477.5	1183	S709	812	477.5
1004	S530	3318	622.5	1064	S590	2478	622.5	1124	S650	1638	622.5	1184	S710	798	622.5
1005	S531	3304	477.5	1065	S591	2464	477.5	1125	S651	1624	477.5	1185	S711	784	477.5
1006	S532	3290	622.5	1066	S592	2450	622.5	1126	S652	1610	622.5	1186	S712	770	622.5
1007	S533	3276	477.5	1067	S593	2436	477.5	1127	S653	1596	477.5	1187	S713	756	477.5
1008	S534	3262	622.5	1068	S594	2422	622.5	1128	S654	1582	622.5	1188	S714	742	622.5
1009	S535	3248	477.5	1069	S595	2408	477.5	1129	S655	1568	477.5	1189	S715	728	477.5
1010	S536	3234	622.5	1070	S596	2394	622.5	1130	S656	1554	622.5	1190	S716	714	622.5
1011	S537	3220	477.5	1071	S597	2380	477.5	1131	S657	1540	477.5	1191	S717	700	477.5
1012	S538	3206	622.5	1072	S598	2366	622.5	1132	S658	1526	622.5	1192	S718	686	622.5
1013	S539	3192	477.5	1073	S599	2352	477.5	1133	S659	1512	477.5	1193	S719	672	477.5
1014	S540	3178	622.5	1074	S600	2338	622.5	1134	S660	1498	622.5	1194	S720	658	622.5
1015	S541	3164	477.5	1075	S601	2324	477.5	1135	S661	1484	477.5	1195	VSSIDUM9	644	477.5
1016	S542	3150	622.5	1076	S602	2310	622.5	1136	S662	1470	622.5	1196	VSSIDUM10	630	622.5
1017	S543	3136	477.5	1077	S603	2296	477.5	1137	S663	1456	477.5	1197	VSSIDUM11	616	477.5
1018	S544	3122	622.5	1078	S604	2282	622.5	1138	S664	1442	622.5	1198	VSSIDUM12	602	622.5
1019	S545	3108	477.5	1079	S605	2268	477.5	1139	S665	1428	477.5	1199	VSSIDUM13	588	477.5
1020	S546	3094	622.5	1080	S606	2254	622.5	1140	S666	1414	622.5	1200	VSSIDUM14	574	622.5

No.	Text Name	X-axis	Y-axis	No.	Text Name	X-axis	Y-axis	No.	Text Name	X-axis	Y-axis	No.	Text Name	X-axis	Y-axis
1201	VSSIDUM16	546	622.5	1261	S742	-336	477.5	1321	S802	-1176	477.5	1381	S862	-2016	477.5
1202	VSSIDUM20	490	622.5	1262	S743	-350	622.5	1322	S803	-1190	622.5	1382	S863	-2030	622.5
1203	VSSIDUM21	476	477.5	1263	S744	-364	477.5	1323	S804	-1204	477.5	1383	S864	-2044	477.5
1204	VSSIDUM22	462	622.5	1264	S745	-378	622.5	1324	S805	-1218	622.5	1384	S865	-2058	622.5
1205	VSSIDUM23	448	477.5	1265	S746	-392	477.5	1325	S806	-1232	477.5	1385	S866	-2072	477.5
1206	VSSIDUM24	434	622.5	1266	S747	-406	622.5	1326	S807	-1246	622.5	1386	S867	-2086	622.5
1207	VSSIDUM25	420	477.5	1267	S748	-420	477.5	1327	S808	-1260	477.5	1387	S868	-2100	477.5
1208	VSSIDUM26	406	622.5	1268	S749	-434	622.5	1328	S809	-1274	622.5	1388	S869	-2114	622.5
1209	VSSIDUM27	392	477.5	1269	S750	-448	477.5	1329	S810	-1288	477.5	1389	S870	-2128	477.5
1210	VSSIDUM28	378	622.5	1270	S751	-462	622.5	1330	S811	-1302	622.5	1390	S871	-2142	622.5
1211	VSSIDUM29	364	477.5	1271	S752	-476	477.5	1331	S812	-1316	477.5	1391	S872	-2156	477.5
1212	VSSIDUM30	350	622.5	1272	S753	-490	622.5	1332	S813	-1330	622.5	1392	S873	-2170	622.5
1213	VSSIDUM31	336	477.5	1273	S754	-504	477.5	1333	S814	-1344	477.5	1393	S874	-2184	477.5
1214	VSSIDUM32	322	622.5	1274	S755	-518	622.5	1334	S815	-1358	622.5	1394	S875	-2198	622.5
1215	VSSIDUM33	308	477.5	1275	S756	-532	477.5	1335	S816	-1372	477.5	1395	S876	-2212	477.5
1216	VSSIDUM34	294	622.5	1276	S757	-546	622.5	1336	S817	-1386	622.5	1396	S877	-2226	622.5
1217	VSSIDUM35	280	477.5	1277	S758	-560	477.5	1337	S818	-1400	477.5	1397	S878	-2240	477.5
1218	VSSIDUM36	266	622.5	1278	S759	-574	622.5	1338	S819	-1414	622.5	1398	S879	-2254	622.5
1219	VSSIDUM37	252	477.5	1279	S760	-588	477.5	1339	S820	-1428	477.5	1399	S880	-2268	477.5
1220	VSSIDUM38	238	622.5	1280	S761	-602	622.5	1340	S821	-1442	622.5	1400	S881	-2282	622.5
1221	VSSIDUM39	224	477.5	1281	S762	-616	477.5	1341	S822	-1456	477.5	1401	S882	-2296	477.5
1222	VSSIDUM40	210	622.5	1282	S763	-630	622.5	1342	S823	-1470	622.5	1402	S883	-2310	622.5
1223	VSSIDUM41	196	477.5	1283	S764	-644	477.5	1343	S824	-1484	477.5	1403	S884	-2324	477.5
1224	VSSIDUM42	182	622.5	1284	S765	-658	622.5	1344	S825	-1498	622.5	1404	S885	-2338	622.5
1225	VSSIDUM43	168	477.5	1285	S766	-672	477.5	1345	S826	-1512	477.5	1405	S886	-2352	477.5
1226	VSSIDUM44	154	622.5	1286	S767	-686	622.5	1346	S827	-1526	622.5	1406	S887	-2366	622.5
1227	VSSIDUM45	140	477.5	1287	S768	-700	477.5	1347	S828	-1540	477.5	1407	S888	-2380	477.5
1228	VSSIDUM46	126	622.5	1288	S769	-714	622.5	1348	S829	-1554	622.5	1408	S889	-2394	622.5
1229	VSSIDUM47	112	477.5	1289	S770	-728	477.5	1349	S830	-1568	477.5	1409	S890	-2408	477.5
1230	VSSIDUM48	98	622.5	1290	S771	-742	622.5	1350	S831	-1582	622.5	1410	S891	-2422	622.5
1231	VSSIDUM49	84	477.5	1291	S772	-756	477.5	1351	S832	-1596	477.5	1411	S892	-2436	477.5
1232	VSSIDUM50	70	622.5	1292	S773	-770	622.5	1352	S833	-1610	622.5	1412	S893	-2450	622.5
1233	VSSIDUM51	56	477.5	1293	S774	-784	477.5	1353	S834	-1624	477.5	1413	S894	-2464	477.5
1234	VSSIDUM52	42	622.5	1294	S775	-798	622.5	1354	S835	-1638	622.5	1414	S895	-2478	622.5
1235	VSSIDUM53	28	477.5	1295	S776	-812	477.5	1355	S836	-1652	477.5	1415	S896	-2492	477.5
1236	VSSIDUM54	14	622.5	1296	S777	-826	622.5	1356	S837	-1666	622.5	1416	S897	-2506	622.5
1237	VSSIDUM55	0	477.5	1297	S778	-840	477.5	1357	S838	-1680	477.5	1417	S898	-2520	477.5
1238	VSSIDUM56	-14	622.5	1298	S779	-854	622.5	1358	S839	-1694	622.5	1418	S899	-2534	622.5
1239	VSSIDUM57	-28	477.5	1299	S780	-868	477.5	1359	S840	-1708	477.5	1419	S900	-2548	477.5
1240	S721	-42	622.5	1300	S781	-882	622.5	1360	S841	-1722	622.5	1420	S901	-2562	622.5
1241	S722	-56	477.5	1301	S782	-896	477.5	1361	S842	-1736	477.5	1421	S902	-2576	477.5
1242	S723	-70	622.5	1302	S783	-910	622.5	1362	S843	-1750	622.5	1422	S903	-2590	622.5
1243	S724	-84	477.5	1303	S784	-924	477.5	1363	S844	-1764	477.5	1423	S904	-2604	477.5
1244	S725	-98	622.5	1304	S785	-938	622.5	1364	S845	-1778	622.5	1424	S905	-2618	622.5
1245	S726	-112	477.5	1305	S786	-952	477.5	1365	S846	-1792	477.5	1425	S906	-2632	477.5
1246	S727	-126	622.5	1306	S787	-966	622.5	1366	S847	-1806	622.5	1426	S907	-2646	622.5
1247	S728	-140	477.5	1307	S788	-980	477.5	1367	S848	-1820	477.5	1427	S908	-2660	477.5
1248	S729	-154	622.5	1308	S789	-994	622.5	1368	S849	-1834	622.5	1428	S909	-2674	622.5
1249	S730	-168	477.5	1309	S790	-1008	477.5	1369	S850	-1848	477.5	1429	S910	-2688	477.5
1250	S731	-182	622.5	1310	S791	-1022	622.5	1370	S851	-1862	622.5	1430	S911	-2702	622.5
1251	S732	-196	477.5	1311	S792	-1036	477.5	1371	S852	-1876	477.5	1431	S912	-2716	477.5
1252	S733	-210	622.5	1312	S793	-1050	622.5	1372	S853	-1890	622.5	1432	S913	-2730	622.5
1253	S734	-224	477.5	1313	S794	-1064	477.5	1373	S854	-1904	477.5	1433	S914	-2744	477.5
1254	S735	-238	622.5	1314	S795	-1078	622.5	1374	S855	-1918	622.5	1434	S915	-2758	622.5
1255	S736	-252	477.5	1315	S796	-1092	477.5	1375	S856	-1932	477.5	1435	S916	-2772	477.5
1256	S737	-266	622.5	1316	S797	-1106	622.5	1376	S857	-1946	622.5	1436	S917	-2786	622.5
1257	S738	-280	477.5	1317	S798	-1120	477.5	1377	S858	-1960	477.5	1437	S918	-2800	477.5
1258	S739	-294	622.5	1318	S799	-1134	622.5	1378	S859	-1974	622.5	1438	S919	-2814	622.5
1259	S740	-308	477.5	1319	S800	-1148	477.5	1379	S860	-1988	477.5	1439	S920	-2828	477.5
1260	S741	-322	622.5	1320	S801	-1162	622.5	1380	S861	-2002	622.5	1440	S921	-2842	622.5

No.	Text Name	X-axis	Y-axis	No.	Text Name	X-axis	Y-axis	No.	Text Name	X-axis	Y-axis	No.	Text Name	X-axis	Y-axis
1441	S922	-2856	477.5	1501	S982	-3696	477.5	1561	S1042	-4536	477.5	1621	S1102	-5376	477.5
1442	S923	-2870	622.5	1502	S983	-3710	622.5	1562	S1043	-4550	622.5	1622	S1103	-5390	622.5
1443	S924	-2884	477.5	1503	S984	-3724	477.5	1563	S1044	-4564	477.5	1623	S1104	-5404	477.5
1444	S925	-2898	622.5	1504	S985	-3738	622.5	1564	S1045	-4578	622.5	1624	S1105	-5418	622.5
1445	S926	-2912	477.5	1505	S986	-3752	477.5	1565	S1046	-4592	477.5	1625	S1106	-5432	477.5
1446	S927	-2926	622.5	1506	S987	-3766	622.5	1566	S1047	-4606	622.5	1626	S1107	-5446	622.5
1447	S928	-2940	477.5	1507	S988	-3780	477.5	1567	S1048	-4620	477.5	1627	S1108	-5460	477.5
1448	S929	-2954	622.5	1508	S989	-3794	622.5	1568	S1049	-4634	622.5	1628	S1109	-5474	622.5
1449	S930	-2968	477.5	1509	S990	-3808	477.5	1569	S1050	-4648	477.5	1629	S1110	-5488	477.5
1450	S931	-2982	622.5	1510	S991	-3822	622.5	1570	S1051	-4662	622.5	1630	S1111	-5502	622.5
1451	S932	-2996	477.5	1511	S992	-3836	477.5	1571	S1052	-4676	477.5	1631	S1112	-5516	477.5
1452	S933	-3010	622.5	1512	S993	-3850	622.5	1572	S1053	-4690	622.5	1632	S1113	-5530	622.5
1453	S934	-3024	477.5	1513	S994	-3864	477.5	1573	S1054	-4704	477.5	1633	S1114	-5544	477.5
1454	S935	-3038	622.5	1514	S995	-3878	622.5	1574	S1055	-4718	622.5	1634	S1115	-5558	622.5
1455	S936	-3052	477.5	1515	S996	-3892	477.5	1575	S1056	-4732	477.5	1635	S1116	-5572	477.5
1456	S937	-3066	622.5	1516	S997	-3906	622.5	1576	S1057	-4746	622.5	1636	S1117	-5586	622.5
1457	S938	-3080	477.5	1517	S998	-3920	477.5	1577	S1058	-4760	477.5	1637	S1118	-5600	477.5
1458	S939	-3094	622.5	1518	S999	-3934	622.5	1578	S1059	-4774	622.5	1638	S1119	-5614	622.5
1459	S940	-3108	477.5	1519	S1000	-3948	477.5	1579	S1060	-4788	477.5	1639	S1120	-5628	477.5
1460	S941	-3122	622.5	1520	S1001	-3962	622.5	1580	S1061	-4802	622.5	1640	S1121	-5642	622.5
1461	S942	-3136	477.5	1521	S1002	-3976	477.5	1581	S1062	-4816	477.5	1641	S1122	-5656	477.5
1462	S943	-3150	622.5	1522	S1003	-3990	622.5	1582	S1063	-4830	622.5	1642	S1123	-5670	622.5
1463	S944	-3164	477.5	1523	S1004	-4004	477.5	1583	S1064	-4844	477.5	1643	S1124	-5684	477.5
1464	S945	-3178	622.5	1524	S1005	-4018	622.5	1584	S1065	-4858	622.5	1644	S1125	-5698	622.5
1465	S946	-3192	477.5	1525	S1006	-4032	477.5	1585	S1066	-4872	477.5	1645	S1126	-5712	477.5
1466	S947	-3206	622.5	1526	S1007	-4046	622.5	1586	S1067	-4886	622.5	1646	S1127	-5726	622.5
1467	S948	-3220	477.5	1527	S1008	-4060	477.5	1587	S1068	-4900	477.5	1647	S1128	-5740	477.5
1468	S949	-3234	622.5	1528	S1009	-4074	622.5	1588	S1069	-4914	622.5	1648	S1129	-5754	622.5
1469	S950	-3248	477.5	1529	S1010	-4088	477.5	1589	S1070	-4928	477.5	1649	S1130	-5768	477.5
1470	S951	-3262	622.5	1530	S1011	-4102	622.5	1590	S1071	-4942	622.5	1650	S1131	-5782	622.5
1471	S952	-3276	477.5	1531	S1012	-4116	477.5	1591	S1072	-4956	477.5	1651	S1132	-5796	477.5
1472	S953	-3290	622.5	1532	S1013	-4130	622.5	1592	S1073	-4970	622.5	1652	S1133	-5810	622.5
1473	S954	-3304	477.5	1533	S1014	-4144	477.5	1593	S1074	-4984	477.5	1653	S1134	-5824	477.5
1474	S955	-3318	622.5	1534	S1015	-4158	622.5	1594	S1075	-4998	622.5	1654	S1135	-5838	622.5
1475	S956	-3332	477.5	1535	S1016	-4172	477.5	1595	S1076	-5012	477.5	1655	S1136	-5852	477.5
1476	S957	-3346	622.5	1536	S1017	-4186	622.5	1596	S1077	-5026	622.5	1656	S1137	-5866	622.5
1477	S958	-3360	477.5	1537	S1018	-4200	477.5	1597	S1078	-5040	477.5	1657	S1138	-5880	477.5
1478	S959	-3374	622.5	1538	S1019	-4214	622.5	1598	S1079	-5054	622.5	1658	S1139	-5894	622.5
1479	S960	-3388	477.5	1539	S1020	-4228	477.5	1599	S1080	-5068	477.5	1659	S1140	-5908	477.5
1480	S961	-3402	622.5	1540	S1021	-4242	622.5	1600	S1081	-5082	622.5	1660	S1141	-5922	622.5
1481	S962	-3416	477.5	1541	S1022	-4256	477.5	1601	S1082	-5096	477.5	1661	S1142	-5936	477.5
1482	S963	-3430	622.5	1542	S1023	-4270	622.5	1602	S1083	-5110	622.5	1662	S1143	-5950	622.5
1483	S964	-3444	477.5	1543	S1024	-4284	477.5	1603	S1084	-5124	477.5	1663	S1144	-5964	477.5
1484	S965	-3458	622.5	1544	S1025	-4298	622.5	1604	S1085	-5138	622.5	1664	S1145	-5978	622.5
1485	S966	-3472	477.5	1545	S1026	-4312	477.5	1605	S1086	-5152	477.5	1665	S1146	-5992	477.5
1486	S967	-3486	622.5	1546	S1027	-4326	622.5	1606	S1087	-5166	622.5	1666	S1147	-6006	622.5
1487	S968	-3500	477.5	1547	S1028	-4340	477.5	1607	S1088	-5180	477.5	1667	S1148	-6020	477.5
1488	S969	-3514	622.5	1548	S1029	-4354	622.5	1608	S1089	-5194	622.5	1668	S1149	-6034	622.5
1489	S970	-3528	477.5	1549	S1030	-4368	477.5	1609	S1090	-5208	477.5	1669	S1150	-6048	477.5
1490	S971	-3542	622.5	1550	S1031	-4382	622.5	1610	S1091	-5222	622.5	1670	S1151	-6062	622.5
1491	S972	-3556	477.5	1551	S1032	-4396	477.5	1611	S1092	-5236	477.5	1671	S1152	-6076	477.5
1492	S973	-3570	622.5	1552	S1033	-4410	622.5	1612	S1093	-5250	622.5	1672	S1153	-6090	622.5
1493	S974	-3584	477.5	1553	S1034	-4424	477.5	1613	S1094	-5264	477.5	1673	S1154	-6104	477.5
1494	S975	-3598	622.5	1554	S1035	-4438	622.5	1614	S1095	-5278	622.5	1674	S1155	-6118	622.5
1495	S976	-3612	477.5	1555	S1036	-4452	477.5	1615	S1096	-5292	477.5	1675	S1156	-6132	477.5
1496	S977	-3626	622.5	1556	S1037	-4466	622.5	1616	S1097	-5306	622.5	1676	S1157	-6146	622.5
1497	S978	-3640	477.5	1557	S1038	-4480	477.5	1617	S1098	-5320	477.5	1677	S1158	-6160	477.5
1498	S979	-3654	622.5	1558	S1039	-4494	622.5	1618	S1099	-5334	622.5	1678	S1159	-6174	622.5
1499	S980	-3668	477.5	1559	S1040	-4508	477.5	1619	S1100	-5348	477.5	1679	S1160	-6188	477.5
1500	S981	-3682	622.5	1560	S1041	-4522	622.5	1620	S1101	-5362	622.5	1680	S1161	-6202	622.5

No.	Text Name	X-axis	Y-axis	No.	Text Name	X-axis	Y-axis	No.	Text Name	X-axis	Y-axis	No.	Text Name	X-axis	Y-axis
1681	S1162	-6216	477.5	1741	S1222	-7056	477.5	1801	S1282	-7896	477.5	1861	S1342	-8736	477.5
1682	S1163	-6230	622.5	1742	S1223	-7070	622.5	1802	S1283	-7910	622.5	1862	S1343	-8750	622.5
1683	S1164	-6244	477.5	1743	S1224	-7084	477.5	1803	S1284	-7924	477.5	1863	S1344	-8764	477.5
1684	S1165	-6258	622.5	1744	S1225	-7098	622.5	1804	S1285	-7938	622.5	1864	S1345	-8778	622.5
1685	S1166	-6272	477.5	1745	S1226	-7112	477.5	1805	S1286	-7952	477.5	1865	S1346	-8792	477.5
1686	S1167	-6286	622.5	1746	S1227	-7126	622.5	1806	S1287	-7966	622.5	1866	S1347	-8806	622.5
1687	S1168	-6300	477.5	1747	S1228	-7140	477.5	1807	S1288	-7980	477.5	1867	S1348	-8820	477.5
1688	S1169	-6314	622.5	1748	S1229	-7154	622.5	1808	S1289	-7994	622.5	1868	S1349	-8834	622.5
1689	S1170	-6328	477.5	1749	S1230	-7168	477.5	1809	S1290	-8008	477.5	1869	S1350	-8848	477.5
1690	S1171	-6342	622.5	1750	S1231	-7182	622.5	1810	S1291	-8022	622.5	1870	S1351	-8862	622.5
1691	S1172	-6356	477.5	1751	S1232	-7196	477.5	1811	S1292	-8036	477.5	1871	S1352	-8876	477.5
1692	S1173	-6370	622.5	1752	S1233	-7210	622.5	1812	S1293	-8050	622.5	1872	S1353	-8890	622.5
1693	S1174	-6384	477.5	1753	S1234	-7224	477.5	1813	S1294	-8064	477.5	1873	S1354	-8904	477.5
1694	S1175	-6398	622.5	1754	S1235	-7238	622.5	1814	S1295	-8078	622.5	1874	S1355	-8918	622.5
1695	S1176	-6412	477.5	1755	S1236	-7252	477.5	1815	S1296	-8092	477.5	1875	S1356	-8932	477.5
1696	S1177	-6426	622.5	1756	S1237	-7266	622.5	1816	S1297	-8106	622.5	1876	S1357	-8946	622.5
1697	S1178	-6440	477.5	1757	S1238	-7280	477.5	1817	S1298	-8120	477.5	1877	S1358	-8960	477.5
1698	S1179	-6454	622.5	1758	S1239	-7294	622.5	1818	S1299	-8134	622.5	1878	S1359	-8974	622.5
1699	S1180	-6468	477.5	1759	S1240	-7308	477.5	1819	S1300	-8148	477.5	1879	S1360	-8988	477.5
1700	S1181	-6482	622.5	1760	S1241	-7322	622.5	1820	S1301	-8162	622.5	1880	S1361	-9002	622.5
1701	S1182	-6496	477.5	1761	S1242	-7336	477.5	1821	S1302	-8176	477.5	1881	S1362	-9016	477.5
1702	S1183	-6510	622.5	1762	S1243	-7350	622.5	1822	S1303	-8190	622.5	1882	S1363	-9030	622.5
1703	S1184	-6524	477.5	1763	S1244	-7364	477.5	1823	S1304	-8204	477.5	1883	S1364	-9044	477.5
1704	S1185	-6538	622.5	1764	S1245	-7378	622.5	1824	S1305	-8218	622.5	1884	S1365	-9058	622.5
1705	S1186	-6552	477.5	1765	S1246	-7392	477.5	1825	S1306	-8232	477.5	1885	S1366	-9072	477.5
1706	S1187	-6566	622.5	1766	S1247	-7406	622.5	1826	S1307	-8246	622.5	1886	S1367	-9086	622.5
1707	S1188	-6580	477.5	1767	S1248	-7420	477.5	1827	S1308	-8260	477.5	1887	S1368	-9100	477.5
1708	S1189	-6594	622.5	1768	S1249	-7434	622.5	1828	S1309	-8274	622.5	1888	S1369	-9114	622.5
1709	S1190	-6608	477.5	1769	S1250	-7448	477.5	1829	S1310	-8288	477.5	1889	S1370	-9128	477.5
1710	S1191	-6622	622.5	1770	S1251	-7462	622.5	1830	S1311	-8302	622.5	1890	S1371	-9142	622.5
1711	S1192	-6636	477.5	1771	S1252	-7476	477.5	1831	S1312	-8316	477.5	1891	S1372	-9156	477.5
1712	S1193	-6650	622.5	1772	S1253	-7490	622.5	1832	S1313	-8330	622.5	1892	S1373	-9170	622.5
1713	S1194	-6664	477.5	1773	S1254	-7504	477.5	1833	S1314	-8344	477.5	1893	S1374	-9184	477.5
1714	S1195	-6678	622.5	1774	S1255	-7518	622.5	1834	S1315	-8358	622.5	1894	S1375	-9198	622.5
1715	S1196	-6692	477.5	1775	S1256	-7532	477.5	1835	S1316	-8372	477.5	1895	S1376	-9212	477.5
1716	S1197	-6706	622.5	1776	S1257	-7546	622.5	1836	S1317	-8386	622.5	1896	S1377	-9226	622.5
1717	S1198	-6720	477.5	1777	S1258	-7560	477.5	1837	S1318	-8400	477.5	1897	S1378	-9240	477.5
1718	S1199	-6734	622.5	1778	S1259	-7574	622.5	1838	S1319	-8414	622.5	1898	S1379	-9254	622.5
1719	S1200	-6748	477.5	1779	S1260	-7588	477.5	1839	S1320	-8428	477.5	1899	S1380	-9268	477.5
1720	S1201	-6762	622.5	1780	S1261	-7602	622.5	1840	S1321	-8442	622.5	1900	S1381	-9282	622.5
1721	S1202	-6776	477.5	1781	S1262	-7616	477.5	1841	S1322	-8456	477.5	1901	S1382	-9296	477.5
1722	S1203	-6790	622.5	1782	S1263	-7630	622.5	1842	S1323	-8470	622.5	1902	S1383	-9310	622.5
1723	S1204	-6804	477.5	1783	S1264	-7644	477.5	1843	S1324	-8484	477.5	1903	S1384	-9324	477.5
1724	S1205	-6818	622.5	1784	S1265	-7658	622.5	1844	S1325	-8498	622.5	1904	S1385	-9338	622.5
1725	S1206	-6832	477.5	1785	S1266	-7672	477.5	1845	S1326	-8512	477.5	1905	S1386	-9352	477.5
1726	S1207	-6846	622.5	1786	S1267	-7686	622.5	1846	S1327	-8526	622.5	1906	S1387	-9366	622.5
1727	S1208	-6860	477.5	1787	S1268	-7700	477.5	1847	S1328	-8540	477.5	1907	S1388	-9380	477.5
1728	S1209	-6874	622.5	1788	S1269	-7714	622.5	1848	S1329	-8554	622.5	1908	S1389	-9394	622.5
1729	S1210	-6888	477.5	1789	S1270	-7728	477.5	1849	S1330	-8568	477.5	1909	S1390	-9408	477.5
1730	S1211	-6902	622.5	1790	S1271	-7742	622.5	1850	S1331	-8582	622.5	1910	S1391	-9422	622.5
1731	S1212	-6916	477.5	1791	S1272	-7756	477.5	1851	S1332	-8596	477.5	1911	S1392	-9436	477.5
1732	S1213	-6930	622.5	1792	S1273	-7770	622.5	1852	S1333	-8610	622.5	1912	S1393	-9450	622.5
1733	S1214	-6944	477.5	1793	S1274	-7784	477.5	1853	S1334	-8624	477.5	1913	S1394	-9464	477.5
1734	S1215	-6958	622.5	1794	S1275	-7798	622.5	1854	S1335	-8638	622.5	1914	S1395	-9478	622.5
1735	S1216	-6972	477.5	1795	S1276	-7812	477.5	1855	S1336	-8652	477.5	1915	S1396	-9492	477.5
1736	S1217	-6986	622.5	1796	S1277	-7826	622.5	1856	S1337	-8666	622.5	1916	S1397	-9506	622.5
1737	S1218	-7000	477.5	1797	S1278	-7840	477.5	1857	S1338	-8680	477.5	1917	S1398	-9520	477.5
1738	S1219	-7014	622.5	1798	S1279	-7854	622.5	1858	S1339	-8694	622.5	1918	S1399	-9534	622.5
1739	S1220	-7028	477.5	1799	S1280	-7868	477.5	1859	S1340	-8708	477.5	1919	S1400	-9548	477.5
1740	S1221	-7042	622.5	1800	S1281	-7882	622.5	1860	S1341	-8722	622.5	1920	S1401	-9562	622.5

No.	Text Name	X-axis	Y-axis
1921	S1402	-9576	477.5
1922	S1403	-9590	622.5
1923	S1404	-9604	477.5
1924	S1405	-9618	622.5
1925	S1406	-9632	477.5
1926	S1407	-9646	622.5
1927	S1408	-9660	477.5
1928	S1409	-9674	622.5
1929	S1410	-9688	477.5
1930	S1411	-9702	622.5
1931	S1412	-9716	477.5
1932	S1413	-9730	622.5
1933	S1414	-9744	477.5
1934	S1415	-9758	622.5
1935	S1416	-9772	477.5
1936	S1417	-9786	622.5
1937	S1418	-9800	477.5
1938	S1419	-9814	622.5
1939	S1420	-9828	477.5
1940	S1421	-9842	622.5
1941	S1422	-9856	477.5
1942	S1423	-9870	622.5
1943	S1424	-9884	477.5
1944	S1425	-9898	622.5
1945	S1426	-9912	477.5
1946	S1427	-9926	622.5
1947	S1428	-9940	477.5
1948	S1429	-9954	622.5
1949	S1430	-9968	477.5
1950	S1431	-9982	622.5
1951	S1432	-9996	477.5
1952	S1433	-10010	622.5
1953	S1434	-10024	477.5
1954	S1435	-10038	622.5
1955	S1436	-10052	477.5
1956	S1437	-10066	622.5
1957	S1438	-10080	477.5
1958	S1439	-10094	622.5
1959	S1440	-10108	477.5
1960	SDUM2	-10122	622.5
1961	SDUM3	-10136	477.5
1962	VSSIDUM58	-10150	622.5
1963	VSSIDUM59	-10164	477.5
1964	VGLO_L	-10178	622.5
1965	VGLO_L	-10192	477.5
1966	VGLO_L	-10206	622.5
1967	VGLO_L	-10220	477.5
1968	VGLO_L	-10234	622.5
1969	VGLO_L	-10248	477.5
1970	VGLO_L	-10262	622.5
1971	VGLO_L	-10276	477.5
1972	VGLO_L	-10290	622.5
1973	VGH	-10304	477.5
1974	VGH	-10318	622.5
1975	VGH	-10332	477.5
1976	VGH	-10346	622.5
1977	VGH	-10360	477.5
1978	VGH	-10374	622.5
1979	VGH	-10388	477.5
1980	VGH	-10402	622.5

No.	Text Name	X-axis	Y-axis
1981	VSSIDUM60	-10416	477.5
1982	VSSIDUM61	-10430	622.5
1983	VSSIDUM62	-10444	477.5
1984	VSSIDUM63	-10458	622.5
1985	VSSIDUM64	-10472	477.5
1986	VSSIDUM65	-10486	622.5
1987	VSSIDUM66	-10500	477.5
1988	VSSIDUM67	-10514	622.5
1989	VSSIDUM68	-10528	477.5
1990	VSSIDUM69	-10542	622.5
1991	VSSIDUM70	-10556	477.5
1992	VSSIDUM71	-10570	622.5
1993	VSSIDUM72	-10584	477.5
1994	VSSIDUM73	-10598	622.5
1995	VSSIDUM74	-10612	477.5
1996	VSSIDUM75	-10626	622.5
1997	VSSIDUM76	-10640	477.5
1998	VSSIDUM77	-10654	622.5
1999	VSSIDUM78	-10668	477.5
2000	VSSIDUM79	-10682	622.5
2001	VSSIDUM80	-10696	477.5
2002	VSSIDUM81	-10710	622.5
2003	VSSIDUM82	-10724	477.5
2004	VSSIDUM83	-10738	622.5
2005	VSSIDUM84	-10752	477.5
2006	VSSIDUM85	-10766	622.5
2007	VSSIDUM86	-10780	477.5
2008	VSSIDUM87	-10794	622.5
2009	VSSIDUM88	-10808	477.5
2010	VSSIDUM89	-10822	622.5
2011	VSSIDUM90	-10836	477.5
2012	VSSIDUM91	-10850	622.5
2013	VSSIDUM92	-10864	477.5
2014	VSSIDUM93	-10878	622.5
2015	VSSIDUM94	-10892	477.5
2016	VSSIDUM95	-10906	622.5
2017	VSSIDUM96	-10920	477.5
2018	VSSIDUM97	-10934	622.5
2019	VSSIDUM98	-10948	477.5
2020	VSSIDUM99	-10962	622.5
2021	VSSIDUM100	-10976	477.5
2022	VSSIDUM101	-10990	622.5
2023	VSSIDUM102	-11004	477.5
2024	VSSIDUM103	-11018	622.5
2025	GOUT17	-11032	477.5
2026	GOUT17	-11046	622.5
2027	GOUT18	-11060	477.5
2028	GOUT18	-11074	622.5
2029	GOUT19	-11088	477.5
2030	GOUT19	-11102	622.5
2031	GOUT20	-11116	477.5
2032	GOUT20	-11130	622.5
2033	GOUT21	-11144	477.5
2034	GOUT21	-11158	622.5
2035	GOUT22	-11172	477.5
2036	GOUT22	-11186	622.5
2037	GOUT23	-11200	477.5
2038	GOUT23	-11214	622.5
2039	GOUT24	-11228	477.5
2040	GOUT24	-11242	622.5

No.	Text Name	X-axis	Y-axis
2041	GOUT25	-11256	477.5
2042	GOUT25	-11270	622.5
2043	GOUT26	-11284	477.5
2044	GOUT26	-11298	622.5
2045	GOUT27	-11312	477.5
2046	GOUT27	-11326	622.5
2047	GOUT28	-11340	477.5
2048	GOUT28	-11354	622.5
2049	GOUT29	-11368	477.5
2050	GOUT29	-11382	622.5
2051	GOUT30	-11396	477.5
2052	GOUT30	-11410	622.5
2053	VGLO_L	-11424	477.5
2054	VGLO_L	-11438	622.5
2055	VGLO_L	-11452	477.5
2056	VRGH_L	-11466	622.5
2057	VRGH_L	-11480	477.5
2058	VRGH_L	-11494	622.5
2059	LVGL_L	-11508	477.5
2060	LVGL_L	-11522	622.5
2061	LVGL_L	-11536	477.5
2062	GOUT31	-11550	622.5
2063	GOUT31	-11564	477.5
2064	GOUT32	-11578	622.5
2065	GOUT32	-11592	477.5
2066	VGLO_L	-11606	622.5
2067	VGLO_L	-11620	477.5
2068	VGLO_L	-11634	622.5
2069	VGH	-11648	477.5
2070	VGH	-11662	622.5
2071	VGH	-11676	477.5
2072	PADA4	-11690	622.5
2073	PADB4	-11704	477.5
2074	VSSIDUM104	-11718	622.5
2075	VSSIDUM105	-11732	477.5
2076	VSSIDUM106	-11746	622.5
2077	DUMMY	-11760	477.5
2078	DUMMY	-11774	622.5
2079	DUMMY	-11788	477.5
2080	DUMMY	-11802	622.5
2081	DUMMY	-11816	477.5
2082	DUMMY	-11830	622.5
2083	DUMMY	-11844	477.5
2084	DUMMY	-11858	622.5
2085	DUMMY	-11872	477.5
2086	DUMMY	-11886	622.5
2087	DUMMY	-11900	477.5
2088	DUMMY	-11914	622.5
2089	DUMMY	-11928	477.5
2090	DUMMY	-11942	622.5
2091	DUMMY	-11956	477.5
2092	DUMMY	-11970	622.5
2093	DUMMY	-11984	477.5
2094	DUMMY	-11998	622.5
2095	DUMMY	-12012	477.5
2096	DUMMY	-12026	622.5
2097	DUMMY	-12040	477.5
2098	DUMMY	-12054	622.5
2099	DUMMY	-12068	477.5
2100	DUMMY	-12082	622.5
2101	DUMMY	-12096	477.5
2102	DUMMY	-12110	622.5
2103	DUMMY	-12124	477.5
2104	DUMMY	-12138	622.5
2105	DUMMY	-12152	477.5
2106	DUMMY	-12166	622.5
2107	DUMMY	-12180	477.5
2108	DUMMY	-12194	622.5
2109	DUMMY	-12208	477.5
2110	DUMMY	-12222	622.5
2111	DUMMY	-12236	477.5
2112	DUMMY	-12250	622.5
2113	DUMMY	-12264	477.5
2114	DUMMY	-12278	622.5
2115	DUMMY	-12292	477.5
2116	DUMMY	-12306	622.5
2117	DUMMY	-12320	477.5
2118	DUMMY	-12334	622.5
2119	DUMMY	-12348	477.5
2120	DUMMY	-12362	622.5
2121	DUMMY	-12376	477.5
2122	DUMMY	-12390	622.5
2123	DUMMY	-12404	477.5
2124	DUMMY	-12418	622.5
2125	DUMMY	-12432	477.5
2126	DUMMY	-12446	622.5
2127	DUMMY	-12460	477.5
2128	DUMMY	-12474	622.5
2129	DUMMY	-12488	477.5
2130	DUMMY	-12502	622.5
2131	DUMMY	-12516	477.5
2132	DUMMY	-12530	622.5
2133	DUMMY	-12544	477.5
2134	DUMMY	-12558	622.5
2135	DUMMY	-12572	477.5
2136	DUMMY	-12586	622.5
2137	DUMMY	-12600	477.5
2138	DUMMY	-12614	622.5
2139	DUMMY	-12628	477.5
2140	DUMMY	-12642	622.5
2141	DUMMY	-12656	477.5
2142	DUMMY	-12670	622.5
2143	DUMMY	-12684	477.5
2144	DUMMY	-12698	622.5
2145	DUMMY	-12712	477.5
2146	DUMMY	-12726	622.5
2147	DUMMY	-12740	477.5
2148	DUMMY	-12754	622.5
2149	DUMMY	-12768	477.5
2150	DUMMY	-12782	622.5
2151	DUMMY	-12796	477.5
2152	DUMMY	-12810	622.5
2153	DUMMY	-12824	477.5
2154	DUMMY	-12838	622.5
2155	DUMMY	-12852	477.5
2156	DUMMY	-12866	622.5
2157	DUMMY	-12880	477.5
2158	DUMMY	-12894	622.5
2159	DUMMY	-12908	477.5
2160	DUMMY	-12922	622.5
2161	DUMMY	-12936	477.5
2162	DUMMY	-12950	622.5
2163	DUMMY	-12964	477.5
2164	DUMMY	-12978	622.5
2165	DUMMY	-12992	477.5
2166	DUMMY	-13006	622.5
2167	DUMMY	-13020	477.5
2168	DUMMY	-13034	622.5
2169	DUMMY	-13048	477.5
2170	DUMMY	-13062	622.5
2171	DUMMY	-13076	477.5
2172	DUMMY	-13090	622.5
2173	DUMMY	-13104	477.5
2174	DUMMY	-13118	622.5
2175	DUMMY	-13132	477.5
2176	DUMMY	-13146	622.5
2177	DUMMY	-13160	477.5
2178	DUMMY	-13174	622.5
2179	DUMMY	-13188	477.5
2180	DUMMY	-13202	622.5
2181	DUMMY	-13216	477.5
2182	DUMMY	-13230	622.5
2183	DUMMY	-13244	477.5
2184	DUMMY	-13258	622.5
2185	DUMMY	-13272	477.5
2186	DUMMY	-13286	622.5
2187	DUMMY	-13300	477.5
2188	DUMMY	-13314	622.5
2189	DUMMY	-13328	477.5
2190	DUMMY	-13342	622.5
2191	DUMMY	-13356	477.5
2192	DUMMY	-13370	622.5
2193	DUMMY	-13384	477.5
2194	DUMMY	-13398	622.5
2195	DUMMY	-13412	477.5
2196	DUMMY	-13426	622.5
2197	DUMMY	-13440	477.5
2198	DUMMY	-13454	622.5
2199	DUMMY	-13468	477.5
2200	DUMMY	-13482	622.5
2201	DUMMY	-13496	477.5
2202	DUMMY	-13510	622.5
2203	DUMMY	-13524	477.5
2204	DUMMY	-13538	622.5
2205	DUMMY	-13552	477.5
2206	DUMMY	-13566	622.5
2207	DUMMY	-13580	477.5
2208	DUMMY	-13594	622.5
2209	DUMMY	-13608	477.5
2210	DUMMY	-13622	622.5
2211	DUMMY	-13636	477.5

System Interface

3.7. DBI Type B Parallel Interface

The ILI9806G supports an 8-/9-/16-/18-/24-bit MPU DBI Type B parallel interface. The chip-select CSX (active low) is used to enable or disable the ILI9806G chip. The RESX (active low) is an external reset signal, the WRX is parallel data write strobe, the RDX is parallel data read strobe, and DB [23:0] is parallel data bus.

The ILI9806G latches the input data at the rising edge of the WRX signal. The DCX is the signal for data/command selection. When DCX = 1, DB [23:0] bits are RAM data or command parameters. When DCX = 0, DB [23:0] bits are commands. The DBI Type B bi-directional interface is used for communication between the MPU controller and LCD driver chip. The selection of the parallel interface is shown in Table 8.

Table 8: DBI Type B Parallel Interface

IM3	IM2	IM1	IM0	MPU-Interface Mode	WRX	RDX	DCX	Function
0	0	0	0	DBI Type B 8-bit bus interface		"H"	"L"	Write command code.
					"H"		"H"	Read internal status.
						"H"	"H"	Write parameter or display data.
					"H"		"H"	Reads parameter or display data.
0	0	0	1	DBI Type B 16-bit bus interface		"H"	"L"	Write command code.
					"H"		"H"	Read internal status.
						"H"	"H"	Write parameter or display data.
					"H"		"H"	Reads parameter or display data.
0	0	1	0	DBI Type B 24-bit bus interface		"H"	"L"	Write command code.
					"H"		"H"	Read internal status.
						"H"	"H"	Write parameter or display data.
					"H"		"H"	Reads parameter or display data.
1	1	0	0	DBI Type B 9-bit bus interface		"H"	"L"	Write command code.
					"H"		"H"	Read internal status.
						"H"	"H"	Write parameter or display data.
					"H"		"H"	Reads parameter or display data.
1	1	0	1	DBI Type B 18-bit bus interface		"H"	"L"	Write command code.
					"H"		"H"	Read internal status.
						"H"	"H"	Write parameter or display data.
					"H"		"H"	Reads parameter or display data.

3.7.1. Write Cycle Sequence

The WRX signal is driven from high to low then pulled back to high during the write cycle. The host processor provides information while the display module captures the information from the host processor on the rising edge of the WRX. When the DCX signal is driven to low level, the input data on the interface is interpreted as command information. The DCX signal can also be pulled to high level when the data is RAM data or command parameter.

Figure 2 shows the write cycle of the DBI Type B interface.

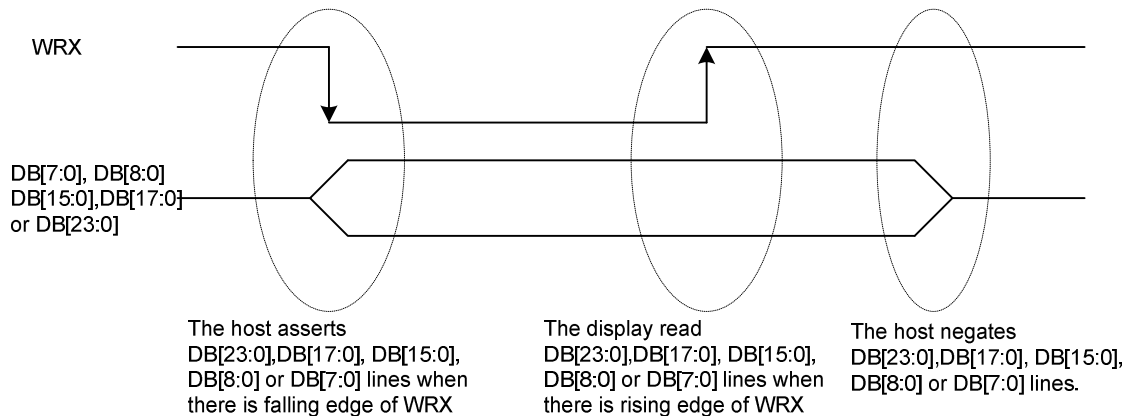


Figure 2: DBI Type B Write Cycle^{Note}

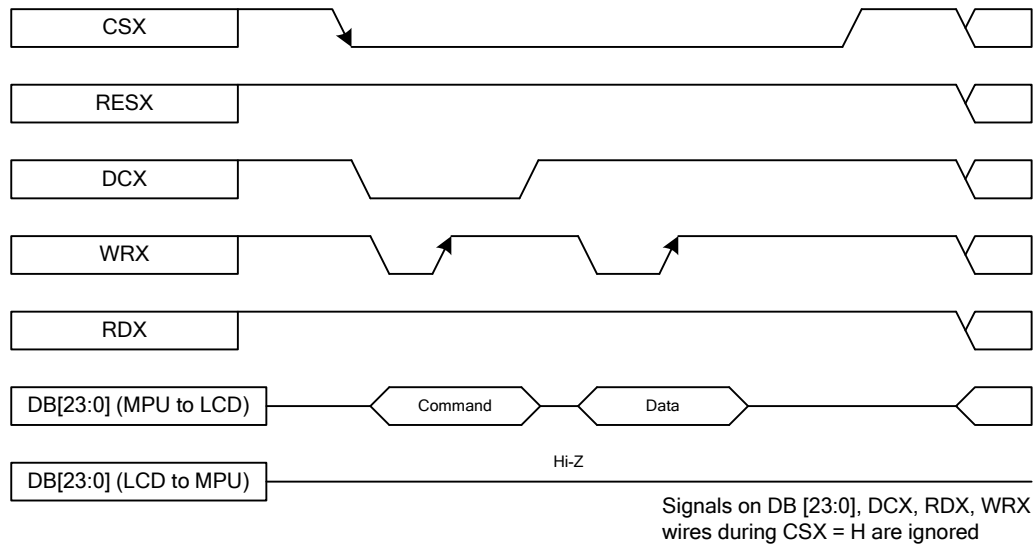


Figure 3: DBI Type B Write Cycle Sequence

^{Note} WRX is an unsynchronized signal, which can be terminated when not in use.

3.7.2. Read Cycle Sequence

The RDX signal is driven from high to low and then pulled back to high during the read cycle. The display module provides information to the host processor while the host processor reads the display module information on the rising edge of the RDX signal. When the DCX signal is driven to the low level, the input data on the interface is interpreted as internal status or parameter data. The DCX signal also can be pulled to high level when the data on the interface is RAM data or a command parameter data.

The following figure shows a read cycle of the DBI Type B interface.

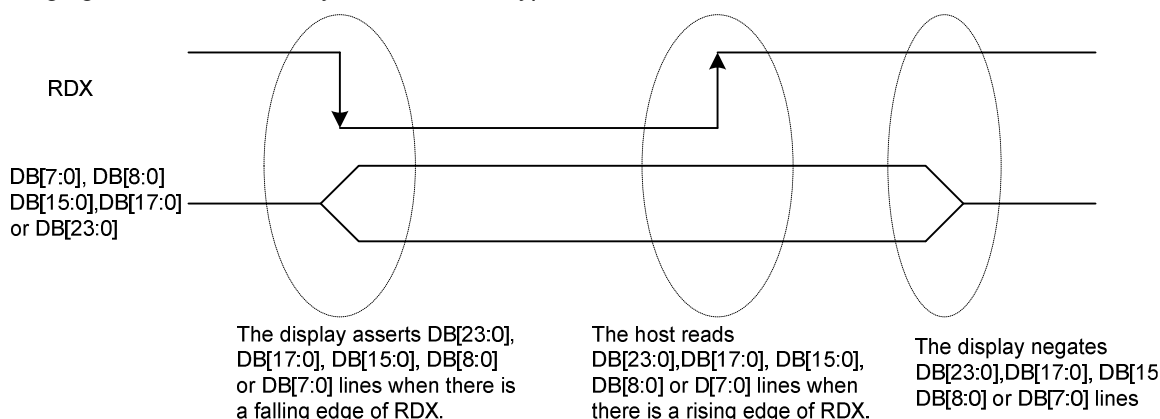


Figure 4: DBI Type B Read Cycle ^{Note 1}

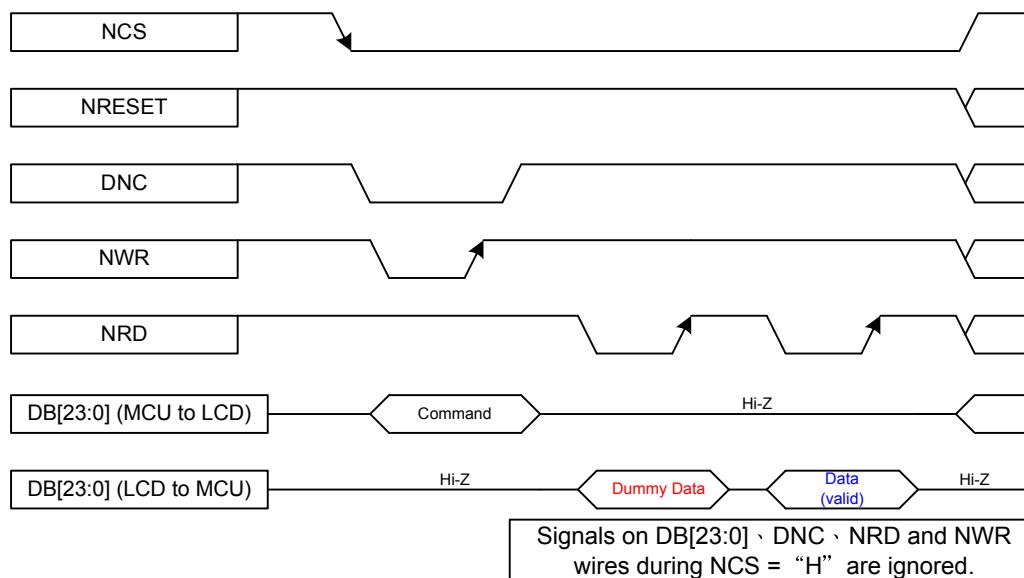


Figure 5: DBI Type B Read Cycle Sequence ^{Note 2}

^{Note 1} RDX is an unsynchronized signal, which can be terminated when not in use.

^{Note 2} Read Data is only valid when the DCX input is pulled high. If the DCX signal is driven low during the read cycle then the display information outputs will be High-Z.

3.7.3. DBI Type B Interface Set Table

24-bit data bus DB [23:0] interface, IM [3:0] = 0010

	Register	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Command/Parameter Write	2Ch / 3Ch																	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Command/Parameter Read	2Eh / 3Eh																	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]

	Set_pixel_format	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
24bpp Frame Memory Write	3'h7	R[7]	R[6]	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[7]	G[6]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[7]	B[6]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]
Frame Memory Read	*	r[7]	r[6]	r[5]	r[4]	r[3]	r[2]	r[1]	r[0]	g[7]	g[6]	g[5]	g[4]	g[3]	g[2]	g[1]	g[0]	b[7]	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0]

Figure 6: DBI Type B 24-bit Data Bus

18-bit data bus DB [17:0] interface, IM [3:0] = 1101

	Register	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Command/Parameter Write	2Ch / 3Ch											D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Command/Parameter Read	2Eh / 3Eh											D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]

	Set_pixel_format	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
18bpp Frame Memory Write	3'h5			R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]

	Set_pixel_format	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
18bpp Frame Memory Write	3'h6	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]

		First Transfer						Second Transfer						Third Transfer					
	Set_pixel_format	DB[17:10]			DB[9:8]			DB[7:0]			DB[17:10]			DB[9:8]			DB[7:0]		
18bpp Frame Memory Write	3'h7	R1[7:0]						G1[7:0]			B1[7:0]						R2[7:0]		
Frame Memory Read	*	r1[7:0]						g1[7:0]			b1[7:0]						r2[7:0]		

Figure 7: DBI Type B 18-bit Data Bus

16-bit data bus DB [15:0] interface, IM [3:0] = 0001

	Set_pixel_format	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Command/Parameter Write	2Ch / 3Ch									D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Command/Parameter Read	2Eh / 3Eh									D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]

	Set_pixel_format	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
16bpp Frame Memory Write	3h5	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]

		First Transfer				Second Transfer				Third Transfer			
	Set_pixel_format	DB[15:10]	DB[9:8]	DB[7:2]	DB[1:0]	DB[15:10]	DB[9:8]	DB[7:2]	DB[1:0]	DB[15:10]	DB[9:8]	DB[7:2]	DB[1:0]
16bpp Frame Memory Write	3h6	R1[5:0]		G1[5:0]		B1[5:0]		R2[5:0]		G2[5:0]		B2[5:0]	

		First Transfer				Second Transfer				Third Transfer			
	Set_pixel_format	DB[15:8]	DB[7:0]			DB[15:8]	DB[7:0]			DB[15:8]	DB[7:0]		
16bpp Frame Memory Write	3h7	R1[7:0]	G1[7:0]			B1[7:0]	R2[7:0]			G2[7:0]	B2[7:0]		
Frame Memory Read	*	r1[7:0]	g1[7:0]			b1[7:0]	r2[7:0]			g2[7:0]	b2[7:0]		

Figure 8: DBI Type B 16-bit Data Bus

9-bit data bus DB [8:0] interface, IM [3:0] = 1100

	Register	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Command/Parameter Write	2Ch / 3Ch		D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Command/Parameter Read	2Eh / 3Eh		D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]

		First Transfer									Second Transfer								
9bpp Frame Memory Write	Set_pixel_format	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
	3'h5	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]		G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]	

		First Transfer										Second Transfer									
9bpp Frame Memory Write	Set_pixel_format	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
	3'h6	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]		

		First Transfer										Second Transfer										Third Transfer									
9bpp Frame Memory Write	Set_pixelL_format	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0			
	3h7	R1[7:0]										G1[7:0]										B1[7:0]									
	Frame Memory Read	*	r1[7:0]										g1[7:0]										b1[7:0]								

Figure 9: DBI Type B 9-bit Data Bus

8-bit data bus DB [7:0] interface, IM [3:0] = 0000

	Register	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Command/Parameter Write	2Ch / 3Ch	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Command/Parameter Read	2Eh / 3Eh	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]

		First Transfer								Second Transfer							
8bpp Frame Memory Write	Set_pixel_format	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
	3h5	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]

		First Transfer								Second Transfer								Third Transfer							
8bpp Frame Memory Write	Set_pixel_format	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
	3h6	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]			G[5]	G[4]	G[3]	G[2]	G[1]	G[0]			B[5]	B[4]	B[3]	B[2]	B[1]	B[0]		


		First Transfer								Second Transfer								Third Transfer							
8bpp Frame Memory Write	Set_pixel_format	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
	3h7	R[7:0]								G[7:0]								B[7:0]							
Frame Memory Read	*	r[7:0]								g[7:0]								b[7:0]							

Figure 10: DBI Type B 8-bit Data Bus

3.8. DBI Type C Serial Interface

The selection of this interface is done by the IM [3:0] pins. See Table 9.

Table 9: DBI Type C Serial Interface

IM3	IM2	IM1	IM0	DBI Type C Mode	CSX	SDA	SCL	Function
X	0	1	1	3-line serial interface	"L"	-		Read/Write command, parameter or display data.

The ILI9806G uses a 3-line 9-bit serial interface for communication between the host and the ILI9806G. The 3-line serial interface consists of the chip enable input (CSX), the serial clock input (SCL), and serial data Input/Output (SDA). If the data bus (DB [23:0]) is not used for the DPI interface data transfer, the unused pins are unaffected. The Serial clock (SCL) is used only for the interface with the MPU, so it can be stopped when no communication is necessary.

3.8.1. Write Cycle Sequence

In the Write Mode of the interface, the host writes commands and data to the ILI9806G. The 3-line serial data packet contains a D/C (data/command) select bit and a transmission byte. If the D/C bit is "low", the transmission byte is interpreted as a command byte. If the D/C bit is "high", the transmission byte is stored in the GRAM as display data, or stored in the command register as a parameter data.

Any instruction can be sent in any order to the ILI9806G and the MSB is transmitted first. The serial interface is initialized when the CSX status is high. In this state, SCL clock pulse and SDI data have no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission. See below for the detail of data format for 3-line serial interface.

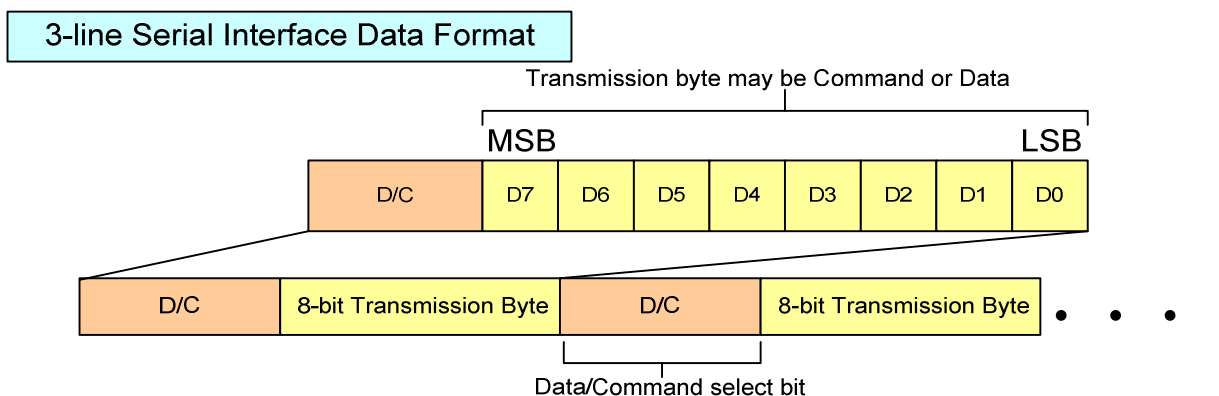


Figure 11: DBI Type C Data Format

The host drives the CSX pin to low and setting the D/C bit on the SDI pin. The bit is read by the ILI9806G on the first rising edge of the SCL signal. On the next falling edge of the SCL, the MSB data bit (D7) is set on the SDI pin by the host. On the next falling edge of the SCL, the next bit (D6) is set on the SDI pin. If the optional D/C signal is used, a byte is eight read cycles long. The 3-line serial interface writes sequences as described in the Figure 12 below.

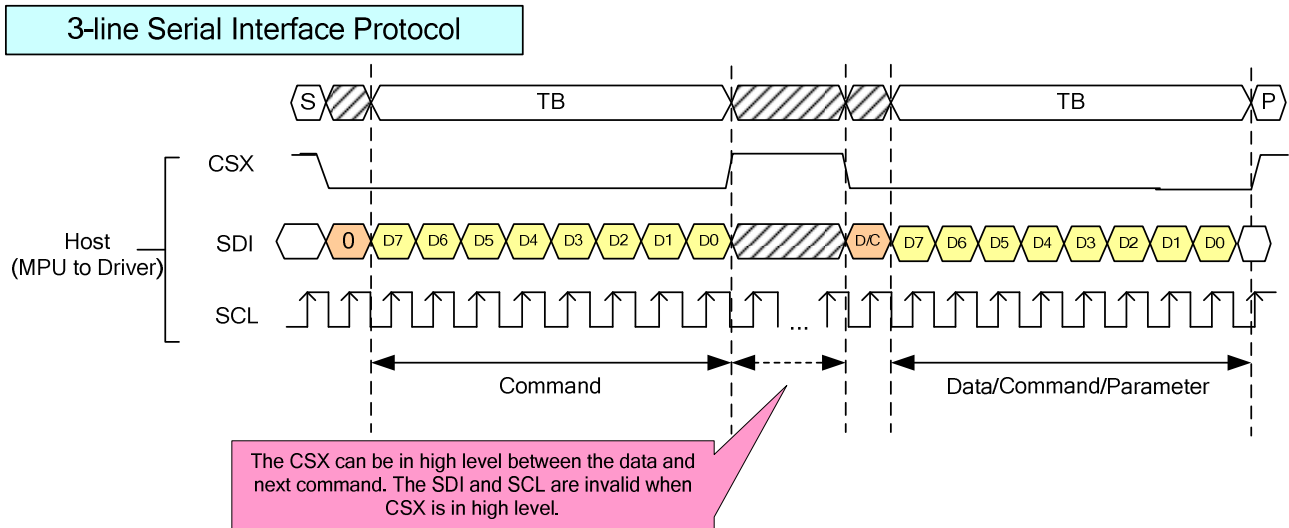


Figure 12: DBI Type C Protocol

3.8.2. Read Cycle Sequence

In the Read Mode of the interface, the host reads the register value from the ILI9806G. The host sends a command (Read ID or register command), then a byte is (bytes are) transmitted in the opposite direction. The ILI9806G samples the SDI (input data) at the rising edge of the SCL (serial clock), and shifts SDO (output data) at the falling edge of the SCL (serial clock). The read mode has three types of transmitted command data (8-/24-/32-bit) according to the command code.

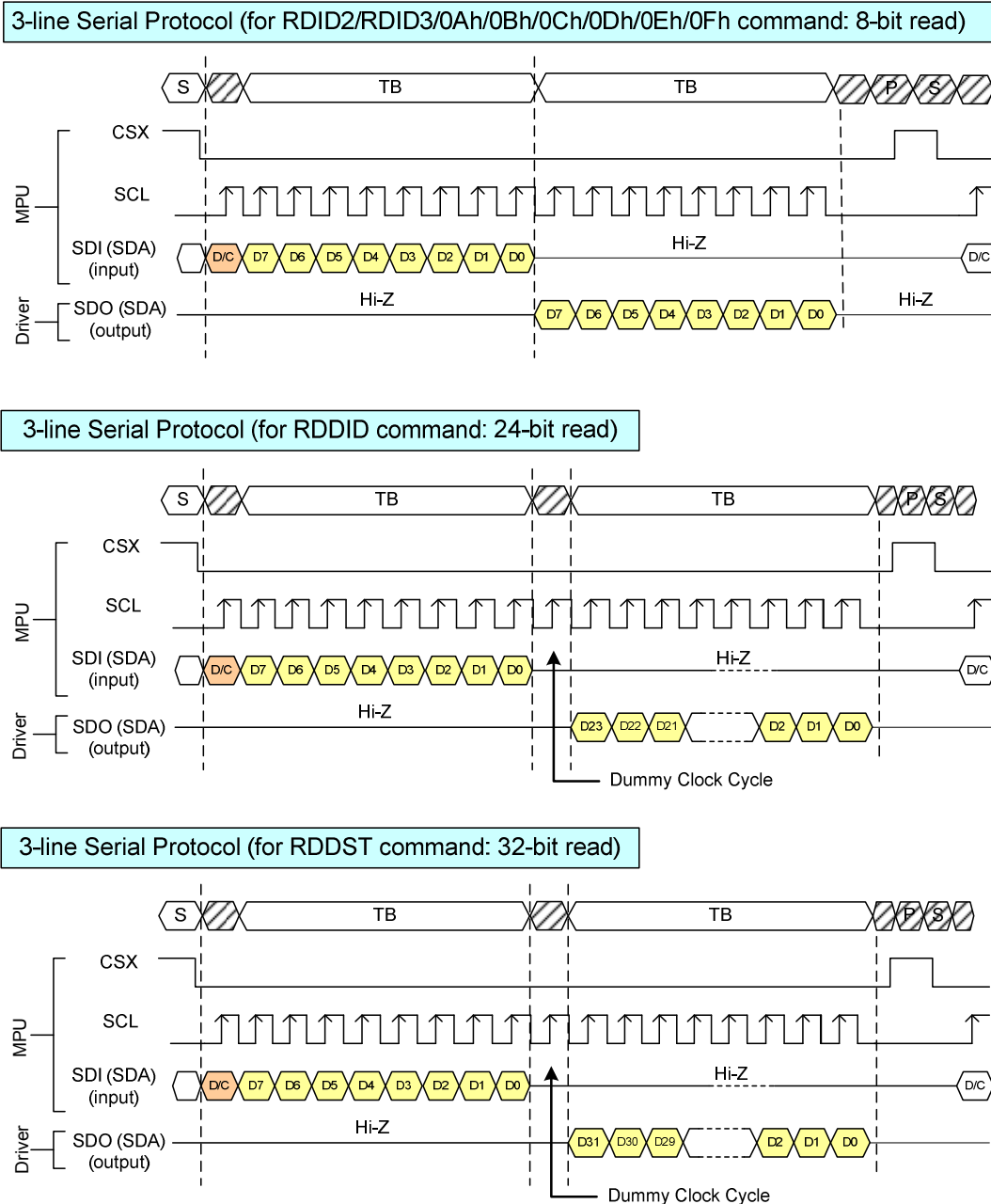


Figure 13: DBI Type C Read Cycle Sequence

3.9. Data Transfer Break and Recovery

If data transmission is interrupted by the CSX pulse while transferring a Command, Frame Memory data or multiple parameter command before Bit D0 of the byte has been completed, then the driver will reject the previous bits and reset the interface so it will be ready to receive the same byte re-transmitted when the chip select pin (CSX) is activated again.

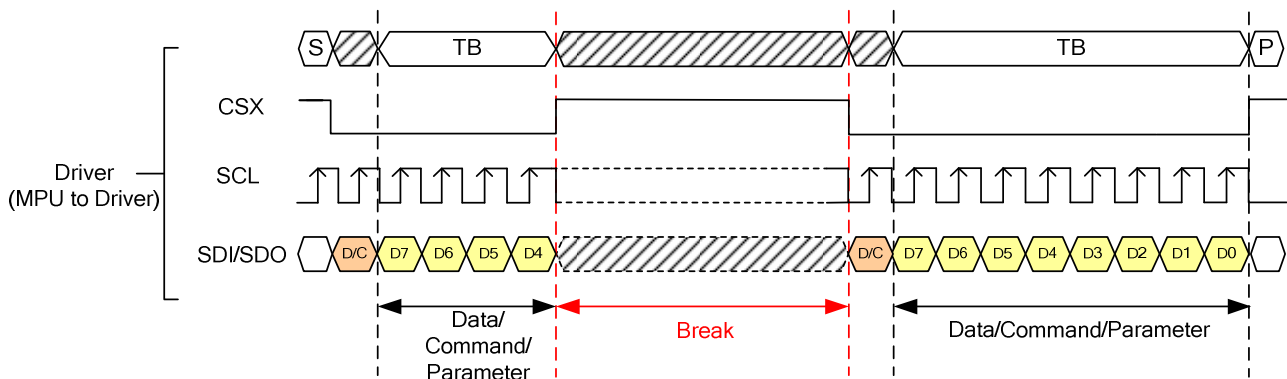


Figure 14: Data Transfer Break and Recovery

If there is a break when transmitting a command with multiple parameters and the host initiates transfer of a new command, the parameters that were successfully transferred are stored and the incomplete parameter data where the break occurred is dropped. The interface is ready to receive the next byte as shown in the figure below.

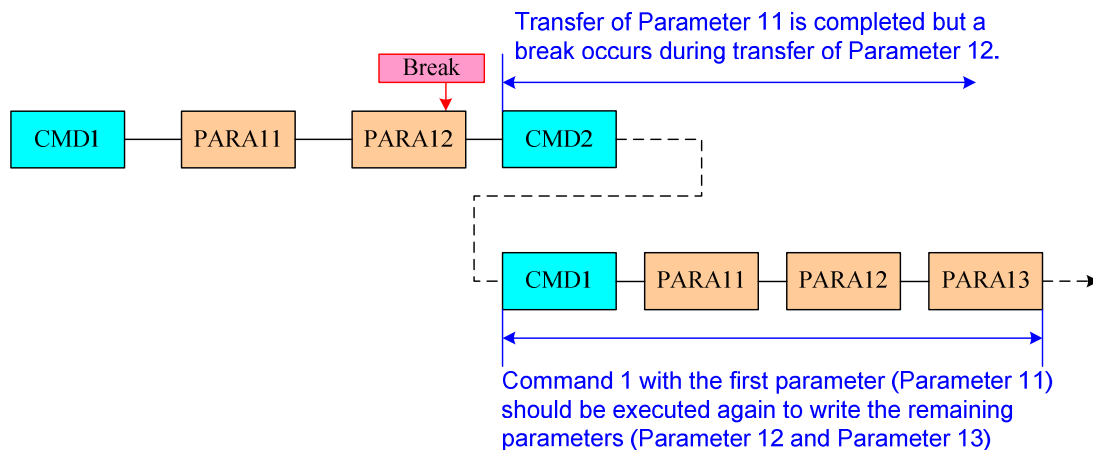


Figure 15: Data Transfer Break - Case 1

If a command with multiple parameters is sent and a break occurs when a new command is sent before all the parameters are transferred, then the parameters that were successfully sent are stored and the remaining parameters of that command remain at the previous value.

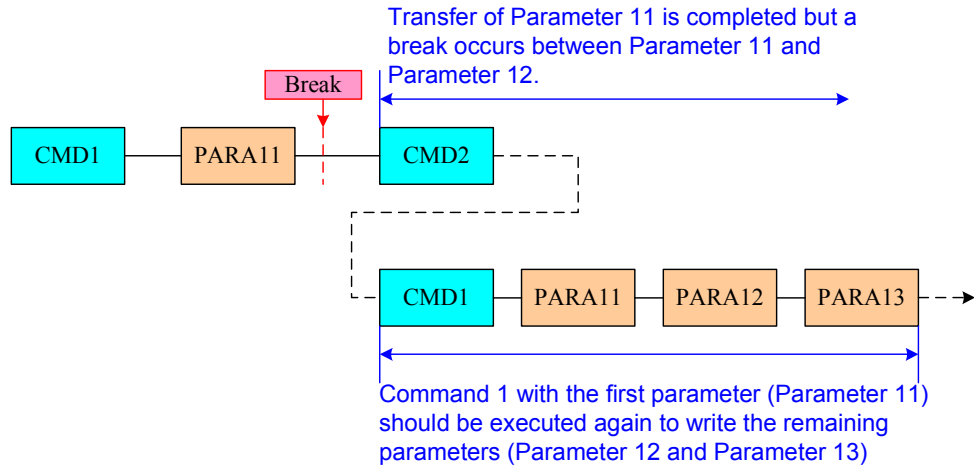


Figure 16: Data Transfer Break - Case 2

3.10. Data Transfer Pause

Transferring a Command, Frame Memory Data, or Multiple Parameter Data might invoke a pause in the data transmission. If the Chip Select pin (CSX) is released after a whole byte of a Frame Memory Data or Multiple Parameter Data has been completed, then the ILI9806G will wait and continue the Frame Memory Data or Parameter Data Transmission from the point where it was paused. If the Chip Select pin is released after a whole byte of a command has been completely transmitted, then the display module will receive either the command's parameters or a new command when the Chip Select Line is enabled again, as shown below.

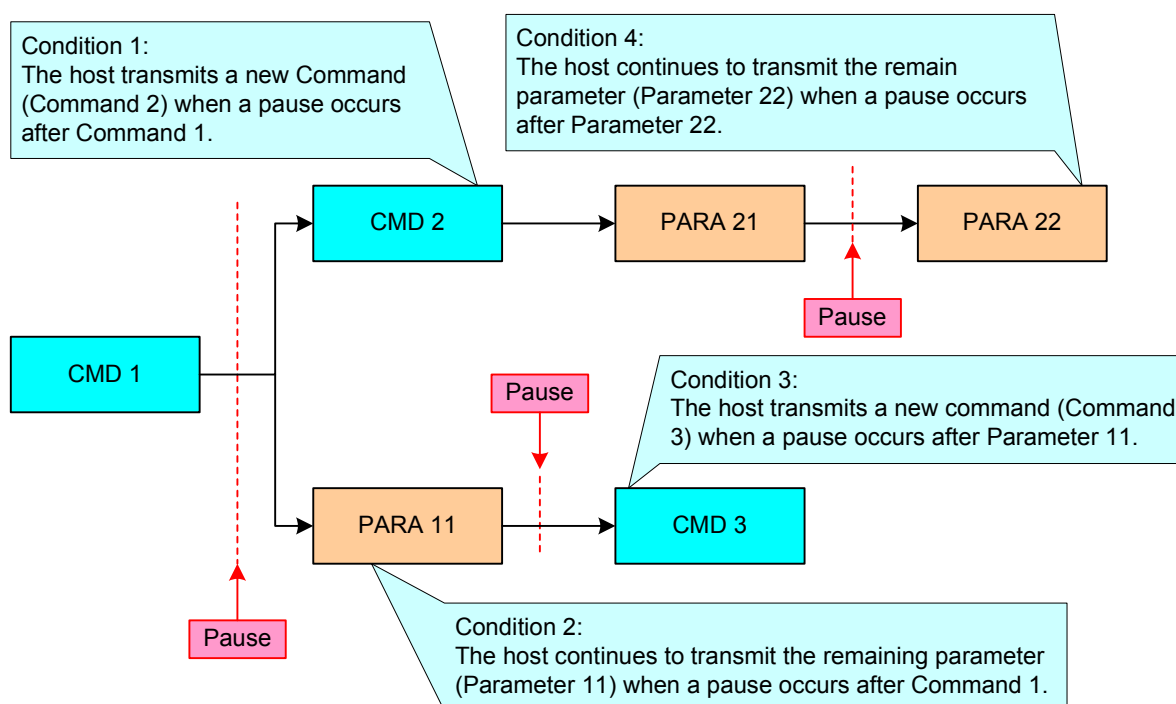


Figure 17: Data Transfer Pause

3.10.1. Serial Interface Pause

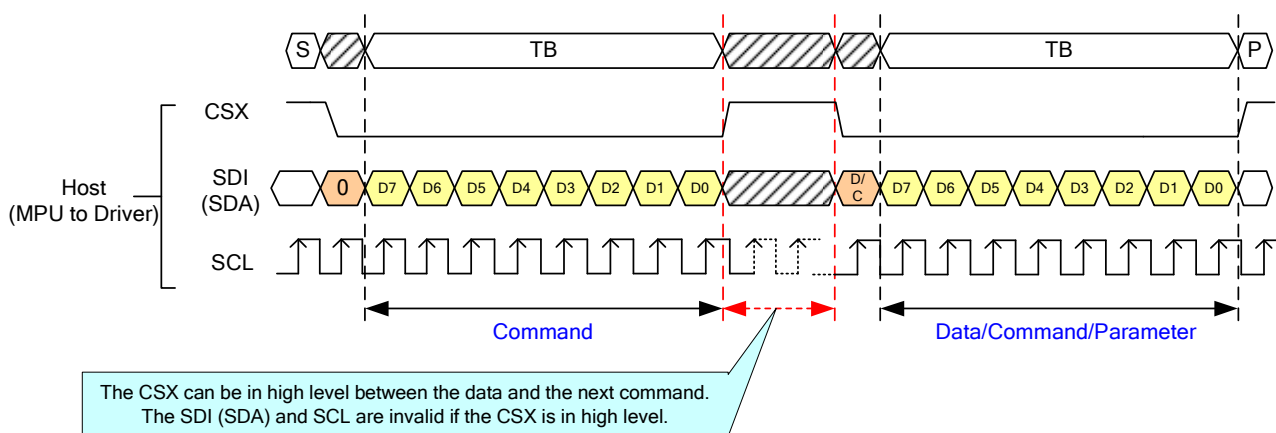


Figure 18: DBI Type C Data Transfer Pause

This applies to the following 4 conditions:

- 1) Command-Pause-Command
- 2) Command-Pause-Parameter
- 3) Parameter-Pause-Command
- 4) Parameter-Pause-Parameter

3.10.2. Parallel Interface Pause

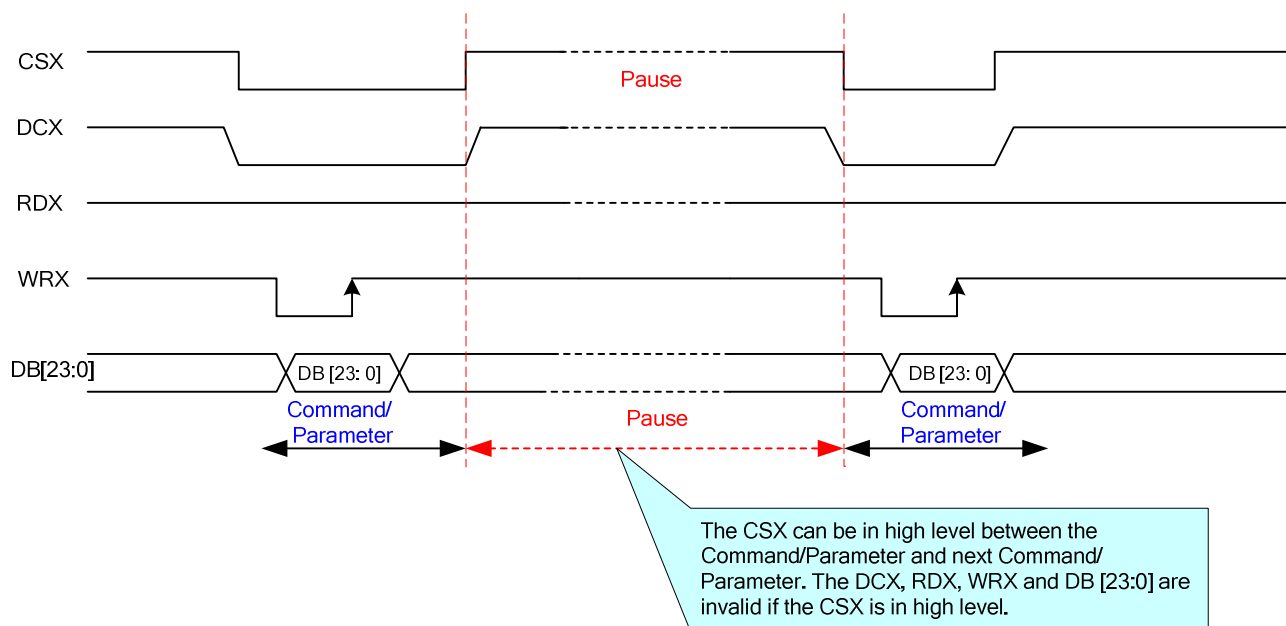


Figure 19: DBI Type B Data Transfer Pause

This applies to the following 4 conditions:

- 1) Command-Pause-Command
- 2) Command-Pause-Parameter
- 3) Parameter-Pause-Command
- 4) Parameter-Pause-Parameter

3.10.3. Data Transfer Mode

The ILI9806G provides five different types of color depth: 8-bit/per pixel, 9-bit/per pixel, 16-bit/per pixel, 18-bit/per pixel, and 24-bit/pixel. The data format is described for each interface. Data can be downloaded to the Frame Memory by 2 methods^{Note}.

3.10.4. Method 1

The Image data is sent to the Frame Memory in the successive Frame writing, each time the Frame Memory is filled by image data, the Frame Memory pointer is reset to the start point and the next Frame is written.

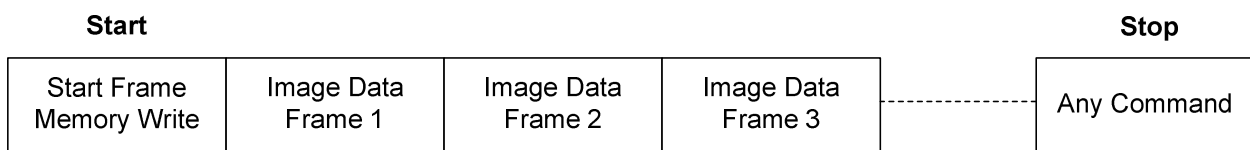


Figure 20: Data Transfer Mode - Method 1

3.10.5. Method 2

Image Data is sent and at the end of each Frame Memory download, a command is sent to stop the Frame Memory Writing. Then Start Memory Write command is sent, and a new Frame is downloaded.

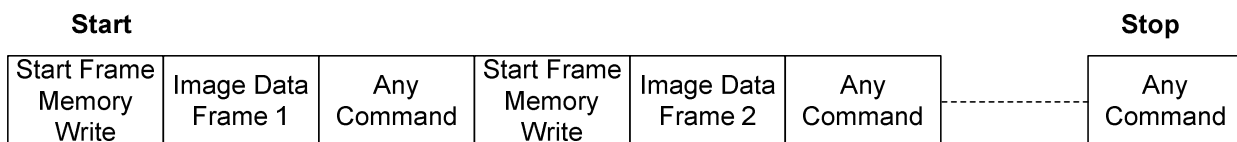


Figure 21: Data Transfer Mode - Method 2

^{Note} 1. These apply to all five kinds of color depth on both serial and parallel interfaces.

2. The Frame Memory can contain both odd and even number of pixels for both methods. Only complete pixel data will be stored in the Frame Memory.

3.11. DPI (RGB) Interface

The DPI can display moving pictures by two ways: rewrite into the GRAM and transmit directly to the shift register. The selection is set by the register BPGRAM and RM bit. The RM bit selects an interface for the access operation of the Frame Memory. For the DPI, RM should be set as 1.

BPGRAM	Display data path
0	Write into Memory

RM	Interface for RAM access
0	System interface
1	RGB interface

The DM bit selects the clock operation mode. It allows switching between display operations in synchronization with the internal oscillation clock. If DM = 1, the external DCK cannot be stopped unless it enters the Sleep In mode.

DM	RGB interface operating clock selection
0	Internal system clock
1	RGB interface DCK (Dot clock)

3.11.1. DPI Interface Selection

The DPI interface is operated with VSYNC, HSYNC, ENABLE, DCK, and DB [23:0] lines. It supports several pixel formats that can be selected by DPI [2:0] bits in Pixel Format Set (R3Ah) command. The selection of a given interface is done by DPI [2:0], as shown in the Table 10 and Figure 22.

Table 10: DPI Interface Selection

DPI [2:0]			DPI (RGB) Interface Mode	Used Pins
1	0	1	16-bit RGB interface	VSYNC, HSYNC, ENABLE, DCK, DB [20:16] , DB [13:8], DB [4:0]
1	1	0	18-bit RGB interface	VSYNC, HSYNC, ENABLE, DCK, DB [21:16] , DB [13:8], DB [5:0]
1	1	1	24-bit RGB interface	VSYNC, HSYNC, ENABLE, DCK, DB [23:0]
Other			Setting prohibited	

```
16-bit DPI interface connection:set pixel format DPI[2:0]=3'h5
```

DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
			R[4]	R[3]	R[2]	R[1]	R[0]			G[5]	G[4]	G[3]	G[2]	G[1]	G[0]				B[4]	B[3]	B[2]	B[1]	B[0]

```
18-bit DPI interface connection:set pixel format DPI[2:0]=3'h6
```

DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
		R[5]	R[4]	R[3]	R[2]	R[1]	R[0]			G[5]	G[4]	G[3]	G[2]	G[1]	G[0]			B[5]	B[4]	B[3]	B[2]	B[1]	B[0]

24-bit DPI interface connection:set pixel format DPI[2:0]=3'h7

DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
	R[6]	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[7]	G[6]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[7]	B[6]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]

Figure 22: DPI Interface 16/18/24-bit Pixel Format Selection

The Pixel clock (DCK) runs all the time without stop, and it is used to enter VSYNC, HSYNC, ENABLE, and DB [23:0] states when there is a rising edge of the DCK. The DCK cannot be used as the internal clock for other functions of the display module.

Vertical synchronization (VSYNC) is used to indicate when a new frame of the display is received. This is a low enable and its state is read to the display module by the rising edge of the DCK signal.

Horizontal synchronization (HSYNC) is used to indicate when a new line of the frame is received. This is a low enable and its state is read to the display module by the rising edge of the DCK signal.

Data Enable (ENABLE) is used to indicate when the RGB information that should be transferred to the display is received. This is a high enable and its state is read to the display module by the rising edge of the DCK signal. DB [23:0] are used to indicate what is the information of the image that is transferred to the display (when ENABLE = 0 (low) and there is a rising edge of DCK). DB [23:0] can be 0 (low) or 1 (high). These lines are read by the rising edge of the DCK signal. In RGB interface modes, the input display data is written to the GRAM first then outputs the corresponding source voltage according to the gray data from the GRAM.

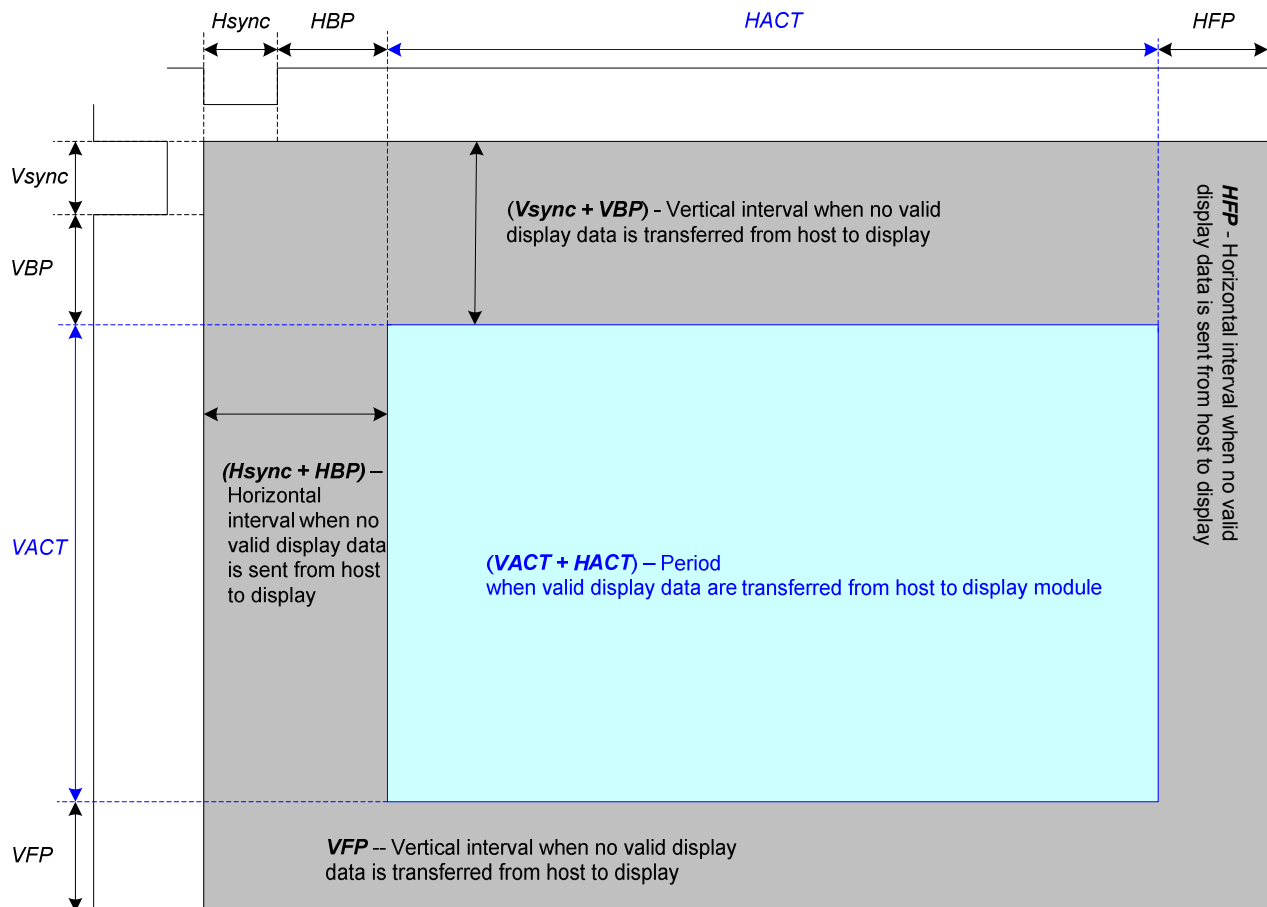


Figure 23: General DPI Timing Diagram

3.11.2. DPI Interface Timing

The timing chart of 24-/18-/16-bit DPI interface mode is illustrated in Figure 24.

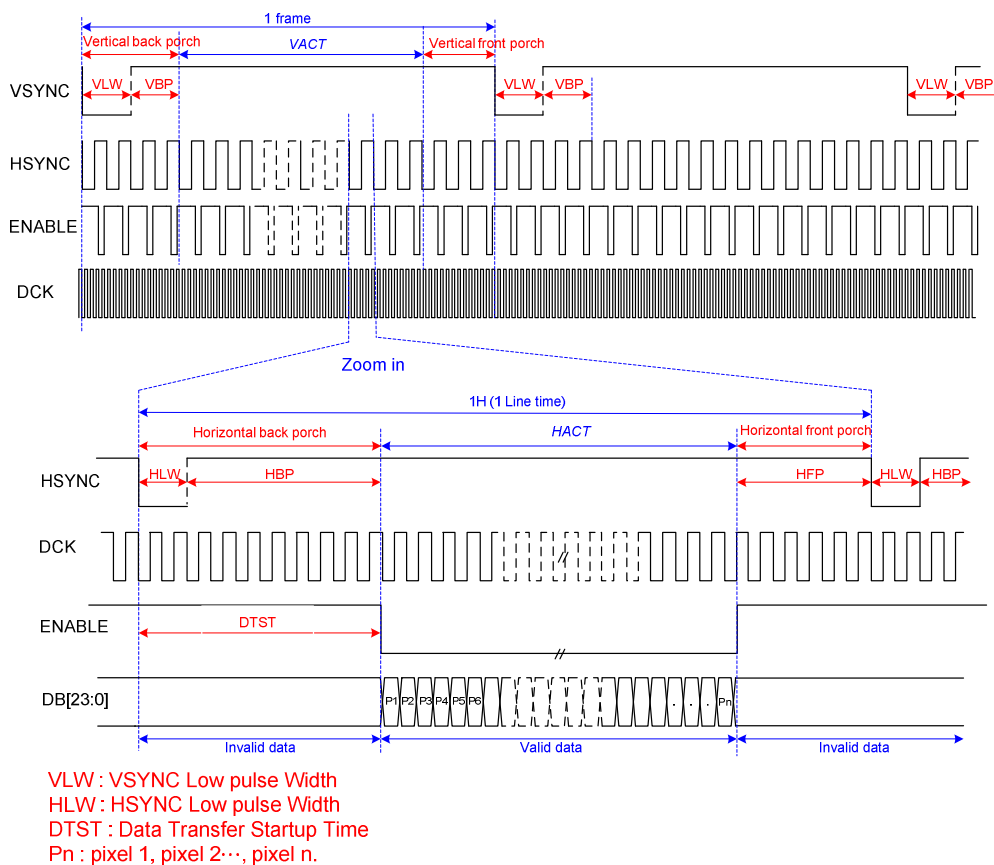
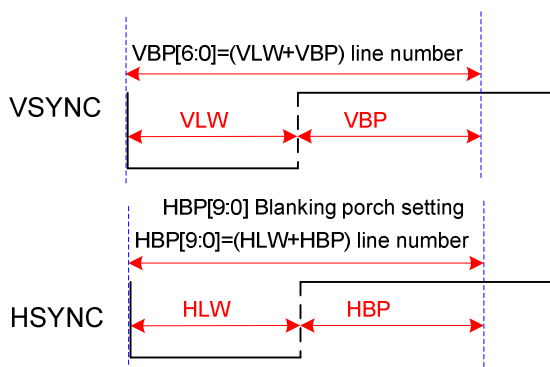


Figure 24: DPI Interface Timing diagram ^{Note}



Constraint1 : Vertical back porch: Minimum VLW ≥ 2 H , VBP ≥ 8 , VFP ≥ 8

Constraint2 : Horizontal porch: Minimum HLW ≥ 2 clocks , HBP ≥ 20 clocks, HFP ≥ 20 clocks

^{Note} VSPL = 0, HSPL = 0, DPL = 0, and EPL = 0 of Interface Mode Control B0h command.

3.12. DSI System Interface

3.12.1. General Description

The MIPI DSI is enabled or disabled by the external IM [3:0] pin.

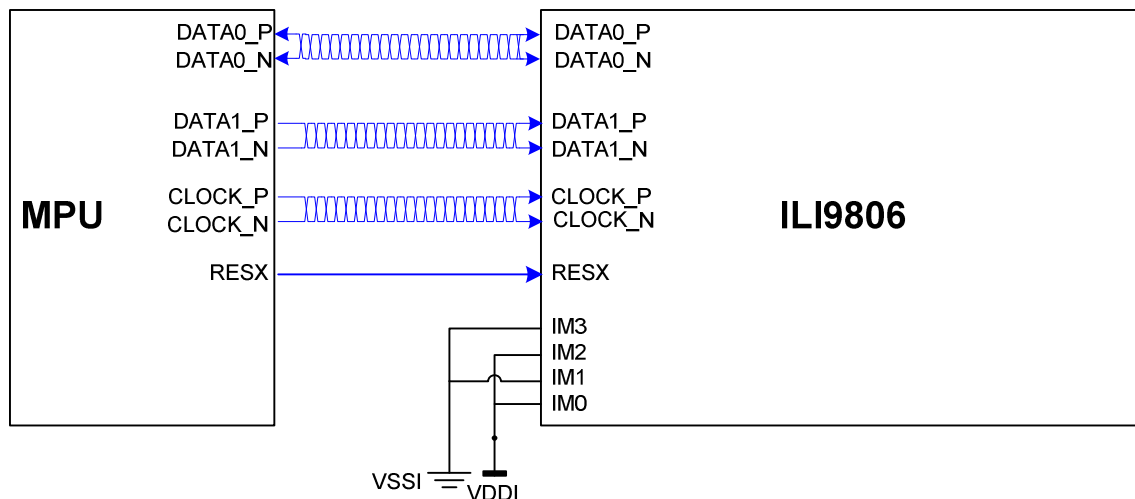


Figure 25: DSI System Interface Diagram

IM3	IM2	IM1	IM0	MPU Interface	Data Pin in Use
0	1	0	1	DSI interface	DSI_CP, DSI_CN DSI_D0P, DSI_D0N DSI_D1P, DSI_D1N

The communication is separated into two different levels between the MPU and the display module:

- Low level communication is done on the interface level.
- High level communication is done on the packet level.

3.12.2. Interface Level Communication

3.12.3. General

The display module uses data and clock lane differential pairs for DSI (DSI-2M). Both differential lane pairs can be driven to the Low Power (LP) or High Speed (HS) mode.

Low Power mode means that each line of the differential pair is used in the single ended mode, a differential receiver is disable (a termination resistor of the receiver is disable), and it can be driven into a low power mode.

High Speed mode means that differential pairs (the termination resistor of the receiver is enable) are not used in the single ended mode.

Different modes and protocols are used in each mode when information is to be transferred from the MPU to the display module and vice versa.

The State Codes of the High Speed (HS) and Low Power (LP) lane pair are defined below.

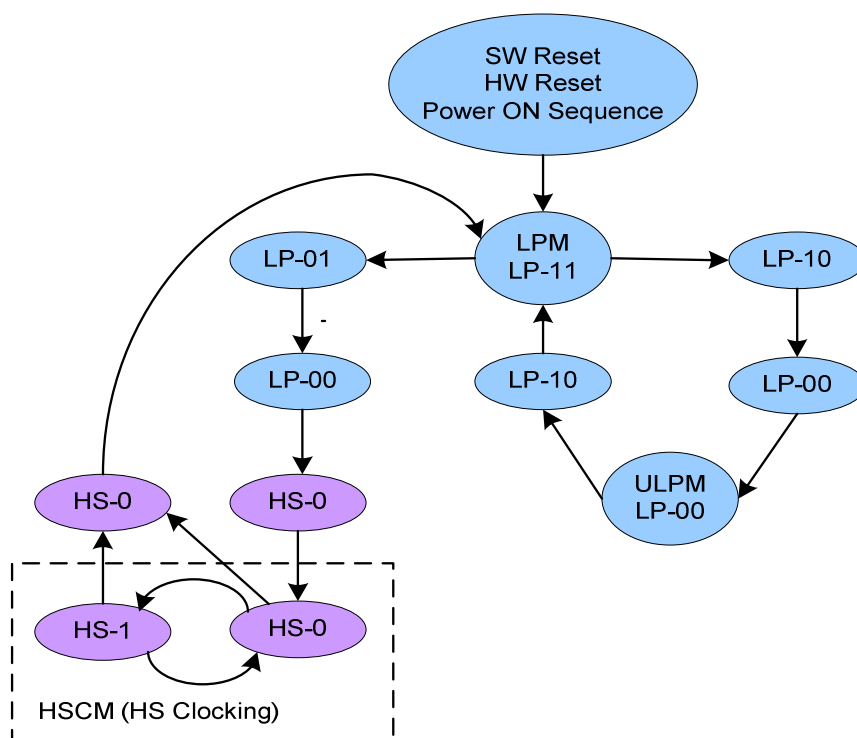
Table 11: High Speed and Low-Power Lane Pair State Codes

Lane Pair State Code	Line DC Voltage Levels		High Speed (HS)	Low Power	
	DATA_P	DATA_N	Burst Mode	CLOCK_P	CLOCK_N
HS-0	Low (HS)	High (HS)	Differential – 0	Note 1	Note 1
HS-1	High (HS)	Low (HS)	Differential – 1	Note 1	Note 1
LP-00	Low (LP)	Low (LP)	Not Defined	Bridge	Space
LP-01	Low (LP)	High (LP)	Not Defined	HS – Request	Mark - 0
LP-10	High (LP)	Low (LP)	Not Defined	LP - Request	Mark - 1
LP-11	High (LP)	High (LP)	Not Defined	Stop	Note 2

3.12.4. DSI-CLK Lanes

DSI-CLK+/- lanes can be driven into three different power modes: Low Power Mode (LPM), Ultra Low Power Mode (ULPM), or High Speed Clock Mode (HSCM). Clock lanes are in the single ended mode (LP = Low Power) when entering or leaving the Low Power Mode (LPM) or Ultra Low Power Mode (ULPM). Likewise, clock lanes are in the single ended mode (LP = Low Power) when entering in or leaving the High Speed Clock Mode (HSCM). These entering and leaving protocols use clock lanes in the single ended mode to generate an entering or leaving sequence.

The principal flow chart of the different power modes of clock lanes is illustrated below.


Figure 26: Power Modes of Clock Lanes

Note 1 Low-Power Receivers (LP-Rx) of the lane pair will check the LP-00 state code when the Lane Pair is in the High Speed (HS) mode.

Note 2 If Low-Power Receivers (LP-Rx) of the lane pair recognizes the LP-11 state code, the lane pair returns to the LP-11 of the Control Mode.

3.12.5. Low Power Mode (LPM)

When DSI-CLK lanes enter the LP-11 State Code, DSI-CLK+/- lanes can be driven to the Low Power Mode (LPM) in three different ways:

- 1) After SW Reset, HW Reset or Power On Sequence => LP-11
- 2) After DSI-CLK+/- lanes leave the Ultra Low Power Mode (ULPM, LP-00 State Code) => LP-10 => LP-11 (LPM)

The sequence is illustrated below.

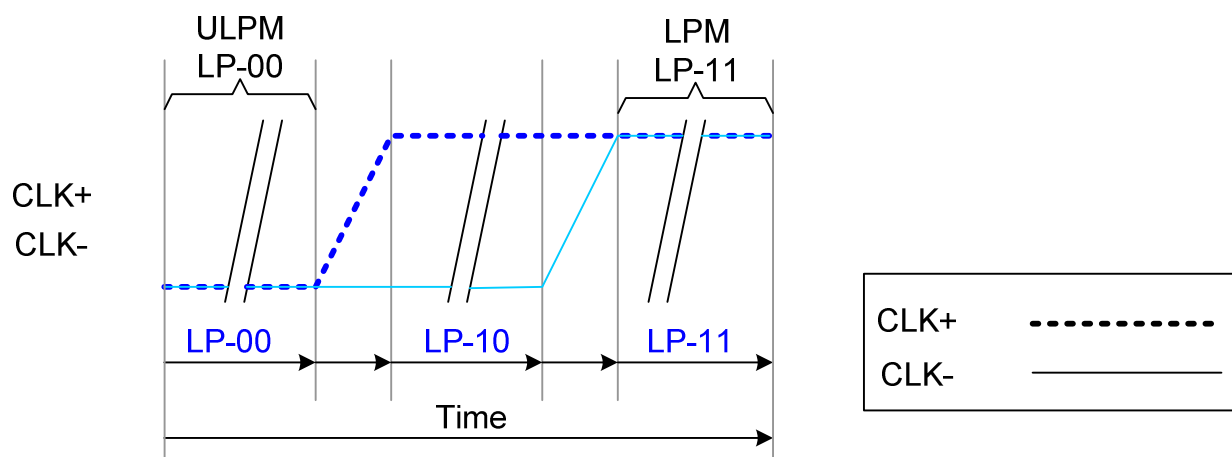


Figure 27: From ULPM to LPM

- 3) After DSI-CLK+/- lanes leave the High Speed Clock Mode (HSCM, HS-0 or HS-1 State Code) => HS-0 => LP-11 (LPM). The sequence is illustrated below.

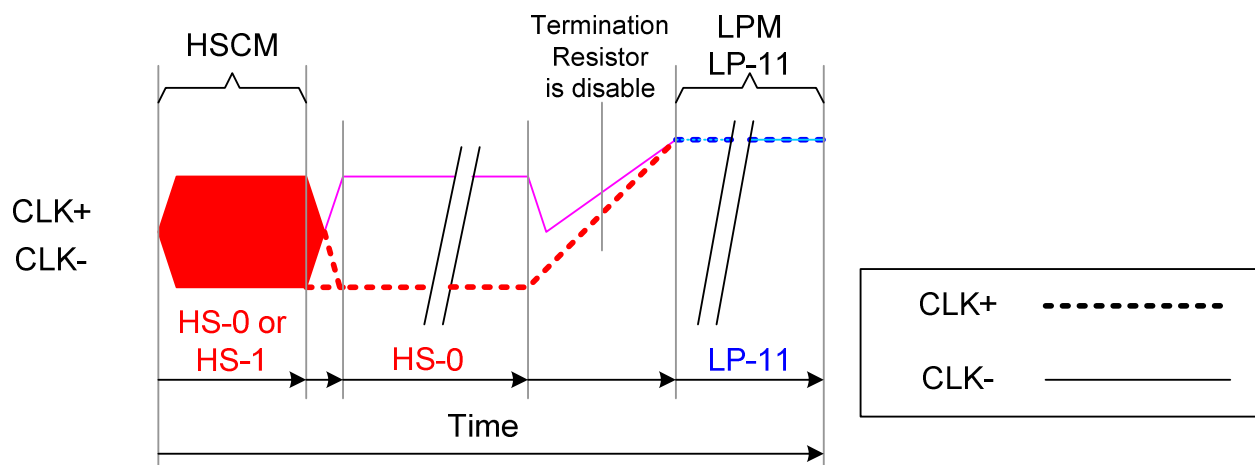


Figure 28: From High Speed Clock Mode (HSCM) to LPM

All the changes of the three modes are illustrated in the flow chart below.

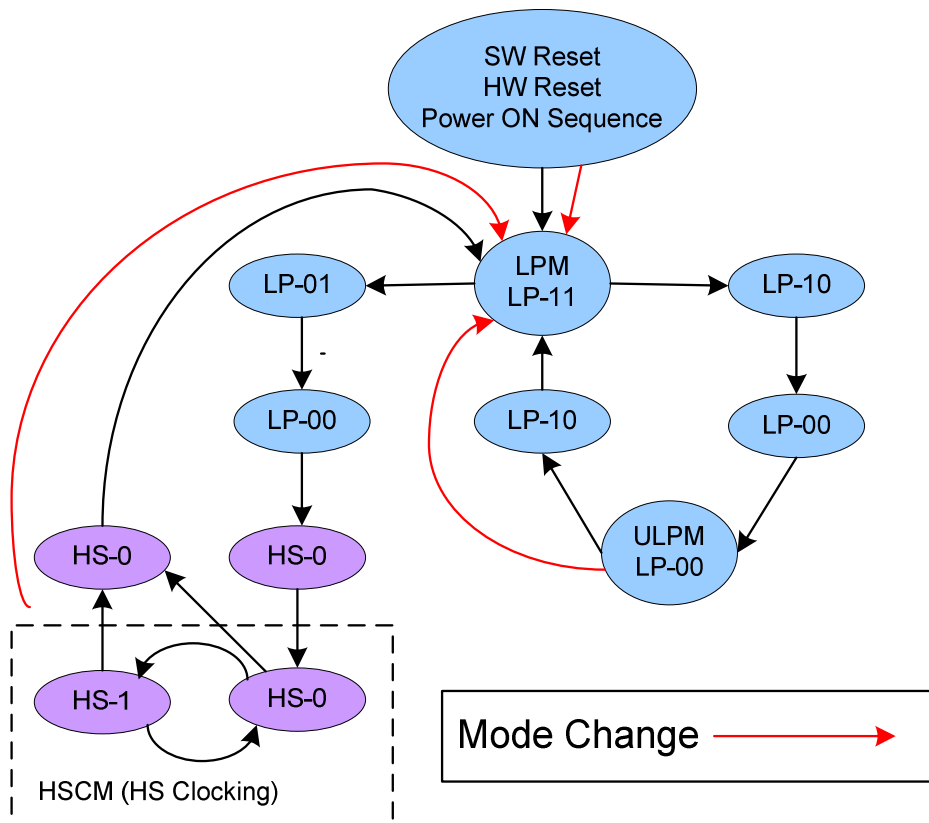


Figure 29: All the Changes of the Three Modes to the LPM

3.12.6. Ultra Low Power Mode (ULPM)

DSI-CLK+/- lanes can be driven to the Ultra Low power Mode (ULPM) when DSI-CLK lanes enter the LP-00 State Code. The only possibility is from the Low Power Mode (LPM, LP-11 State Code) => LP-10 => LP-00 (ULPM).

The sequence is illustrated below.

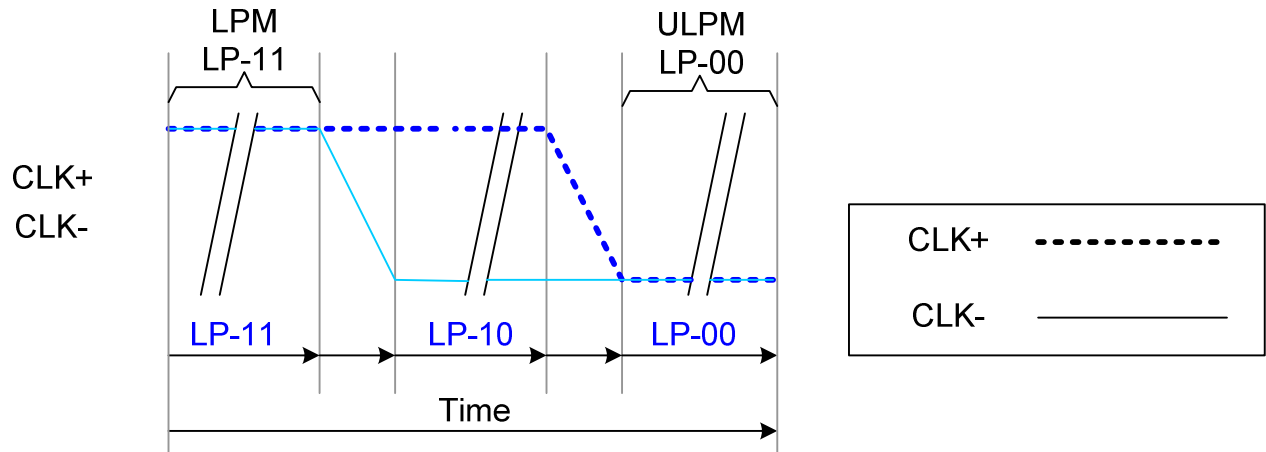


Figure 30: From LPM to ULPM

The mode change is illustrated below.

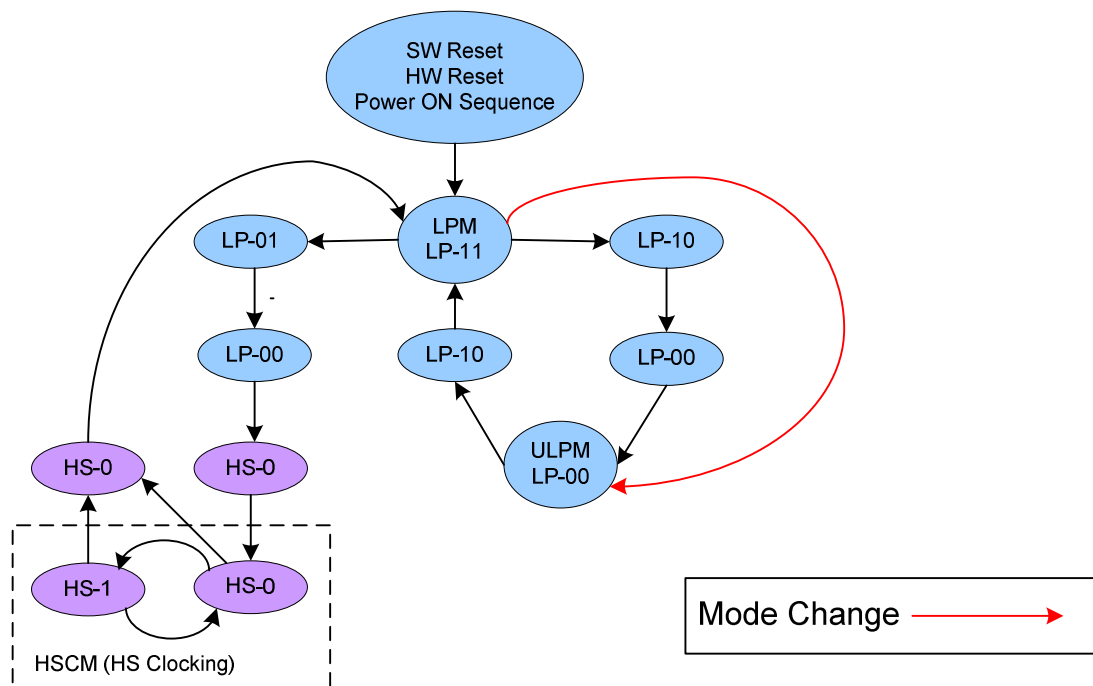


Figure 31: Mode Change from LPM to ULPM

3.12.7. High-Speed Clock Mode (HSCM)

DSI-CLK+/- lanes can be driven to the High Speed Clock Mode (HSCM) when DSI-CLK lanes start to work between HS-0 and HS-1 State Codes.

The only entering possibility is from the Low Power Mode (LPM, LP-11 State Code) =>LP-01 => LP-00 => HS-0 => HS-0/1 (HSCM). The sequence is illustrated below.

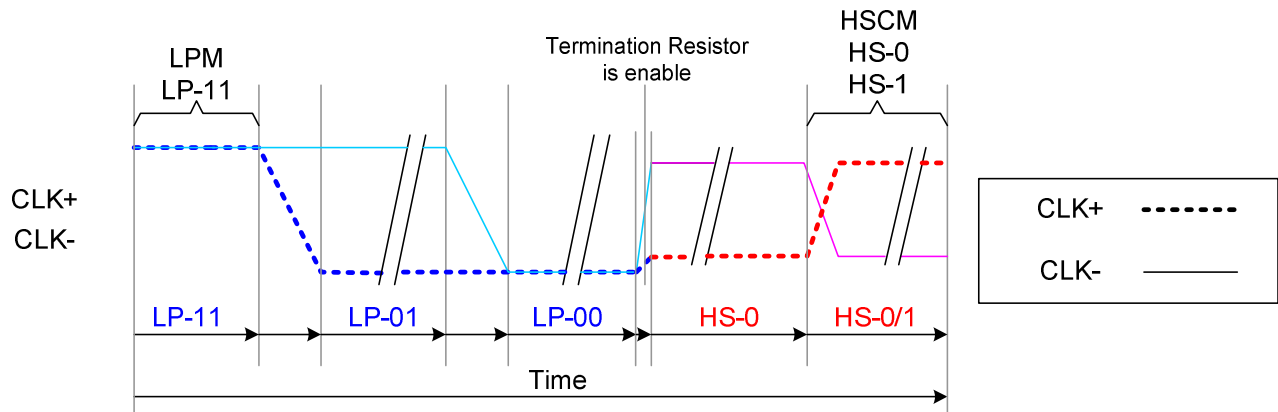


Figure 32: From LPM to HSCM

The mode change is illustrated below.

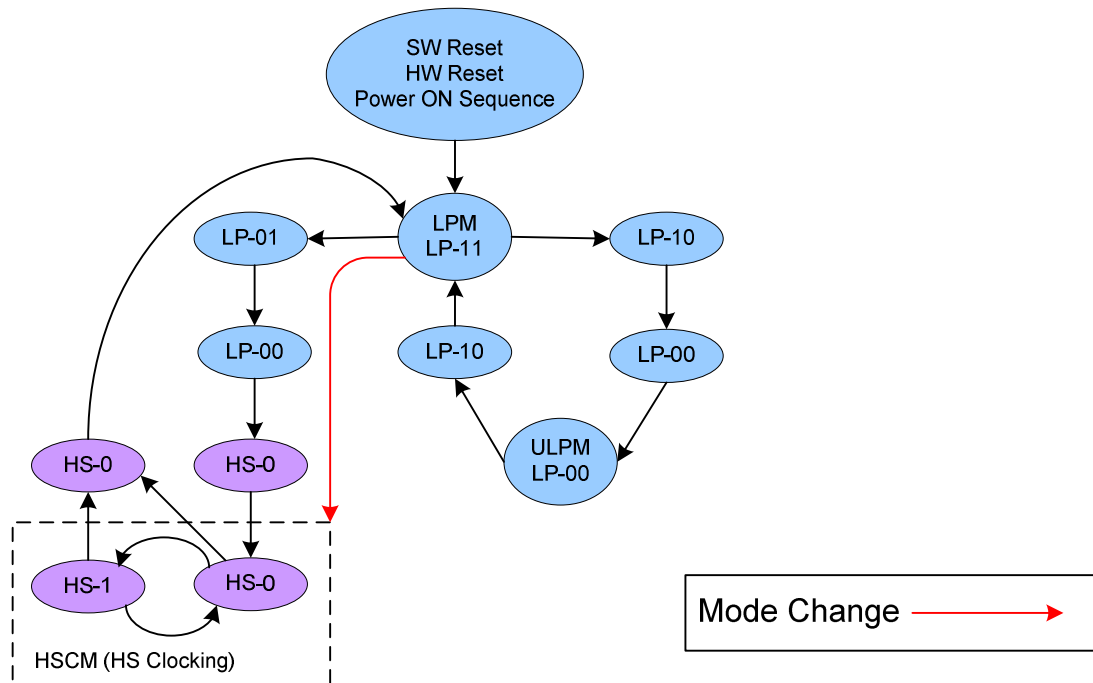


Figure 33: Mode Change from LPM to HSCM

The high speed clock (DSI-CLK+/-) starts before high speed data is sent via DSI-D1+/- or DSI-D0+/- lanes. The high speed clock continues clocking after the high speed data sending is stopped.

The burst of the high speed clock consists of:

- Even number of transitions
- Start state is HS-0
- End state is HS-0

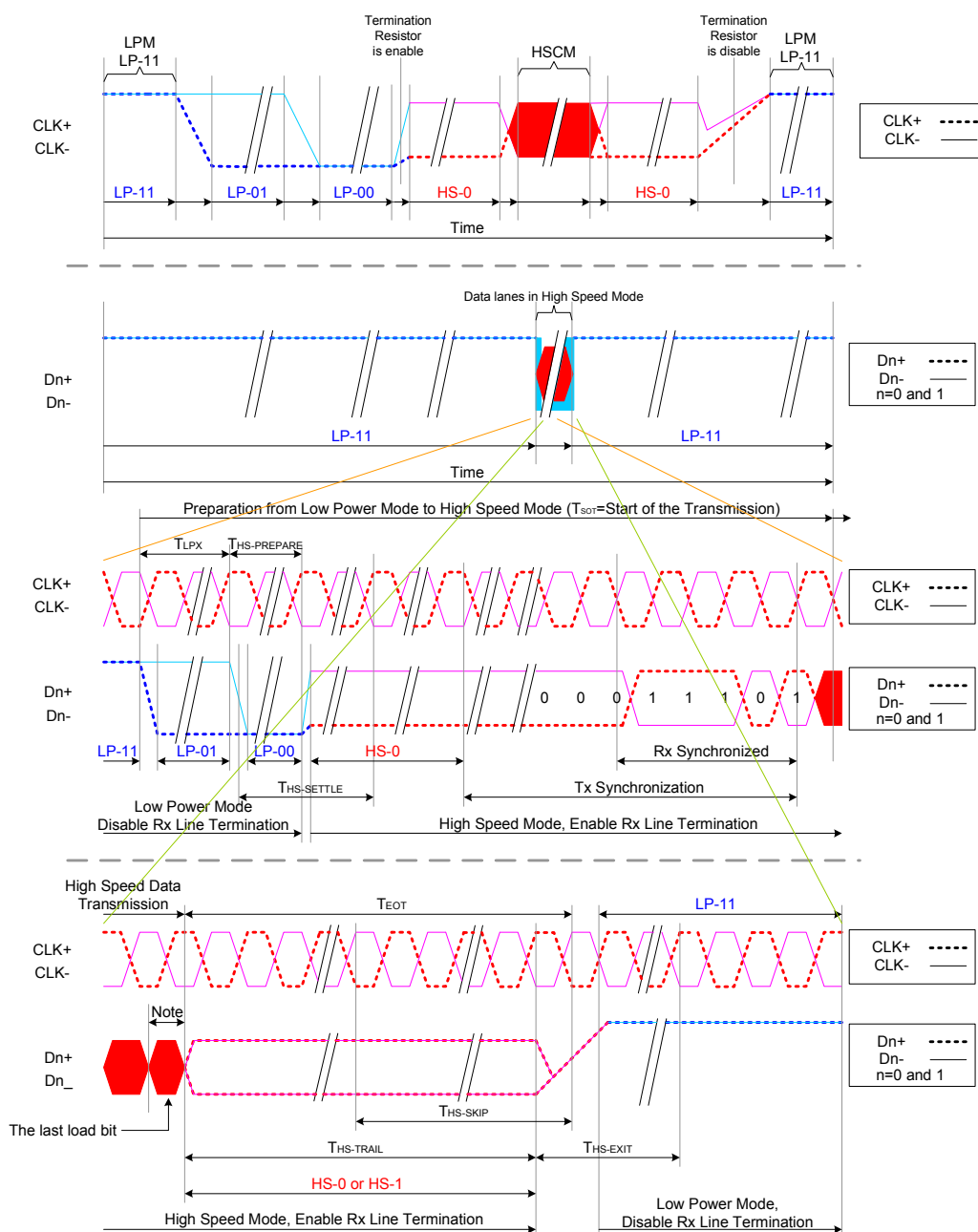


Figure 34: High Speed Clock Burst^{Note}

^{Note} 1. If the last load bit is HS-0, the transmitter changes from HS-0 to HS-1.
2. If the last load bit is HS-1, the transmitter changes from HS-1 to HS-0.

3.12.8. DSI-D1 and DSI-D0 Data Lanes

3.12.9. General

DSI-D1+/- and DSI-D0+/- Data Lanes can be driven to different modes:

- Escape Mode (only DSI-D0+/- data lanes are used)
- High-Speed Data Transmission (DSI-D1+/- and DSI-D0+/- data lanes are used)
- Bus Turnaround Request (only DSI-D0+/- data lanes are used)

These modes and their entering codes are defined in the following table.

Table 12: Entering and Leaving Sequences^{Note}

Mode	Entering Mode Sequence	Leaving Mode Sequence
Escape Mode	LP-11 → LP-10 → LP-00 → LP-01 → LP-00	LP-00 → LP-10 → LP-11 (Mark-1)
High-Speed Data Transmission	LP-11 → LP-01 → LP-00 → HS-0	(HS-0 or HS-1) → LP-11
Bus Turnaround Request	LP-11 → LP-10 → LP-00 → LP-10 → LP-00	Hi-Z

3.12.10. Escape Modes

DSI-D0+/- data lanes can be used in different Escape Modes when data lanes are in the Low Power (LP) mode.

These Escape Modes are used to:

- Send “Low-Power Data Transmission” (LPDT) from the MPU to the display module,
- Drive data lanes to “Ultra-Low Power State” (ULPS),
- Indicate “Remote Application Reset” (RAR), which can reset the display module,
- Indicate “Tearing Effect” (TEE), which is used to transmit a TE line event from the display module to the MPU,
- Indicate “Acknowledge” (ACK), which is used to transmit a non-error event from the display module to the MPU.

The basic sequence of the Escape Mode is as follows:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 => LP-10 => LP-00 => LP-01 => LP-00
- Escape Command (EC), which is coded when one of the data lanes changes from low-to-high-to-low, then this changed data lane presents the value of the current data bit (DSI-D0+ = 1, DSI-D0- = 0). For example, when DSI-D0- changes from low-to-high-to-low, the receiver latches a data bit, which value is the logical 0. The receiver uses this low-to-high-to-low transition for its internal clock.
- A load if necessary
- Exit Escape (Mark-1) LP-00 => LP-10 => LP-11
- End: LP-11

^{Note} 1. DSI-D1+/- and DSI-D0+/- data lanes are used.
2. See more information in the chapter of Bus Turnaround.

This basic construction is illustrated below:

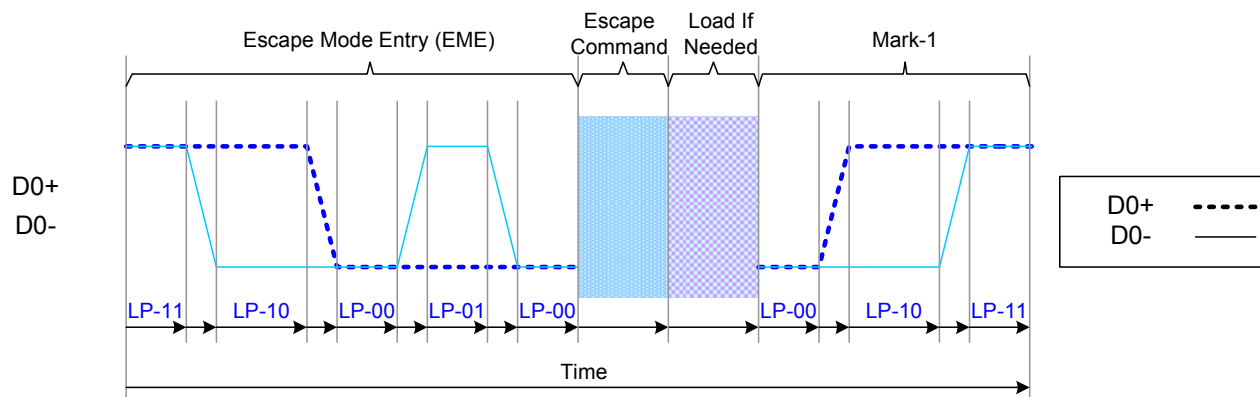


Figure 35: General Escape Mode Sequence

A total of eight Escape Commands (EC) are divided into two types: Mode and Trigger, as described in Table 13: Escape Commands.

An example of a Mode type Escape Command is Ultra-Low Power Mode, where the MPU instructs the display module to enter its Ultra-Low Power Mode.

An example of a Trigger type Escape Command is Tearing Effect. In this case, the MPU has already instructed the display module to provide this trigger and is waiting for a response. The display module then sends a TE trigger (TEE) on the next V-sync event.

Escape commands are defined in the table below.

Table 13: Escape Commands^{Note}

Escape command	Command Type Mode/Trigger	Entry command Pattern (First Bit → Last Bit Transmitted)	Dn	D0
Low-Power Data Transmission	Mode	1110 0001 b	-	X
Ultra-Low Power Mode	Mode	0001 1110 b	X	X
Undefined-1, ^{Note 1}	Mode	1001 1111 b	-	-
Undefined-2, ^{Note 1}	Mode	1101 1110 b	-	-
Remote Application Reset	Trigger	0110 0010 b	-	X
Tearing Effect	Trigger	0101 1101 b	-	X
Acknowledge	Trigger	0010 0001 b	-	X
Unknown-5, ^{Note 1}	Trigger	1010 0000 b	-	-

^{Note} 1. This Escape command is not implemented in the display module.
2. n = 1
3. x = Supported
4. - = Not Supported

3.12.11. Low-Power Data Transmission (LPDT)

The MPU can send data to the display module in the Low-Power Data Transmission (LPDT) mode when data lanes enter the Escape Mode and Low-Power Data Transmission (LPDT) command is sent to the display module. The display module uses the same sequence as which it sends data to the MPU.

The Low Power Data Transmission (LPDT) uses the following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 => LP-10 => LP-00 => LP-01 => LP-00
- Low-Power Data Transmission (LPDT) command in the Escape Mode: 1110 0001 (first to last bit)
- Load (Data):
 - One or more bytes (8 bit)
 - Data lanes are in the pause mode when data lanes are stopped (both lanes are low) between bytes
- Mark-1: LP-00 => LP-10 => LP-11
- End: LP-11

This sequence is illustrated below for reference purpose:

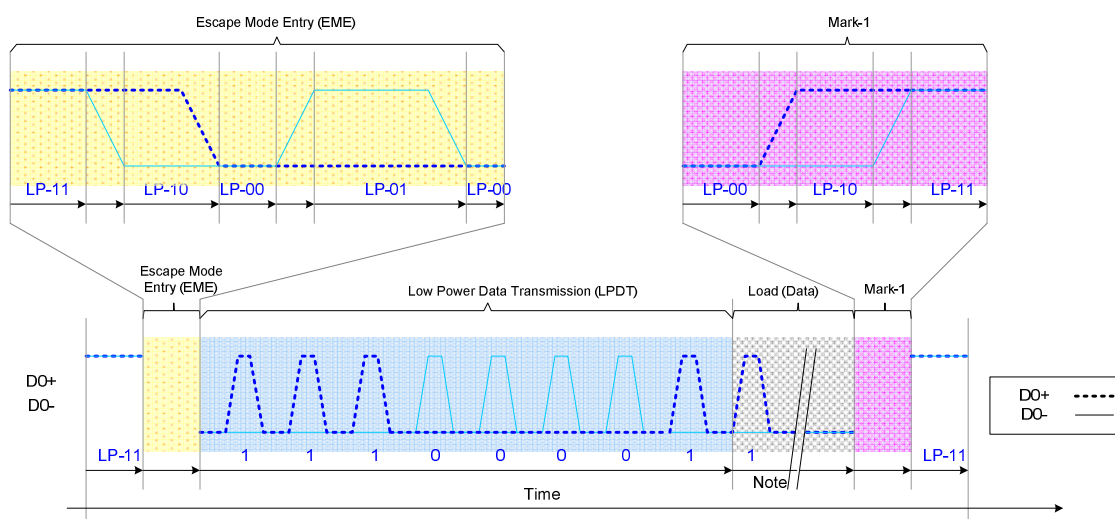


Figure 36: Low-Power Data Transmission (LPDT)^{Note}

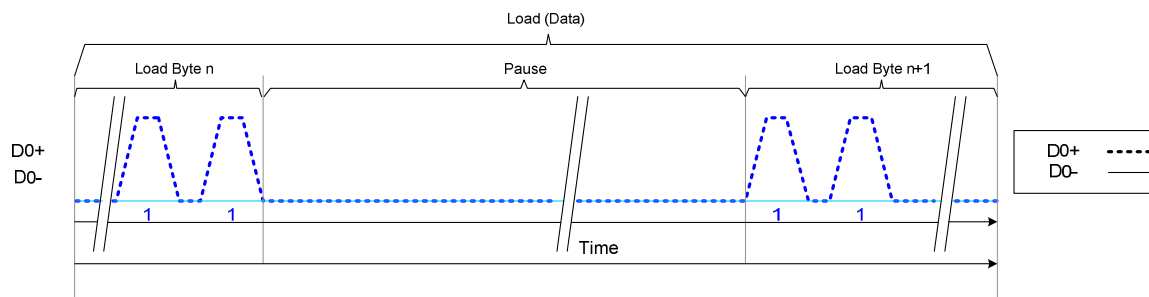


Figure 37: Pause (Example)

^{Note} In this example, load (Data) presents that the first bit is the logical 1.

3.12.12. Ultra-Low Power State (ULPS)

The MPU can force data lanes get into the Ultra-Low Power State (ULPS) mode when data lanes enter the Escape Mode.

The Ultra-Low Power State (ULPS) uses the following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 => LP-10 => LP-00 => LP-01 => LP-00
- Ultra-Low Power State (ULPS) command in the Escape Mode: 0001 1110 (first to last bit)
- Ultra-Low Power State (ULPS) when the MPU keeps data lanes low
- Mark-1: LP-00 => LP-10 => LP-11
- End: LP-11

This sequence is illustrated below for reference purpose:

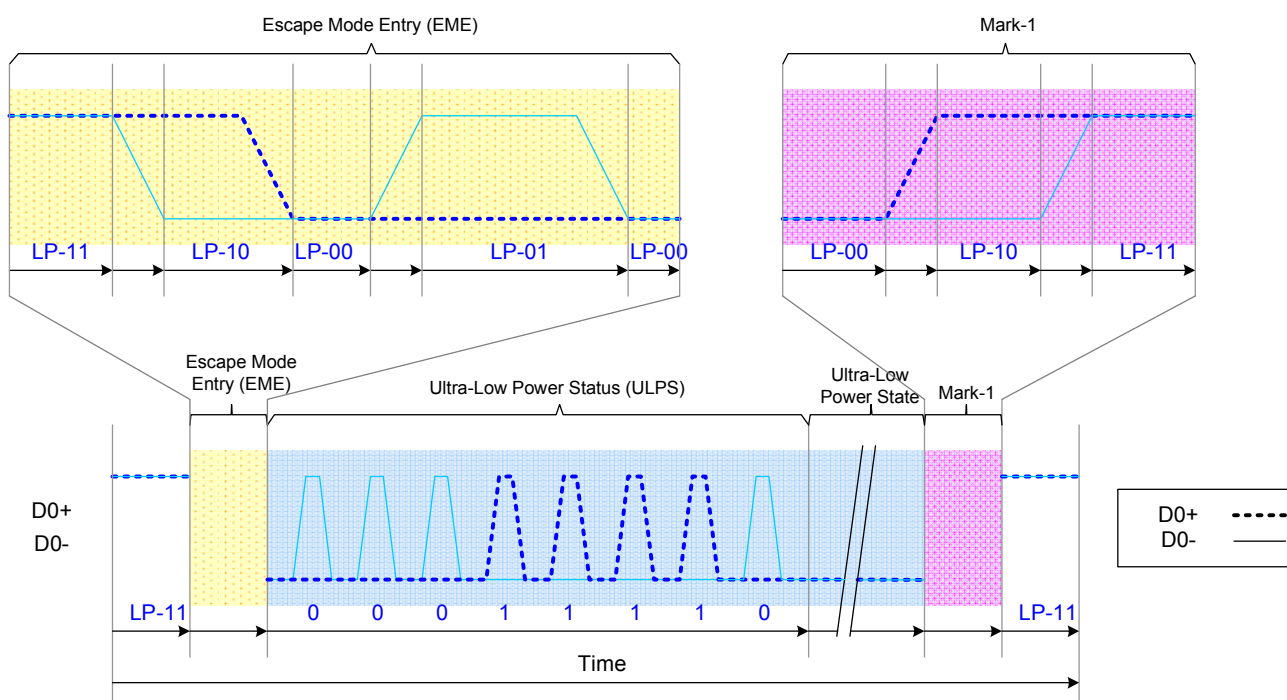


Figure 38: Ultra-Low Power State (ULPS)

3.12.13. Remote Application Reset (RAR)

The MPU can inform the display module that it should be reset in Remote Application Reset (RAR) trigger when data lanes enter the Escape Mode.

The Remote Application Reset (RAR) uses the following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 => LP-10 => LP-00 => LP-01 => LP-00
- Remote Application Reset (RAR) command in the Escape Mode: 0110 0010 (first to last bit)
- Mark-1: LP-00 => LP-10 => LP-11
- End: LP-11

This sequence is illustrated below for reference purpose:

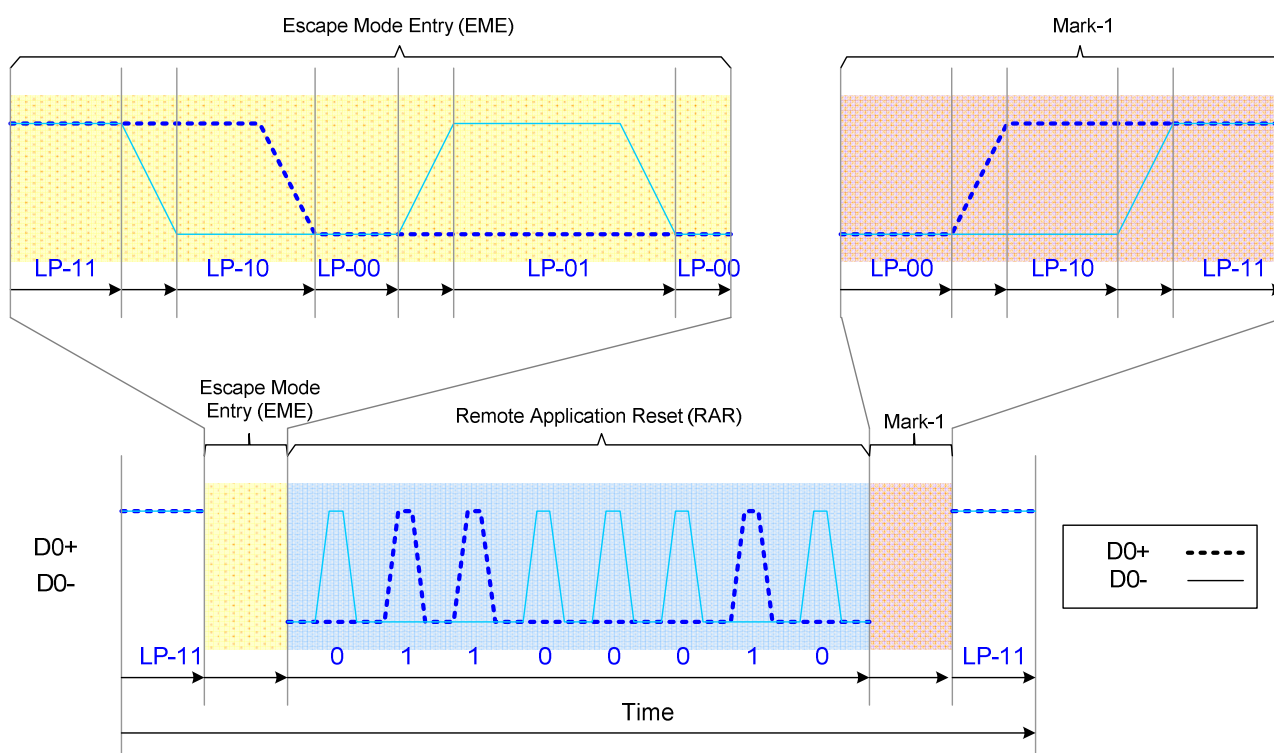


Figure 39: Remote Application Reset (RAR)

3.12.14. Tearing Effect (TEE)

The display module can inform the MPU when a tearing effect event (New V-synch) has happened in the display module by the Tearing Effect (TEE).

The display module sends the Tearing Effect (TEE) with the following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 => LP-10 => LP-00 => LP-01 => LP-00
- Tearing Effect (TEE) trigger in the Escape Mode: 0101 1101 (first to last bit)
- Mark-1: LP-00 => LP-10 => LP-11
- End: LP-11

This sequence is illustrated below for reference purpose:

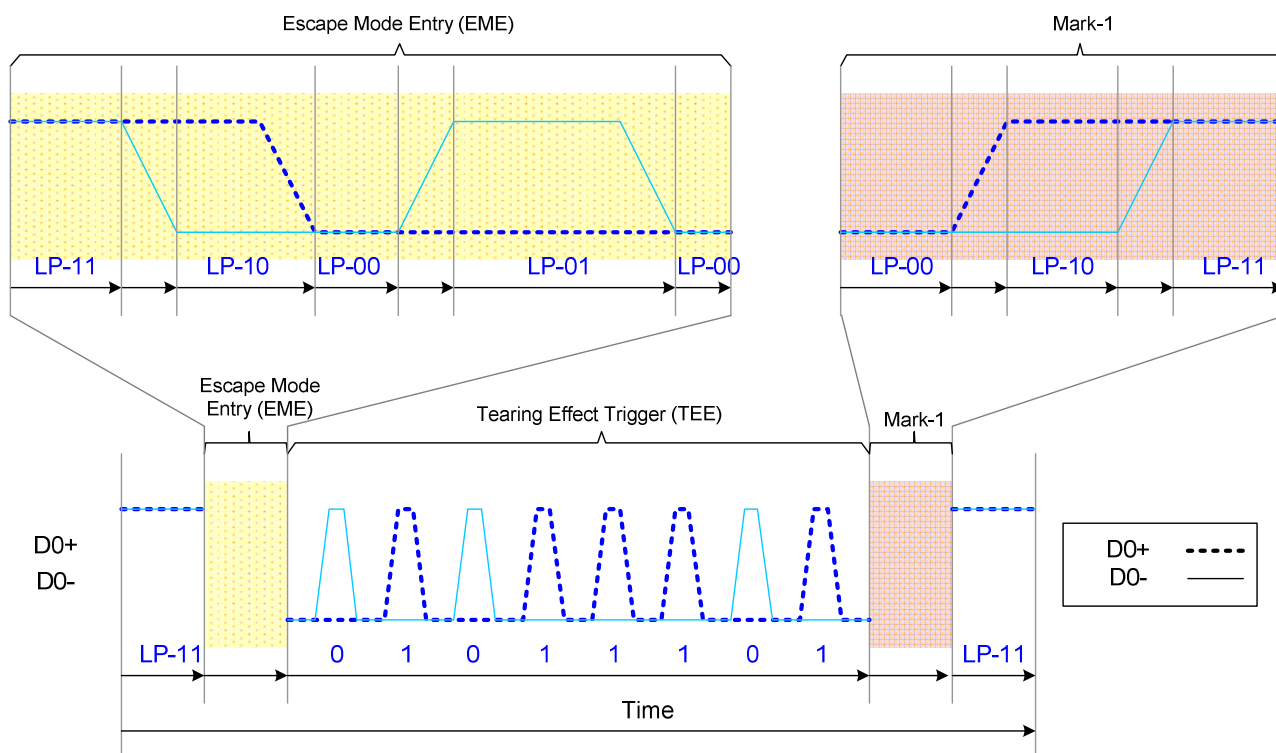


Figure 40: Tearing Effect (TEE)

3.12.15. Acknowledge (ACK)

The display module can inform the MPU that no errors are found by the Acknowledge (ACK).

The display module sends the Acknowledge (ACK) with the following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 => LP-10 => LP-00 => LP-01 => LP-00
- Acknowledge (ACK) command in the Escape Mode: 0010 0001 (first to last bit)
- Mark-1: LP-00 => LP-10 => LP-11
- End: LP-11

This sequence is illustrated below for reference purpose:

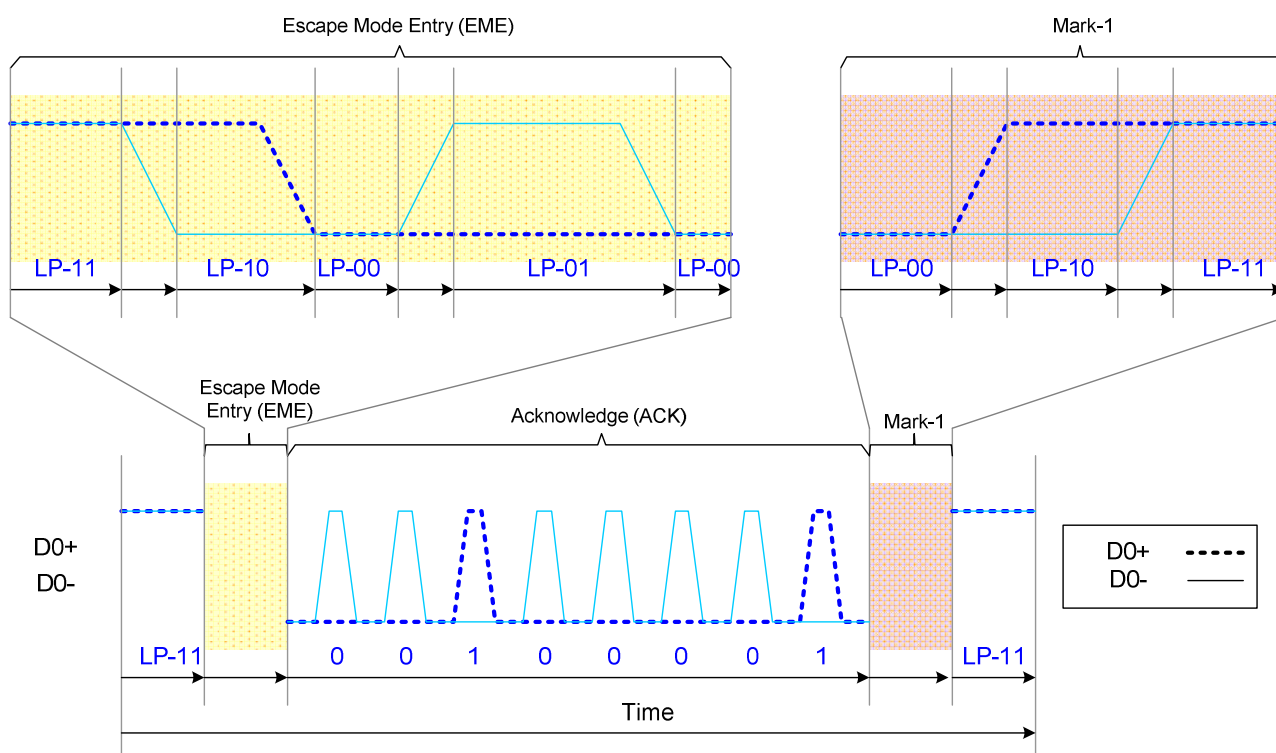


Figure 41: Acknowledge (ACK)

3.12.16. High-Speed Data Transmission (HSDT)

3.12.17. Entering High-Speed Data Transmission (T_{SOT} of HSDT)

The display module enters the High-Speed Data Transmission (HSDT) when Clock lanes DSI-CLK+/- have already entered the High-Speed Clock Mode (HSCM) through the MPU. See more information in the chapter “High-Speed Clock Mode (HSCM)”.

Data lanes DSI-D1+/- and DSI-D0+/- of the display module enter the High-Speed Data Transmission (T_{SOT} of HSDT) with the following sequence:

- Start: LP-11
- HS-Request: LP-01
- HS-Settle: LP-00 => HS-0 (Rx: Lane Termination Enable)
- Rx Synchronization: 011101 (Tx (= MPU) Synchronization: 0001 1101)
- End: High-Speed Data Transmission (HSDT) – Ready to receive High-Speed Data Load

This sequence of entering High-Speed Data Transmission (T_{SOT} of HSDT) is illustrated below:

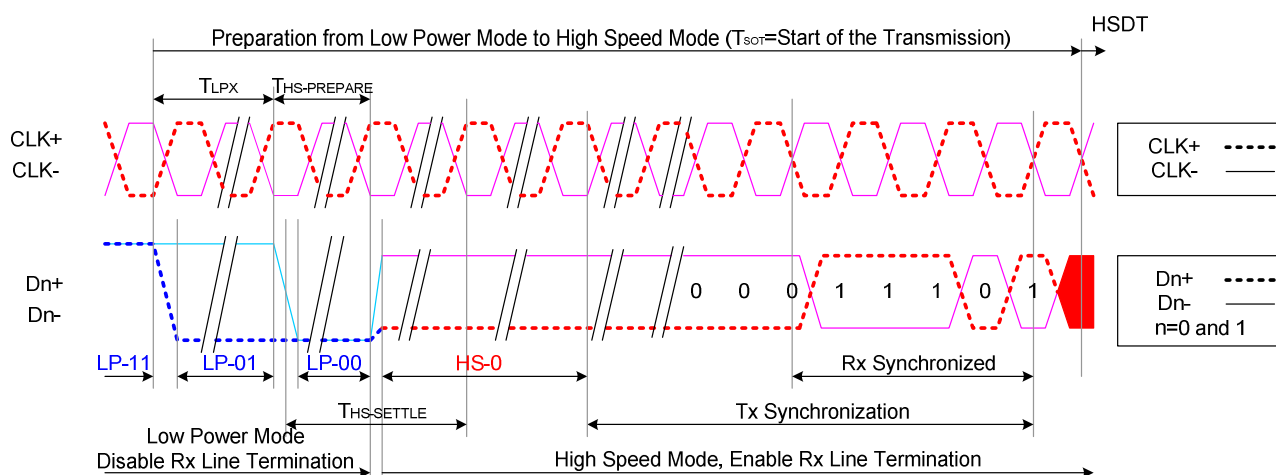


Figure 42: Entering High-Speed Data Transmission (T_{SOT} of HSDT)

3.12.18. Leaving High-Speed Data Transmission (T_{EOT} of HSDT)

The display module leaves the High-Speed Data Transmission (T_{EOT} of HSDT) when Clock lanes DSICLK+/- are in the High-Speed Clock Mode (HSCM) through the MPU. This HSCM is kept until data lanes DSI-D1+/- and DSI-D0+/- are in the LP-11 mode. See more information in the chapter “High-Speed Clock Mode (HSCM)”.

Data lanes DSI-D1+/- and DSI-D0+/- of the display module leave the High-Speed Data Transmission (T_{EOT} of HSDT) with the following sequence:

- Start: High-Speed Data Transmission (HSDT)
- Stops High-Speed Data Transmission
 - o MPU changes to HS-1, if the last load bit is HS-0
 - o MPU changes to HS-0, if the last load bit is HS-1
- End: LP-11 (Rx: Lane Termination Disable)

The sequence of leaving High-Speed Data Transmission (T_{EOT} of HSDT) is illustrated below:

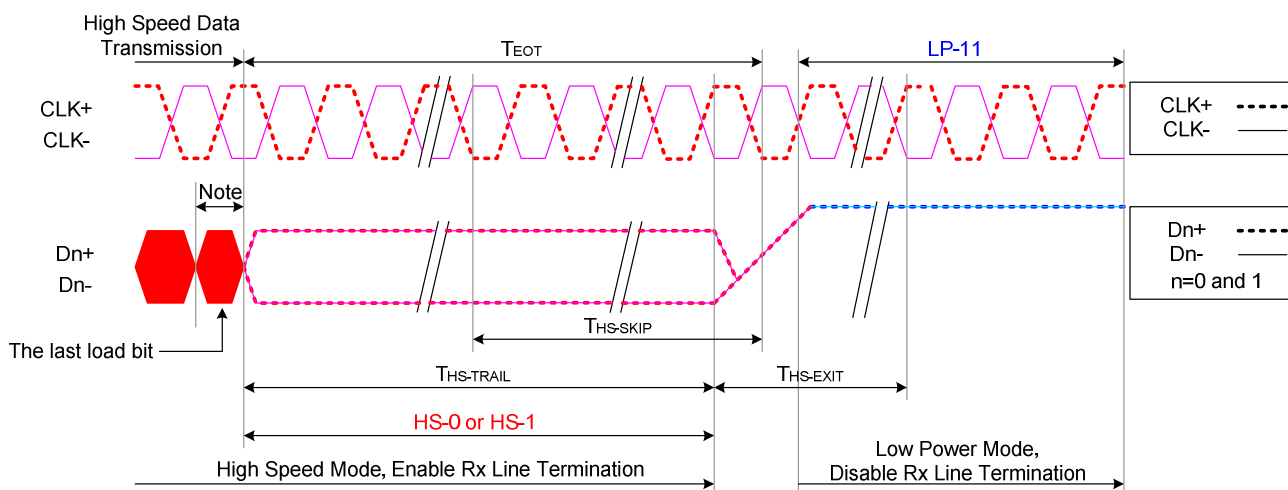


Figure 43: Leaving High-Speed Data Transmission (T_{EOT} of HSDT)^{Note}

^{Note} 1. If the last load bit is HS-0, the transmitter changes from HS-0 to HS-1.
2. If the last load bit is HS-1, the transmitter changes from HS-1 to HS-0.

3.12.19. Burst of the High-Speed Data Transmission (HSDT)

The burst of the “High-Speed Data Transmission” (HSDT) can consist of one data packet or several data packets. These data packets can be Long (LPa) or Short (SPa) packets. These packets are defined in the chapter “Short Packet (SPa) and Long Packet (LPa) Structures”.

These different burst of the High-Speed Data Transmission (HSDT) cases are illustrated below for reference purpose.

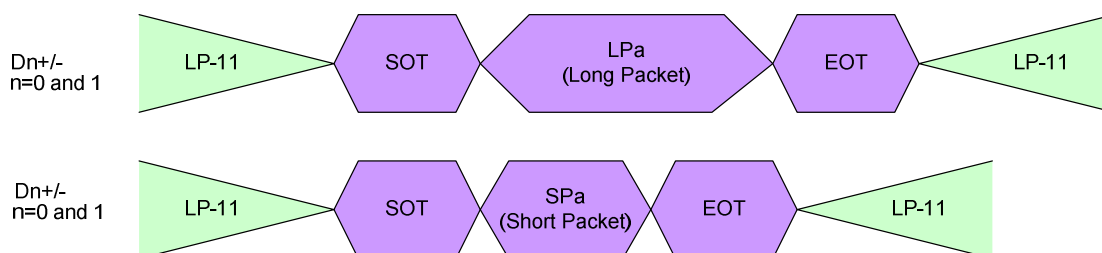


Figure 44: Single Packet in High-Speed Data Transmissions

The multiple packets in High-Speed Data Transmission are illustrated below for reference purposes:

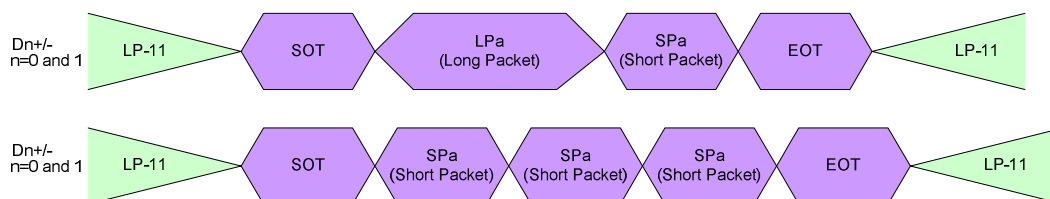


Figure 45: Multiple Packets in High-Speed Data Transmission – Examples

Table 14: Abbreviations

Abbreviation	Explanation
EOT	End of the Transmission
LPa	Long Packet
LP-11	Low Power Mode, Both of Data lanes are 1 (Stop Mode)
SPa	Short Packet
SOT	Start of the Transmission

Byte orders of the sent packet in High-Speed Data Transmission (HSDT) are as follows.

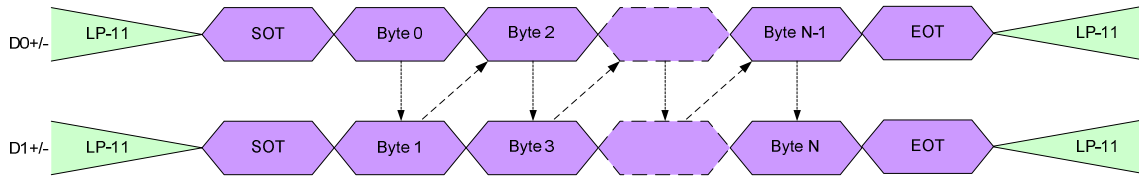


Figure 46: Single Packet in HSDT – Even Number of Bytes

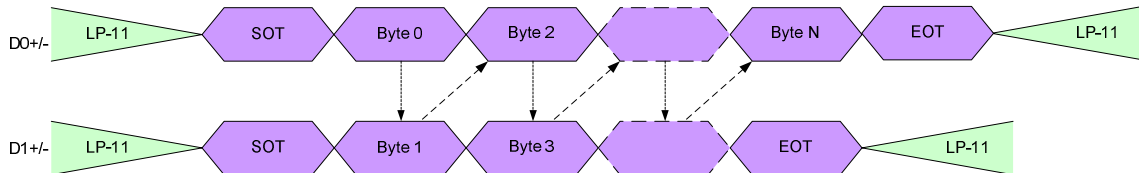


Figure 47: Single Packet in HSDT – Odd Number of Bytes

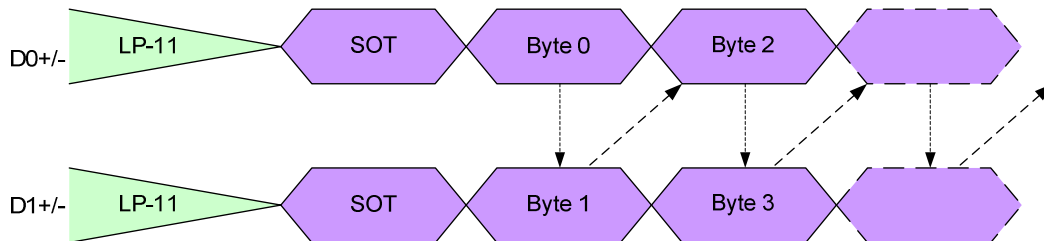


Figure 48: Start of Transmission (SoT) in HSDT for Multiple Packets

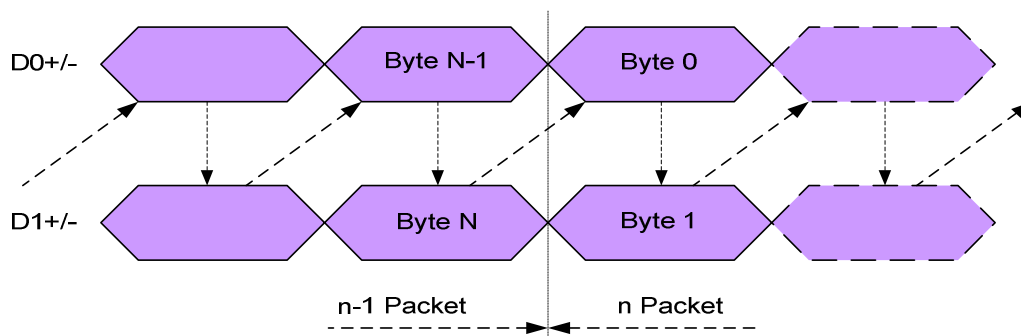


Figure 49: Continuous Multiple Packets in HSDT when Number of Bytes is Equal on Both Data Lanes at the End of the Packet

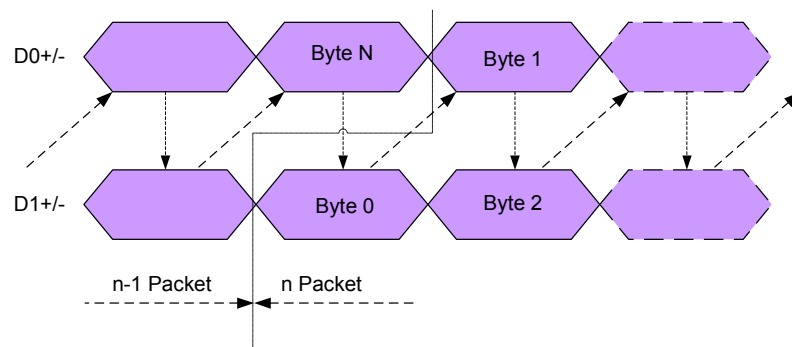


Figure 50: Continuous Multiple Packets in HSDT when Number of Bytes is not Equal on Both Data Lanes at the End of the Packet

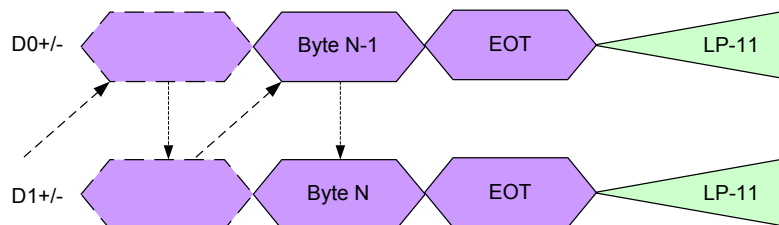


Figure 51: End of Transmission (EoT) in HSDT when Number of Bytes is Equal on Both Data Lanes at the End of the Packet

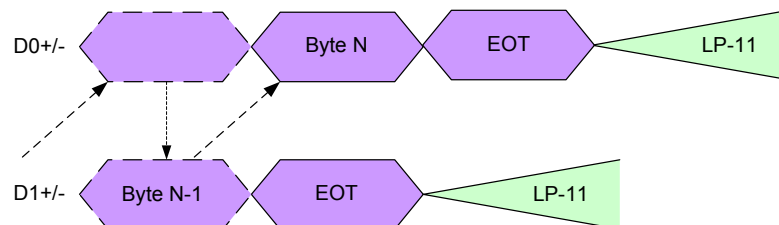


Figure 52: End of Transmission (EoT) in HSDT when Number of Bytes is not Equal on Both Data Lanes at the End of the Packet

3.12.20. Bus Turnaround (BTA)

The MPU or the display module, which controls DSI-D0+/- Data Lanes, can start a bus turnaround procedure when it requires information from a receiver, which can be the MPU or the display module.

The MPU and the display module use the same sequence when this bus turnaround procedure is applied. The sequence when the MPU wants to perform the bus turnaround procedure to the display module is described below for reference purpose:

- Start (MPU): LP-11
- Turnaround Request (MPU): LP-11 => LP-10 => LP-00 => LP-10 => LP-00
- The MPU waits until the display module starts to control DSI-D0+/- data lanes and the MPU stops to control DSI-D0+/- data lanes (= High-Z)
- The display module changes to the stop mode: LP-00 => LP-10 => LP-11

The same bus turnaround procedure (from the MPU to the display module) is illustrated below:

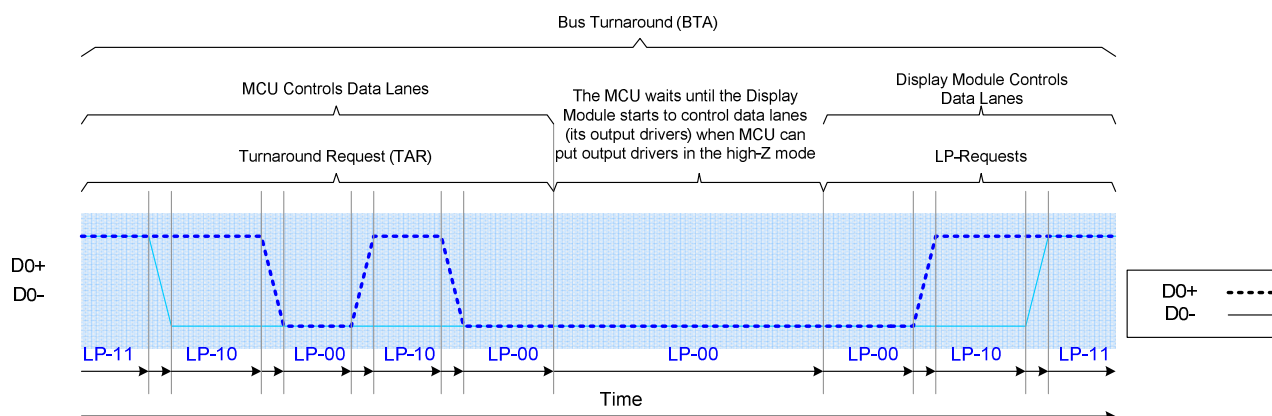


Figure 53: Bus Turnaround Procedure

The MPU and the display module can be switched in Figure 53: Bus Turnaround Procedure, if the Bus Turnaround (BTA) is from the display module to the MPU.

3.12.21. Packet Level Communication

3.12.22. Short Packet (SPa) and Long Packet (LPa) Structures

Short Packets (SPa) and Long Packets (LPa) can always be used when data transmission is done in Low Power Data Transmission (LPDT) or High-Speed Data Transmission (HSDT) modes^{Note}.

The lengths of the packets are:

- Short Packet (SPa): 4 bytes
- Long Packet (LPa): 6 to 65,541 bytes

The type of the packet (SPa or LPa) can be recognized from their packet headers (PH).

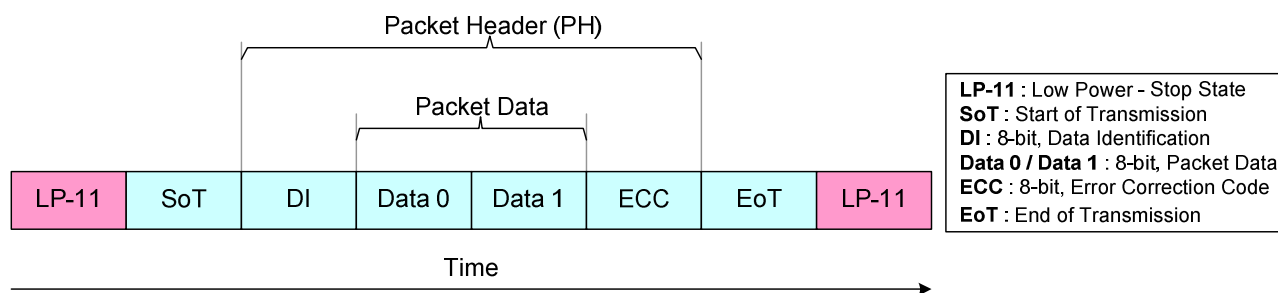


Figure 54: Short Packet (SPa) Structure

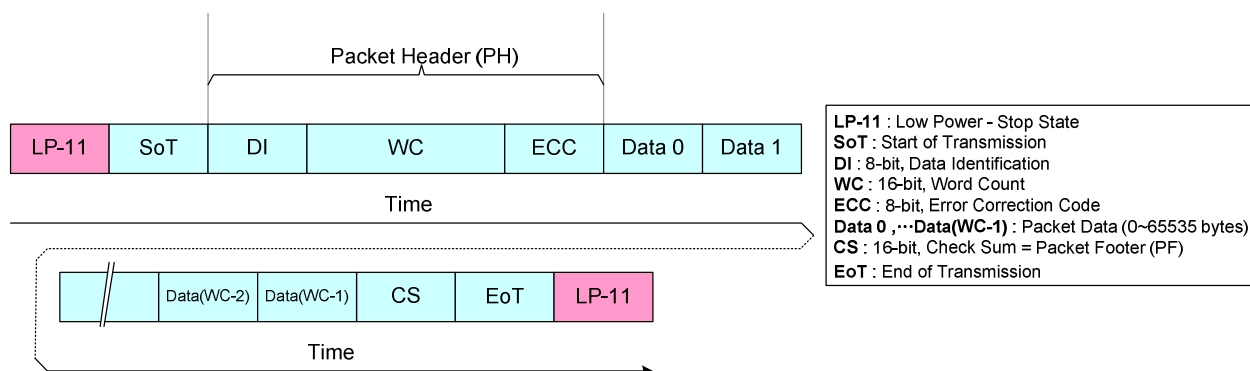


Figure 55: Long Packet (LPa) Structure

^{Note} Short Packet (SPa) and Long Packet (LPa) present a single packet sending (= including LP-11, SoT, and EoT for each packet sending).

The other possibility is that SoT, EoT and LP-11 between packets are not necessary if packets are sent in multiple packet formats, for example:

- LP-11 => SoT => SPa => LPa => SPa => SPa => EoT => LP-11
- LP-11 => SoT => SPa => SPa => SPa => EoT => LP-11
- LP-11 => SoT => LPa => LPa => LPa => EoT => LP-11

3.12.23. Bit Transmission Order of Bytes in Packets

The bit transmission order in a byte, which is used in packets, is that the Least Significant Bit (LSB) of a byte is sent first and the Most Significant Bit (MSB) of a byte is sent last.

This transmission order is illustrated below for reference purpose.

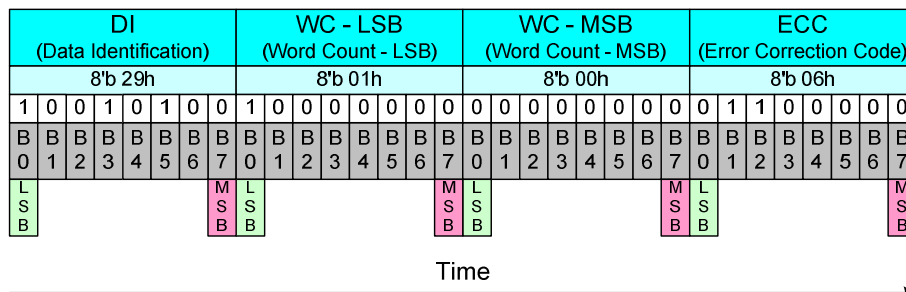


Figure 56: Bit Transmission Order of Bytes in Packets

3.12.24. Byte Transmission Order of Multiple-Byte Information in Packets

The byte transmission order of the multiple-byte information, what is used in packets, is that the Least Significant (LS) Byte of the information is sent first and the Most Significant (MS) Byte of the information is sent last. For example, Word Count (WC) consists of 2 bytes (16 bits); the LS byte is sent first and the MS byte is sent last.

This transmission order is illustrated below for reference purpose.

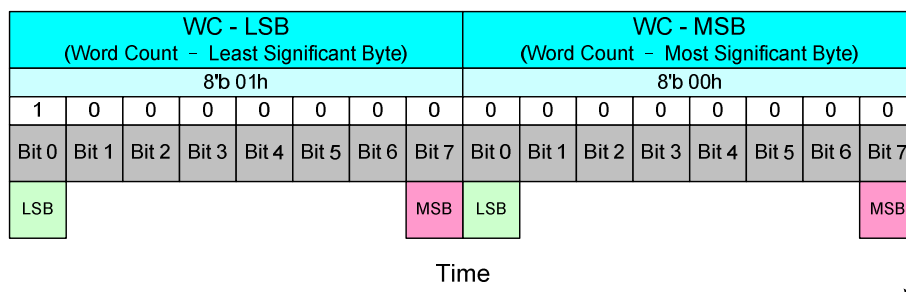


Figure 57: Byte Transmission Order of the Multiple-Byte Information in Packets

3.12.25. Packet Header (PH)

The packet header always consists of 4 bytes. The content of these 4 bytes are different for Short Packets (SPa) and Long Packets (LPa).

Short Packet (SPa)

- 1st byte: Data Identification (DI) => identify that this is a Short Packet (SPa)
- 2nd and 3rd bytes: Packet Data (PD), Data 0 and 1
- 4th byte: Error Correction Code (ECC)

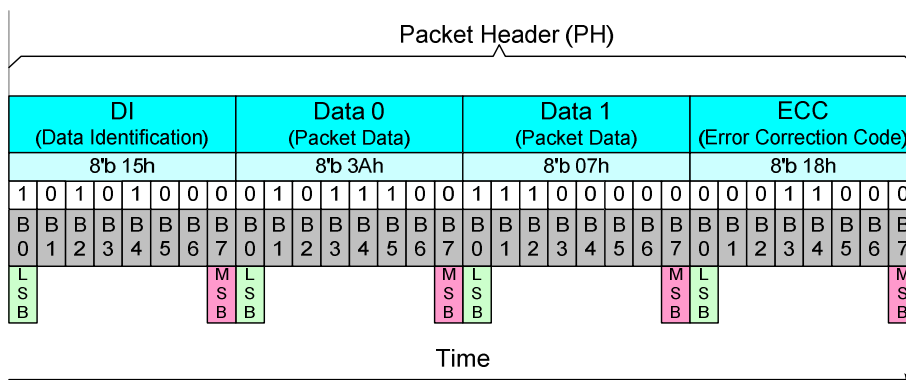


Figure 58: Packet Header (PH) of a Short Packet (SPa)

Long Packet (LPa)

- 1st byte: Data Identification (DI) => identify that this is a Long Packet (LPa)
- 2nd and 3rd bytes: Word Count (WC)
- 4th byte: Error Correction Code (ECC)

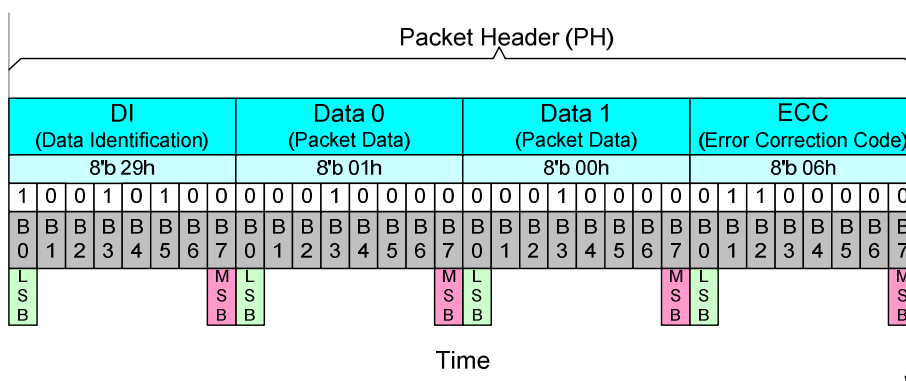


Figure 59: Packet Header (PH) on Long Packet (LPa)

3.12.26. Data Identification (DI)

Data Identification (DI) is a part of the Packet Header (PH) and it consists of 2 parts:

- Virtual Channel (VC), 2 bits, DI [7...6]
- Data Type (DT), 6 bits, DI [5...0]

The Data Identification (DI) structure is illustrated in the figure below.

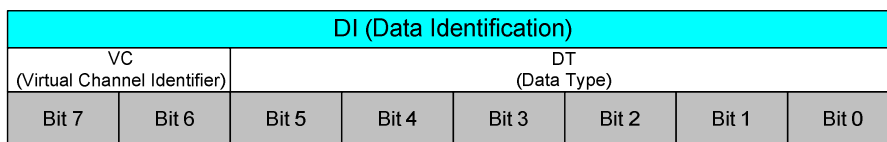


Figure 60: Data Identification (DI) Structure

Data Identification (DI) is illustrated in the Packet Header (PH) below for reference purpose.

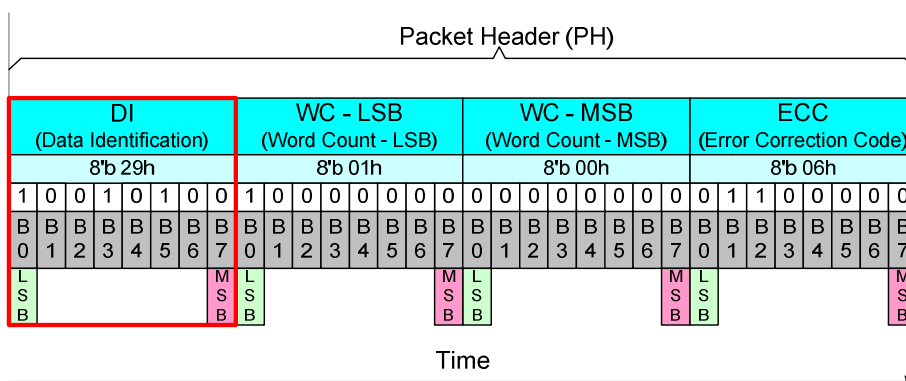


Figure 61: Data Identification (DI) in the Packet Header (PH)

3.12.27. Virtual Channel (VC)

Virtual Channel (VC) is a part of the Data Identification (DI [7...6]) structure and it is used to indicate where a packet is to be sent from the MPU.

Bits of the Virtual Channel (VC) are illustrated below for reference purpose.

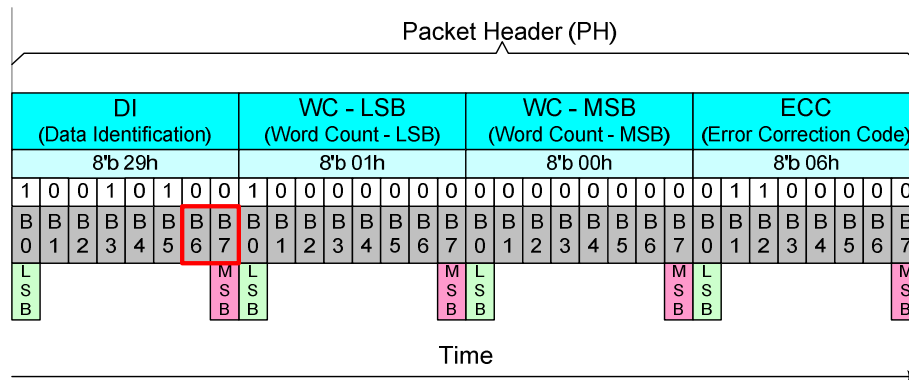


Figure 62: Virtual Channel (VC) on the Packet Header (PH)

Virtual Channel (VC) can assign 4 different channels to 4 different display modules. Devices use the same virtual channel as which the MPU uses to send packets to them, for example,

- The MPU uses the virtual channel 0 when it sends packets to ILI9806G
- ILI9806G also uses the virtual channel 0 when it sends packets to the MPU

This functionality is illustrated below.

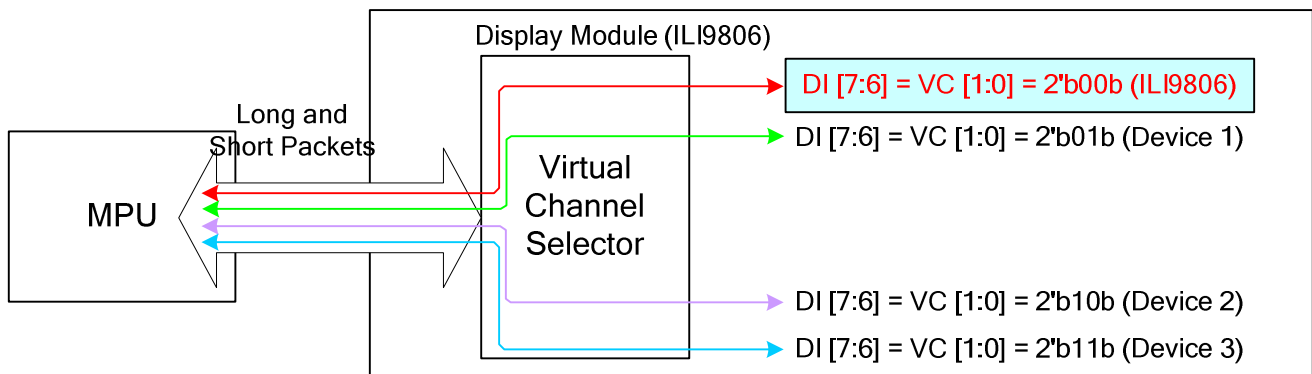


Figure 63: Virtual Channel (VC) Configuration

Virtual Channel (VC) is always 0 (DI [7..6] = VC [1..0] = 00b) when the MPU sends the End of Transmission Packet to the display module. See the chapter “End of Transmission Packet (EoTP)”.

This display module does not support the virtual channel selector for other devices (1 to 3) when the only possible virtual channel (VC [1..0]) is 00b for this display module.

3.12.28. Data Type (DT)

Data Type (DT) is a part of the Data Identification (DI [5...0]) structure and it is used to define the type of the used data in a packet.

Bits of the Data Type (DT) are illustrated below for reference purpose.

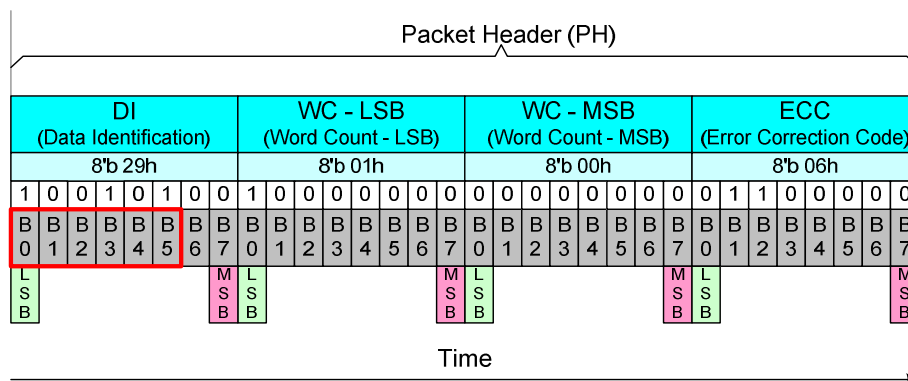


Figure 64: Data Type (DT) in the Packet Header (PH)

This Data Type (DT) also defines the used packet is Short Packet (SPa) or Long Packet (LPa). Data Types (DT) are different from the MPU to the display module (or other devices) and vice versa.

These Data Types (DT) are defined in the tables below.

Table 15: Data Types (DT) from the MPU to the Display Module (ILI9806G)

From the MPU to the Display Module (ILI9806G)									
Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex	Description	Short/Long Packet	Abbreviation
0	0	1	0	0	0	08	End of Transmission Packet, ^{Note 1}	SPa (Short Packet)	EoTP
0	0	0	1	0	1	05	DCS Write, No Parameter	SPa (Short Packet)	DCSWN-S
0	1	0	1	0	1	15	DCS Write, 1 Parameter	SPa (Short Packet)	DCSW1-S
0	0	0	1	1	0	06	DCS Read, No Parameter	SPa (Short Packet)	DCSRN-S
1	1	0	1	1	1	37	Set Maximum Return Packet Size	SPa (Short Packet)	SMRPS-S
0	0	1	0	0	1	09	Null Packet, No Data, ^{Note 2}	LPa (Long Packet)	NP-L
1	1	1	0	0	1	39	DCS Write Long	LPa (Long Packet)	DCSW-L

^{Note 1} This can be used when the MPU wants to make sure that it is the end of the transmission in the High Speed Data Transferring (HSDT) mode.

^{Note 2} This can be used when data lanes are to be kept in the High Speed Data Transferring (HSDT) Mode.

Table 16: Data Types (DT) from the Display Module (ILI9806G) to the MPU

From the Display Module (ILI9806G) to the MPU									
Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex	Description	Short/Long Packet	Abbreviation
0	0	0	0	1	0	02	Acknowledge with Error Report	SPa (Short Packet)	AwER
0	1	1	1	0	0	1C	DCS Read Long Response	LPa (Long Packet)	DCSRR-L
1	0	0	0	0	1	21	DCS Read Short Response, 1 byte returned	SPa (Short Packet)	DCSRR1-S
1	0	0	0	1	0	22	DCS Read Short Response, 2 byte returned	SPa (Short Packet)	DCSRR2-S

The receiver will ignore other Data Types (DT) if they are not defined in the “Table 15: Data Type (DT) from the MPU to the Display Module (or Other Devices)” or “Table 16: Data Type (DT) from the Display Module (or Other Devices) to the MPU”.

3.12.29. Packet Data (PD) of a Short Packet (SPa)

Packet Data (PD) of a Short Packet (SPa) is defined after Data Type (DT) of the Data Identification (DI), which indicates that a Short Packet (SPa) is to be sent.

Packet Data (PD) of a Short Packet (SPa) consists of 2 data bytes: Data 0 and Data 1.

The sending order of Packet Data (PD) is that Data 0 is sent first and the Data 1 is sent last.

Bits of Data 1 are set to 0 if the information length is 1 byte.

Packet Data (PD) of a Short Packet (SPa), when the length of the information is 1 or 2 bytes and Virtual Channel (VC) is 0, are illustrated below for reference purpose.

Packet Data (PD) information:

- Data 0: 35hex (Display Command Set (DCS) with 1 Parameter => DI (Data Type (DT)) = 15hex)
- Data 1: 01hex (DCS's parameter)

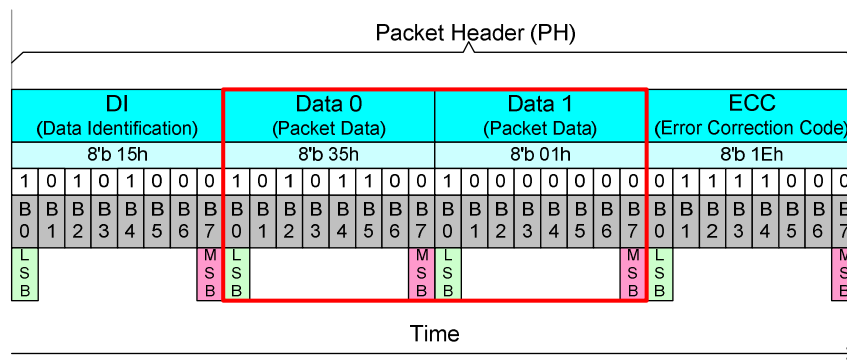


Figure 65: Packet Data (PD) of a Short Packet (SPa), 2 Bytes Information

Packet Data (PD) information:

- Data 0: 10hex (DCS without parameter => DI (Data Type (DT)) = 05hex)
- Data 1: 00hex (Null)

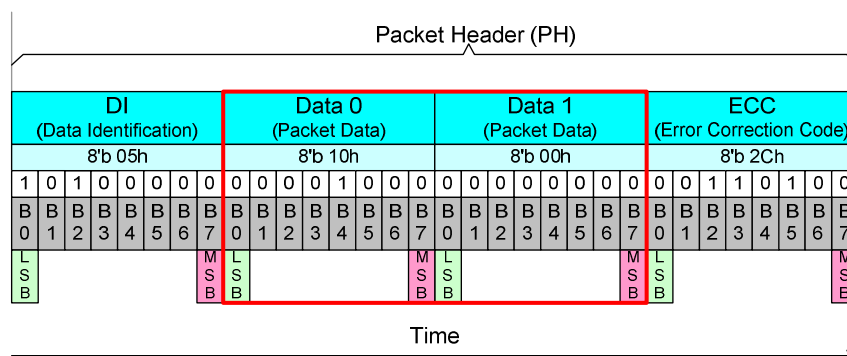


Figure 66: Packet Data (PD) of a Short Packet (SPa), 1 Byte Information

3.12.30. Word Count (WC) of a Long Packet (LPa)

Word Count (WC) of a Long Packet (LPa) is defined after Data Type (DT) of the Data Identification (DI), which indicates that Long Packet (LPa) is to be sent.

Word Count (WC) indicates the amount of data bytes of the Packet Data (PD) which are to be sent after the Packet Header (PH). The location of Word Count (WC) in a Long Packet is the same as which of Packet Data (PD) in a Short Packet.

Word Count (WC) of a Long Packet (LPa) consists of 2 bytes.

The sending order of these 2 bytes of the Word Count (WC) is that the Least Significant (LS) Byte is sent first and the Most Significant (MS) Byte is sent last.

Word Count (WC) of a Long Packet (LPa) is illustrated below for reference purposes.

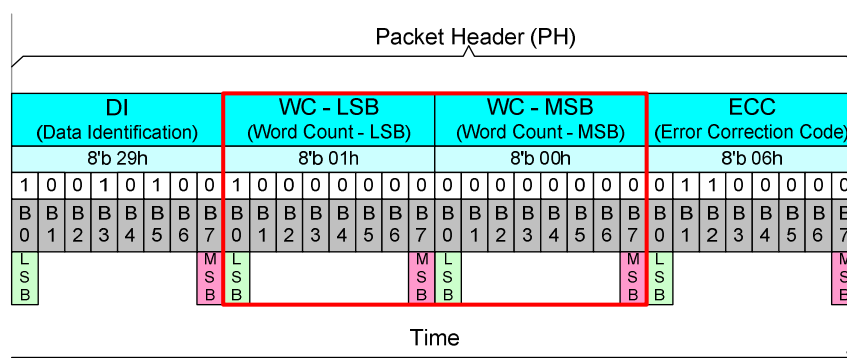


Figure 67: Word Count (WC) of a Long Packet (LPa)

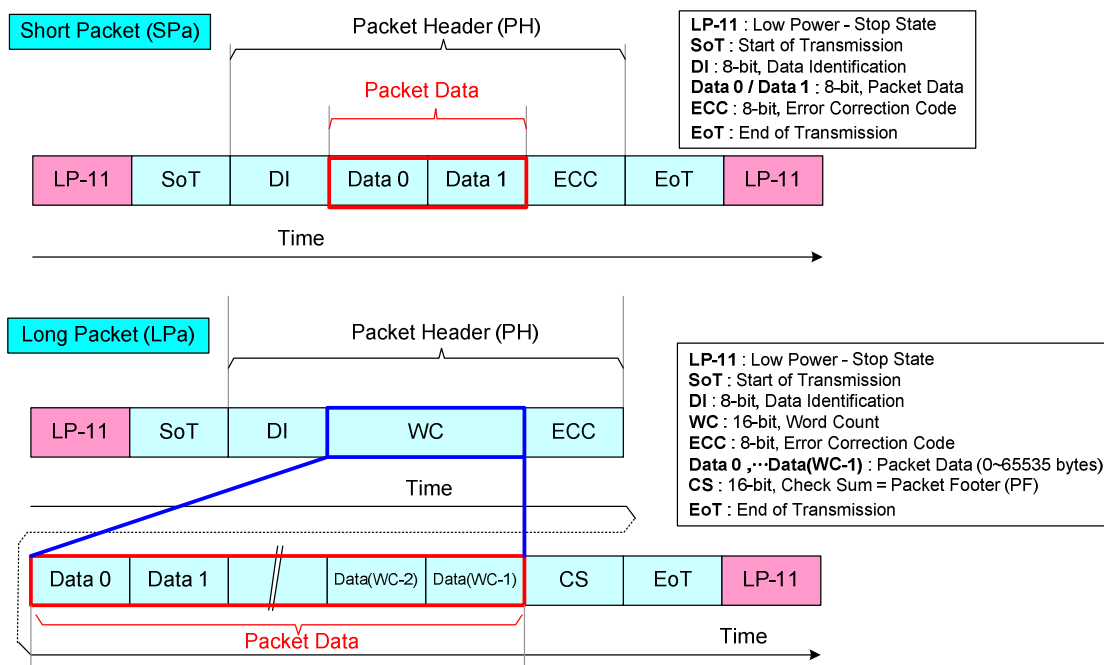


Figure 68: Packet Data in Short and Long Packets

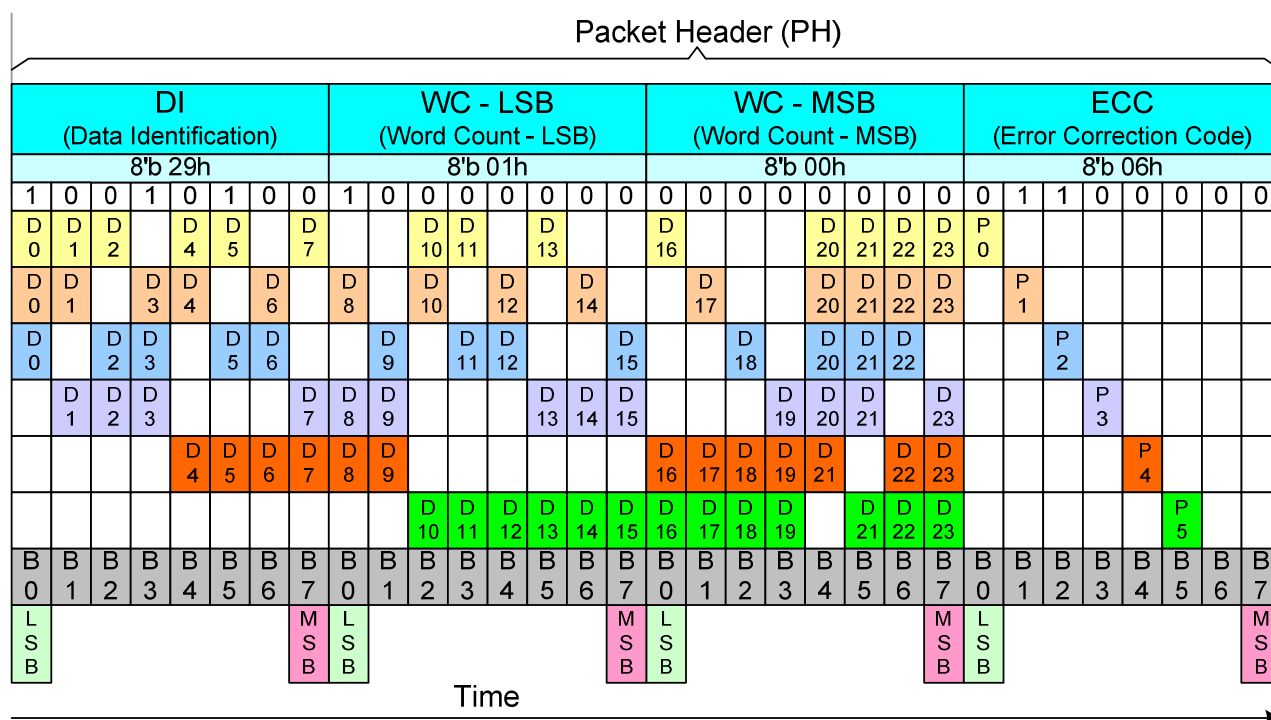


Figure 72: XOR Functionality in a Long Packet (LPa)

The transmitter (the MPU or the Display Module) sends data bits D [23...0] and Error Correction Code (ECC) P [7...0]. The receiver (the Display module or the MPU) calculates an Internal Error Correction Code (IECC) and compares the received Error Correction Code (ECC) and the Internal Error Correction Code (IECC). This comparison is done when each power bit of ECC and IECC have performed the XOR function. The result of this function is PO [7...0]. This functionality, where the transmitter is the MPU and the receiver is the display module, is illustrated below for reference purposes.

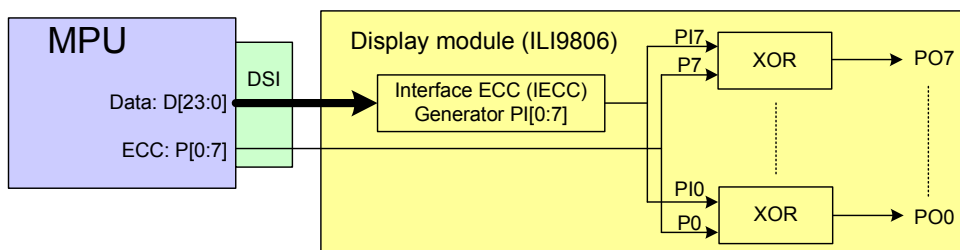


Figure 73: Internal Error Correction Code (IECC) on the Display Module (the Receiver)

The sent data bits (D [23...0]) and ECC (P [7...0]) are received correctly, if the value of the PO [7...0] is 00h.

The sent data bits (D [23...0]) and ECC (P [7...0]) are not received correctly, if the value of the PO [7...0] is not 00h.

ECC P[7...0]	1	1	0	0	0	0	0	0	03h
IECC PI[7...0]	1	1	0	0	0	0	0	0	03h
XOR(ECC, IECC) => PO[7...0]	0	0	0	0	0	0	0	0	= 00h => No Error
	L							M	
	S							S	
	B							B	

Figure 74: Internal XOR Calculation between ECC and IECC Values – No Error

ECC P[7...0]	1	1	0	0	0	0	0	0	03h
IECC PI[7...0]	1	1	1	1	0	0	0	0	0Fh
XOR(ECC, IECC) => PO[7...0]	0	0	1	1	0	0	0	0	= 0Ch => Error
	L							M	
	S							S	
	B							B	

Figure 75: Internal XOR Calculation between ECC and IECC Values - Error

The received Error Correction Code (ECC) can be 00h when the Error Correction Code (ECC) functionality is not used for data values D [23...0] on the transmitter side.

The amount of the errors (one or more) can be defined when the value of the PO [7...0] is compared to the values in the following table.

Table 17: One Bit Error Value of the Error Correction Code (ECC)

Data Bit	PO7	PO6	PO5	PO4	PO3	PO2	PO1	PO0	Hex
D [0]	0	0	0	0	0	1	1	1	07h
D [1]	0	0	0	0	1	0	1	1	0Bh
D [2]	0	0	0	0	1	1	0	1	0Dh
D [3]	0	0	0	0	1	1	1	0	0Eh
D [4]	0	0	0	1	0	0	1	1	13h
D [5]	0	0	0	1	0	1	0	1	15h
D [6]	0	0	0	1	0	1	1	0	16h
D [7]	0	0	0	1	1	0	0	1	19h
D [8]	0	0	0	1	1	0	1	0	1Ah
D [9]	0	0	0	1	1	1	0	0	1Ch
D [10]	0	0	1	0	0	0	1	1	23h
D [11]	0	0	1	0	0	1	0	1	25h
D [12]	0	0	1	0	0	1	1	0	26h
D [13]	0	0	1	0	1	0	0	1	29h
D [14]	0	0	1	0	1	0	1	0	2Ah
D [15]	0	0	1	0	1	1	0	0	2Ch
D [16]	0	0	1	1	0	0	0	1	31h
D [17]	0	0	1	1	0	0	1	0	32h
D [18]	0	0	1	1	0	1	0	0	34h
D [19]	0	0	1	1	1	0	0	0	38h
D [20]	0	0	0	1	1	1	1	1	1Fh
D [21]	0	0	1	0	1	1	1	1	2Fh
D [22]	0	0	1	1	0	1	1	1	37h
D [23]	0	0	1	1	1	0	1	1	3Bh

One error is detected if the value of the PO [7...0] is found in Table 17: One Bit Error Value of the Error Correction Code (ECC), and the receiver can correct this one-bit error because this found value also defines the location of the corrupt bit, for example,

- PO [7...0] = 0Eh
- The bit of the data (D [23...0]), which is not correct, is D [3]

More than one error is detected if the value of the PO [7...0] is not in Table 17: One Bit Error Value of the Error Correction Code (ECC), for example, PO [7...0] = 0Ch.

3.12.32. Packet Data (PD) of a Long Packet (LPa)

Packet Data (PD) of a Long Packet (LPa) is defined after the Packet Header (PH) of the Long Packet (LPa).

The amount of data bytes is defined in the chapter "Word Count (WC) of a Long Packet (LPa)".

3.12.33. Packet Footer (PF) of a Long Packet (LPa)

The Packet Footer (PF) of a Long Packet (LPa) is defined after the Packet Data (PD) of a Long Packet (LPa). The Packet Footer (PF) is the checksum value which is calculated from the Packet Data of the Long Packet (LPa).

The checksum uses a 16-bit Cyclic Redundancy Check (CRC) value which is generated by a polynomial $X^{16}+X^{12}+X^5+X^0$, as illustrated below.

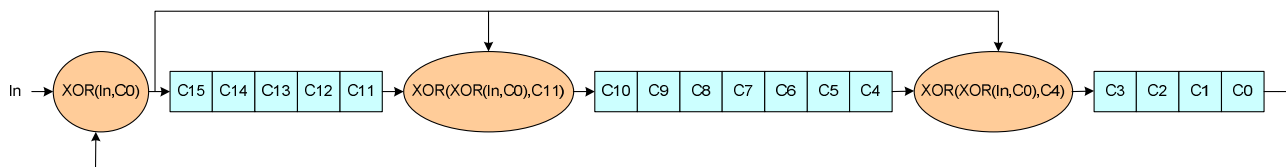


Figure 76: 16-bit Cyclic Redundancy Check (CRC) Calculation

The 16-bit Cyclic Redundancy Check (CRC) generator is initialized to FFFFh before calculations.

The Most Significant Bit (MSB) of the data byte of the Packet Data (PD) is the first bit to be inputted into the 16-bit Cyclic Redundancy Check (CRC).

An example of the 16-bit Cyclic Redundancy Check (CRC), where the Packet Data (PD) of the Long Packet (LPa) is 01h, is illustrated (step-by-step) below.

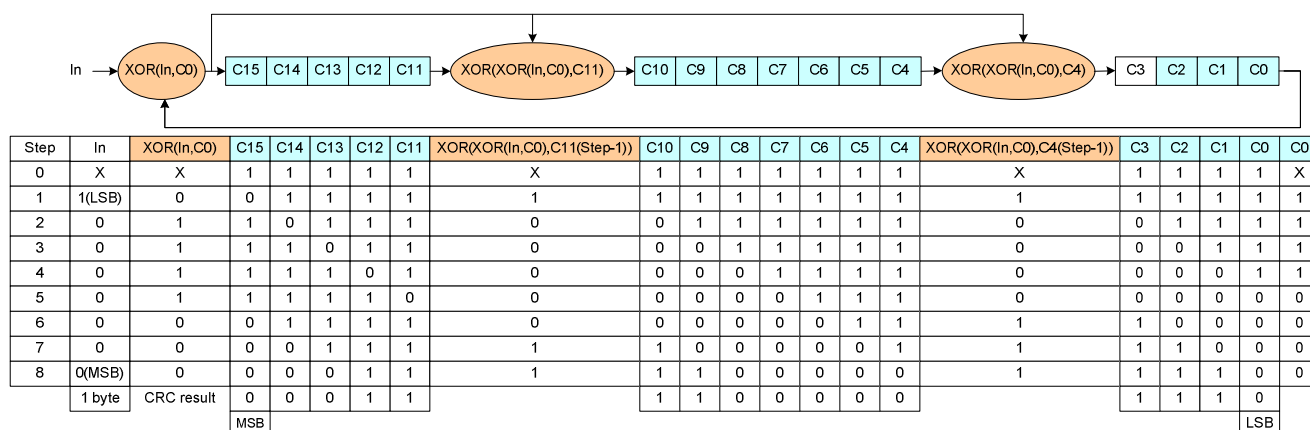


Figure 77: CRC Calculation – Packet Data (PD) is 01h

The value of the Packet Footer (PF) is 1E0Eh in this example. This example (command 01h has been sent) is illustrated below.

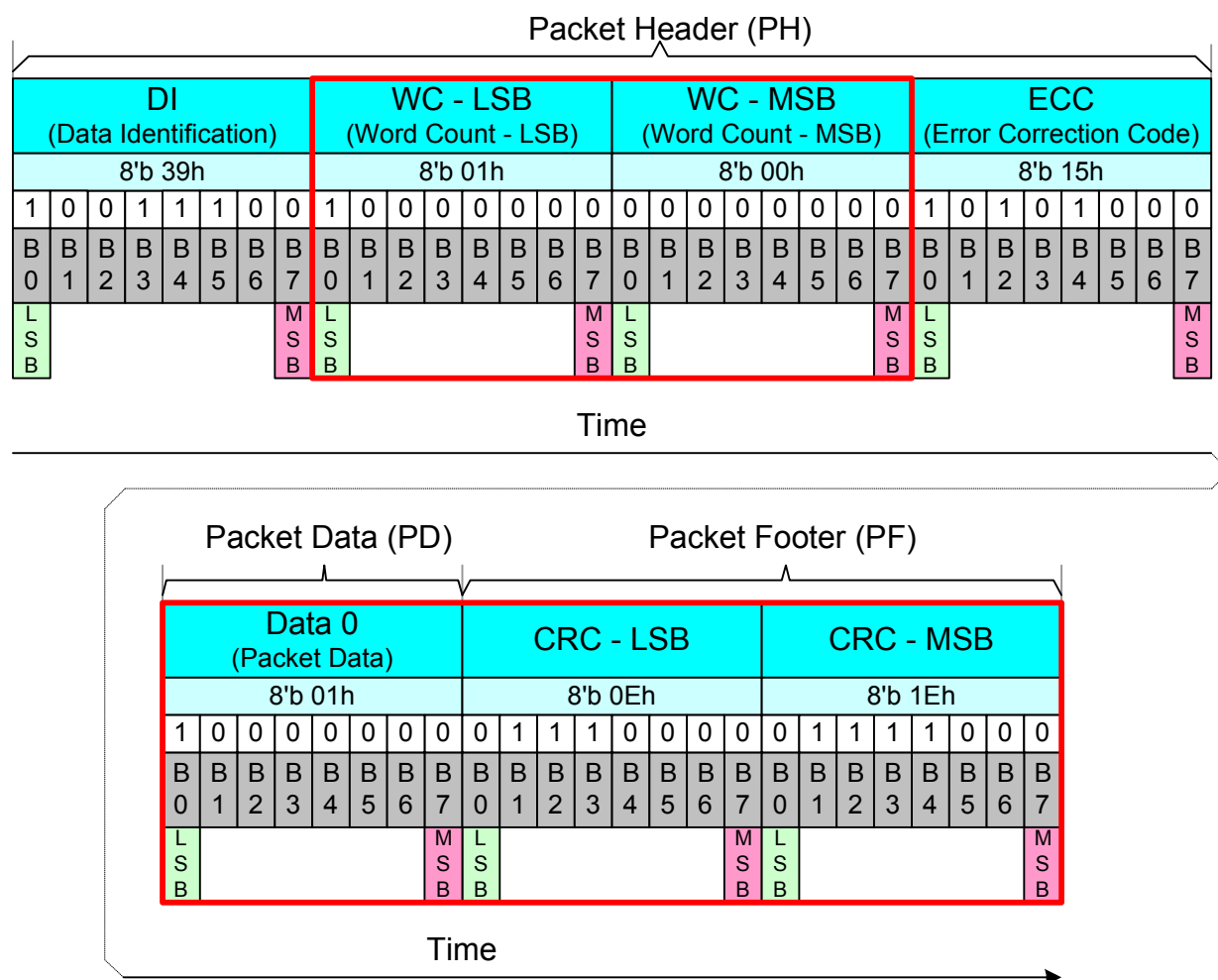


Figure 78: Packet Footer (PF) Example

The receiver calculates its own checksum value from the received Packet Data (PD). The receiver compares its own checksum with the Packet Footer (PF) which the transmitter has sent.

The received Packet Data (PD) and Packet Footer (PF) are correct if the checksums of the receiver and Packet Footer (PF) are equal. The received Packet Data (PD) and Packet Footer (PF) are not correct if the checksums of the receiver and Packet Footer (PF) are not equal.

3.12.34. Packet Transmissions

3.12.35. Packet from the MPU to the Display Module

3.12.36. Display Command Set (DCS)

Display Command Set (DCS), which is defined in the Chapter 4.2 Command Description, is transmitted from the MPU to the display module. This Display Command Set (DCS) is always defined in the Data 0 of the Packet Data (PD), which is included in a Short Packet (SPa) and a Long packet (LPa), as illustrated below.

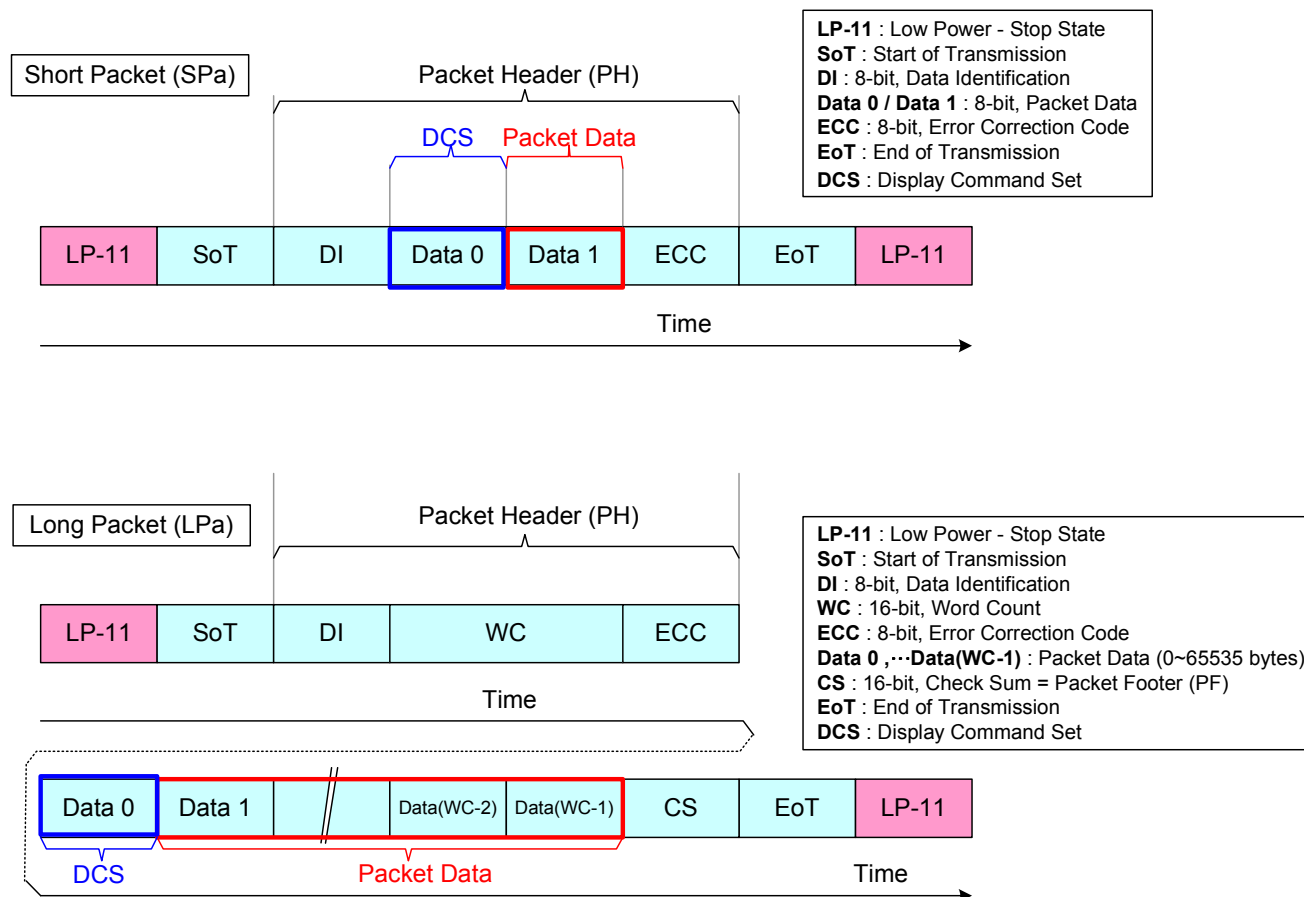


Figure 79: Display Command Set (DCS) in Short Packet (SPa) and Long Packet (LPa)

3.12.37. Display Command Set (DCS) Write, No Parameter (DCSWN-S)

“Display Command Set (DCS) Write, No Parameter” is always used in a Short Packet (SPa), which is defined in the Data Type (DT, 00 0101b), from the MPU to the display module. These commands are defined in the table below. (See Chapter 5.2: Command Description.)

Table 18: Display Command Set (DCS) Write, No Parameters (DCSWN-S)

Command
NOP (00h)
Software Reset (01h)
Sleep In(10h)
Sleep Out (11h)
Partial Mode On (12h)
Normal Display Mode On (13h)
All Pixel Off (22h)
All Pixel On (23h)
Display Off (28h)
Display ON (29h)
Tearing Effect Line OFF (34h)
Idle Mode Off (38h)
Idle Mode On (39h)

A Short Packet (SPa) is defined as:

- Data Identification (DI)
 - o Virtual Channel (VC, DI [7...6]): 00b
 - o Data Type (DT, DI [5...0]): 00 0101b
- Packet Data (PD)
 - o Data 0: “Sleep In (10h)”, Display Command Set (DCS)
 - o Data 1: Always 00hex
- Error Correction Code (ECC)

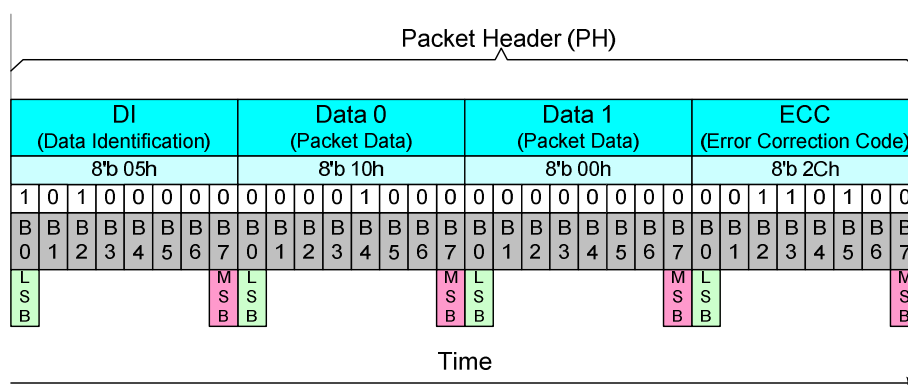


Figure 80: Display Command Set (DCS) Write, No Parameter (DCSWN-S) - Example

3.12.38. Display Command Set (DCS) Write, 1 Parameter (DCSW1-S)

“Display Command Set (DCS) Write, 1 Parameter” (DCSW1-S) is always used in a Short Packet (SPa), which is defined in the Data Type (DT, 01 0101b), from the MPU to the display module. These commands are defined in the table below. (See chapter 5.2: Command Description.)

Table 19: Display Command Set (DCS) Write, 1 Parameter (DCSW1-S)

Command
Gamma Set (26h)
Memory Write (2Ch), Note
Tearing Effect Line ON(35h)
Memory Access Control (36h)
Interface Pixel Format (3Ah)
Memory Write Continue (3Ch), ^{Note}
Write Display Brightness (51h)
Write CTRL Display (53h)
Write Content Adaptive Brightness control (55h)
Write CABC Minimum Brightness (5Eh)

A Short Packet (SPa) is defined as:

- Data Identification (DI)
 - o Virtual Channel (VC, DI [7...6]): 00b
 - o Data Type (DT, DI [5...0]): 01 0101b
- Packet Data (PD)
 - o Data 0: “Gamma Set (26h)”, Display Command Set (DCS)
 - o Data 1: 01hex, Parameter of the DCS
- Error Correction Code (ECC)

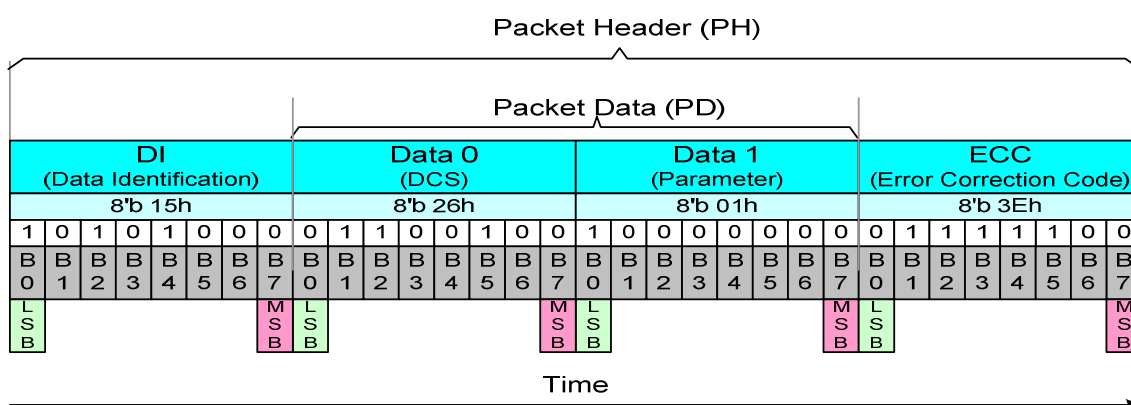


Figure 81: Display Command Set (DCS) Write, 1 Parameter (DCSW1-S) – Example

Note One subpixel has been written.

3.12.39. Display Command Set (DCS) Write Long (DCSW-L)

“Display Command Set (DCS) Write Long” (DCSW-L) is always used in a Long Packet (LPa), which is defined in the Data Type (DT, 11 1001b), from the MPU to the display module. Command (No Parameters) and Write (1 or more parameters), are defined in the table below. (See chapter 5.2: Command Description.)

Table 20: Display Command Set (DCS) Write Long (DCSW-L)

Command
NOP (00h), ^{Note 1}
Software Reset (01h), ^{Note 1}
Sleep In(10h), ^{Note 1}
Sleep Out (11h), ^{Note 1}
Partial Mode On (12h), ^{Note 1}
Normal Display Mode On (13h), ^{Note 1}
All Pixel Off (22h)
All Pixel On (23h)
Gamma Set (26h), ^{Note 2}
Display Off (28h), ^{Note 1}
Display ON (29h), ^{Note 1}
Column Address Set (2Ah)
Page Address Set (2Bh)
Memory Write (2Ch), ^{Note 2}
Partial Area (30h)
Tearing Effect Line OFF (34h), ^{Note 1}
Tearing Effect Line ON (35h), ^{Note 2}
Memory Access Control (36h), ^{Note 2}
Idle Mode Off (38h), ^{Note 1}
Idle Mode On (39h), ^{Note 1}
Interface Pixel Format (3Ah)
Memory Write Continue (3Ch), ^{Note 2}
Write Display Brightness (51h), ^{Note 2}
Write CTRL Display (53h), ^{Note 2}
Write Content Adaptive Brightness control (55h), ^{Note 2}
Write CABC Minimum Brightness (5Eh)

A Long Packet (LPa), when one command (no Parameter) was sent, is defined as:

- Data Identification (DI)
 - o Virtual Channel (VC, DI [7...6]): 00b
 - o Data Type (DT, DI [5...0]): 11 1001b
- Word Count (WC)
 - o Word Count (WC): 0001h
- Error Correction Code (ECC)
- Packet Data (PD): Data 0: “Sleep In (10h)”, Display Command Set (DCS)
- Packet Footer (PF)

^{Note 1} It can also be used in a Short Packet (SPa); See chapter “Display Command Set (DCS) Write, No Parameter”.

^{Note 2} It can also be used in a Short Packet (SPa); See chapter “Display Command Set (DCS) Write, 1 Parameter”.

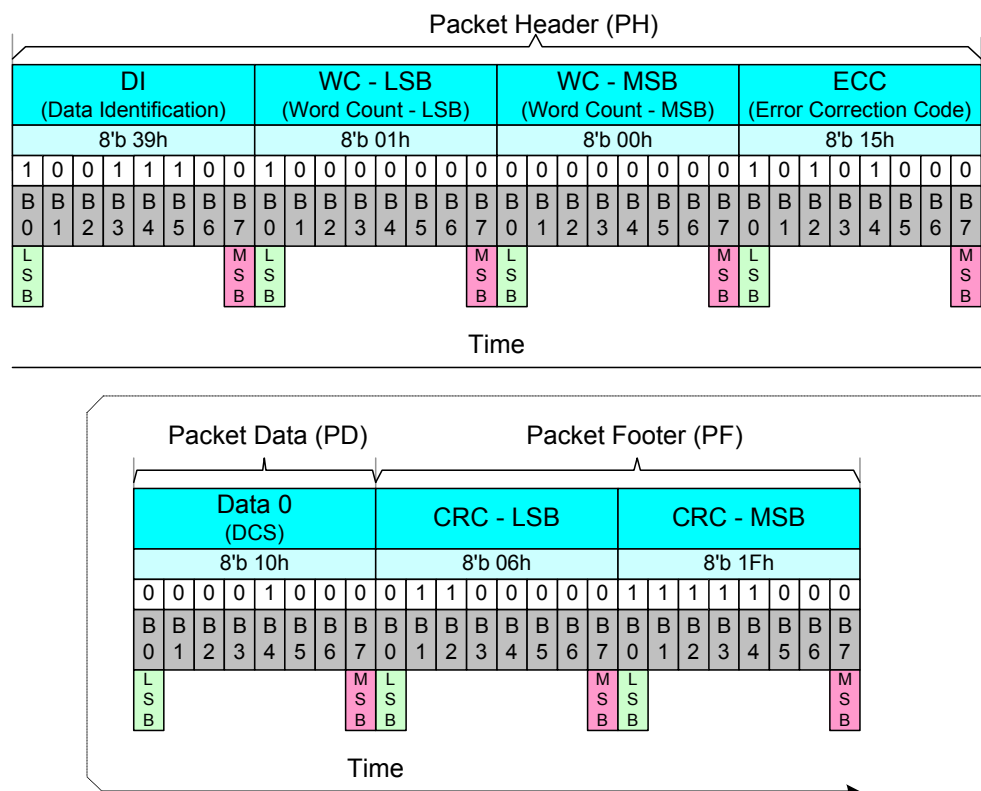


Figure 82: Display Command Set (DCS) Write Long (DCSW-L) with DCS Only - Example

A Long Packet (LPa), when one Write (1 parameter) was sent, is defined as:

- Data Identification (DI)
 - o Virtual Channel (VC, DI [7...6]): 00b
 - o Data Type (DT, DI [5...0]): 11 1001b
- Word Count (WC)
 - o Word Count (WC): 0002h
- Error Correction Code (ECC)
- Packet Data (PD):
 - o Data 0: "Gamma Set (26h)", Display Command Set (DCS)
 - o Data 1: 01hex, Parameter of the DCS
- Packet Footer (PF)

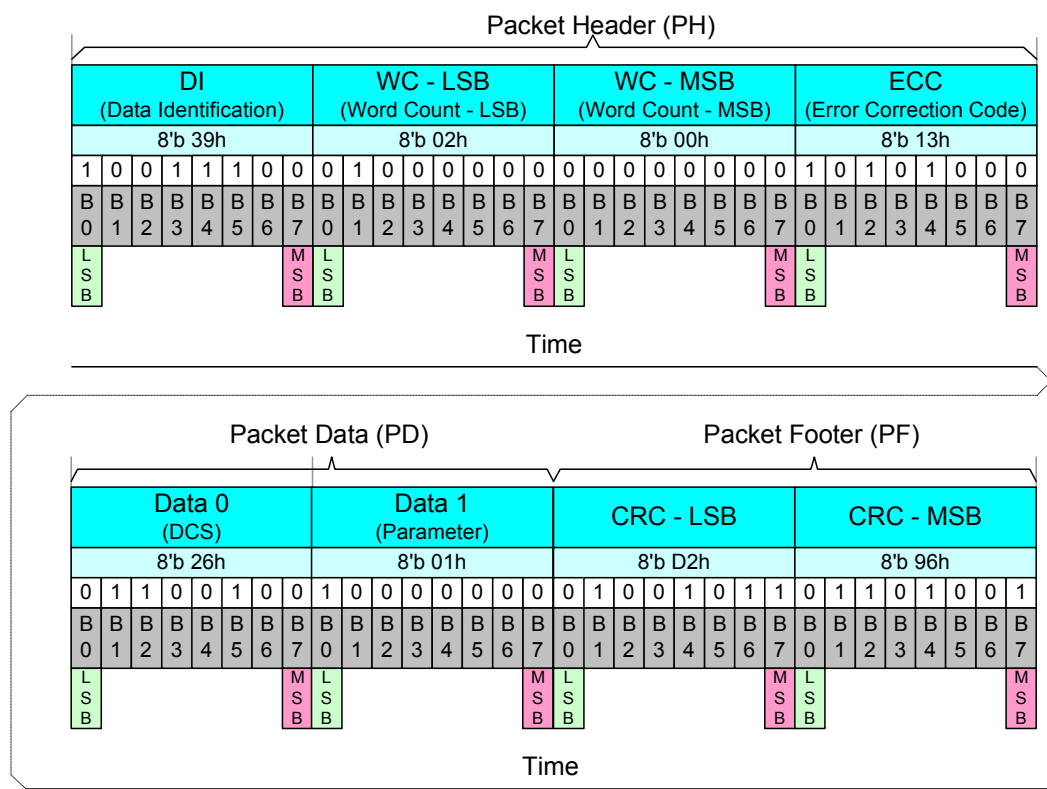


Figure 83: Display Command Set (DCS) Write Long with DCS and 1 Parameter - Example

A Long Packet (LPa), when one Write (4 parameters) was sent, is defined as:

- Data Identification (DI)
 - o Virtual Channel (VC, DI [7...6]): 00b
 - o Data Type (DT, DI [5...0]): 11 1001b
- Word Count (WC)
 - o Word Count (WC): 0005h
- Error Correction Code (ECC)
- Packet Data (PD):
 - o Data 0: "Column Address Set (2Ah)", Display Command Set (DCS)
 - o Data 1: 00hex, 1st Parameter of the DCS, Start Column SC [15...8]
 - o Data 2: 12hex, 2nd Parameter of the DCS, Start Column SC [7...0]
 - o Data 3: 01hex, 3rd Parameter of the DCS, End Column EC [15...8]
 - o Data 4: EFhex, 4th Parameter of the DCS, End Column EC [7...0]
- Packet Footer (PF)

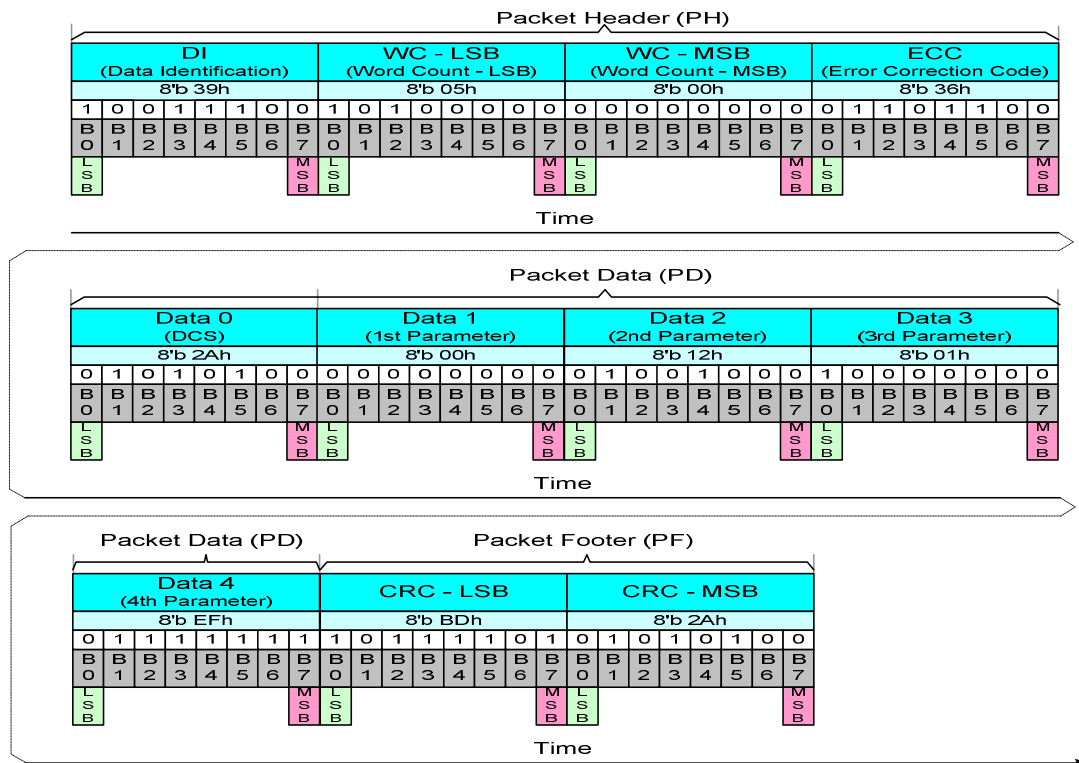


Figure 84: Display Command Set (DCS) Write Long with DCS and 4 Parameters - Example

3.12.40. Display Command Set (DCS) Read, No Parameter (DCSRN-S)

“Display Command Set (DCS) Read, No Parameter” (DCSRN-S) is always used in a Short Packet (SPa), which is defined in the Data Type (DT, 00 0110b), from the MPU to the display module. These commands are defined in the table below. (See Chapter 5.2: Command Description.)

Table 21: Display Command Set (DCS) Read, No Parameter (DCSRN-S)

Command
Read Number of the Errors on DSI (05h)
Read Display Power Mode (0Ah)
Read Display MADCTL (0Bh)
Read Display Pixel Format (0Ch)
Read Display Image Mode (0Dh)
Read Display Signal Mode (0Eh)
Read Display Self-Diagnostic Result (0Fh)
Memory Read (2Eh)
Memory Read Continue (3Eh)
Read Display Brightness Value (52h)
Read CTRL Value Display (54h)
Read Content Adaptive Brightness Control (56h)
Read CABC Minimum Brightness (5Fh)
Read Black/White Low Bits (70h)
Read Bkx (71h)
Read Bky (72h)
Read Wx (73h)
Read Wy (74h)
Read Red/Green Low Bits (75h)
Read Rx (76h)
Read Ry (77h)
Read Gx (78h)
Read Gy (79h)
Read Blue/A Color Low Bits (7Ah)
Read Bx (7Bh)
Read By (7Ch)
Read Ax (7Dh)
Read Ay (7Eh)
Read DDB Start (A1h)
Read DDB Continue (A8h)
First Checksum (AAh)
Read Continue Checksum (AFh)
Read ID1 (DAh)
Read ID2 (DBh)
Read ID3 (DCh)

The MPU has to define to the display module the maximum size of the returned packet. A command used for this purpose is “Set Maximum Return Packet Size” (SMRPS-S), which Data Type (DT) is 11 0111b and which uses Short Packets (SPa) before the MPU can send “Display Command Set (DCS) Read, No Parameter” to the display module. This sequence is illustrated below for reference purposes.

Step 1:

- The MPU sends “Set Maximum Return Packet Size” (Short Packet (SPa)) (SMRPS-S) to the display module when it wants to return one byte from the display module
- Data Identification (DI)
 - o Virtual Channel (VC, DI [7...6]): 00b
 - o Data Type (DT, DI [5...0]): 11 0111b
- Maximum Return Packet Size (MRPS)
 - o Data 0: 01hex
 - o Data 1: 00hex
- Error Correction Code (ECC)

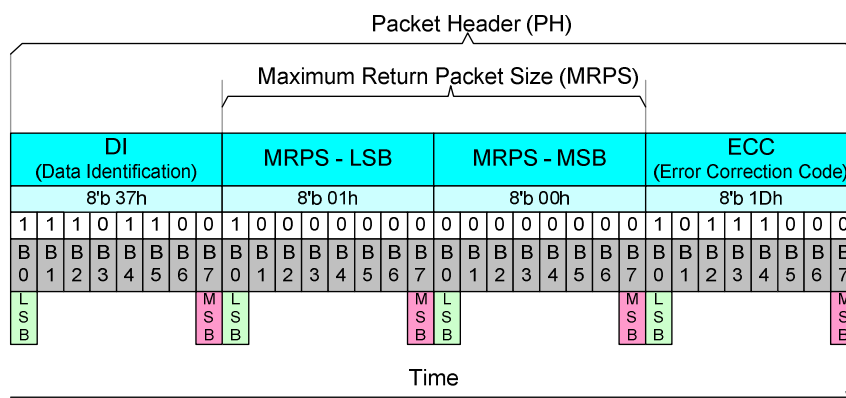


Figure 85 Set Maximum Return Packet Size (SMRPS-S) - Example

Step 2:

- The MPU wants to receive the value of the “Read ID1 (DAh)” from the display module when the MPU sends “Display Command Set (DCS) Read, No Parameter” to the display module.
- Data Identification (DI)
 - o Virtual Channel (VC, DI [7...6]): 00b
 - o Data Type (DT, DI [5...0]): 00 0110b
- Packet Data (PD)
 - o Data 0: “Read ID1 (DAh)”, Display Command Set (DCS)
 - o Data 1: Always 00hex
- Error Correction Code (ECC)

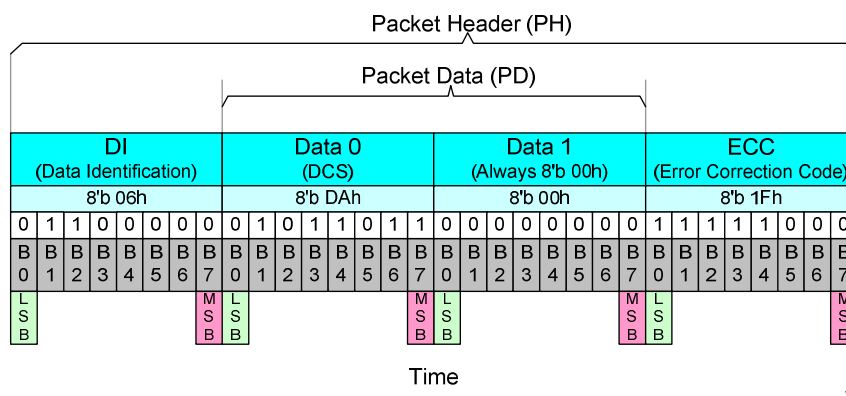


Figure 86 Display Command Set (DCS) Read, No Parameter (DCSRN-S) - Example

Step 3:

The display module can send 2 different information to the MPU after the Bus Turnaround (BTA).

1. An acknowledge with Error Report (AwER): it is used in a Short Packet (SPa) if an error is found while receiving a command. See the chapter "Acknowledge with Error Report (AwER)".
2. Information of the received command: it can be transmitted in a Short Packet (SPa) or Long Packet (LPa).

3.12.41. Null Packet, No Data (NP-L)

"Null Packet, No Data" (NP-L) is always used in a Long Packet (LPa), which is defined in the Data Type (DT, 001001b), from the MPU to the display module. The purpose of this command is to keep data lanes in the high speed mode (HSDT), if necessary.

The display module can ignore the Packet Data (PD), which is sent by the MPU.

A Long Packet (LPa), when 5 random data bytes of the Packet Data (PD) are sent, is defined as:

- Data Identification (DI)
 - o Virtual Channel (VC, DI [7...6]): 00b
 - o Data Type (DT, DI [5...0]): 00 1001b
- Word Count (WC)
 - o Word Count (WC): 0005hex
- Error Correction Code (ECC)
- Packet Data (PD):
 - o Data 0: 89hex (Random data)
 - o Data 1: 23hex (Random data)
 - o Data 2: 12hex (Random data)
 - o Data 3: A2hex (Random data)
 - o Data 4: E2hex (Random data)

- Packet Footer (PF)

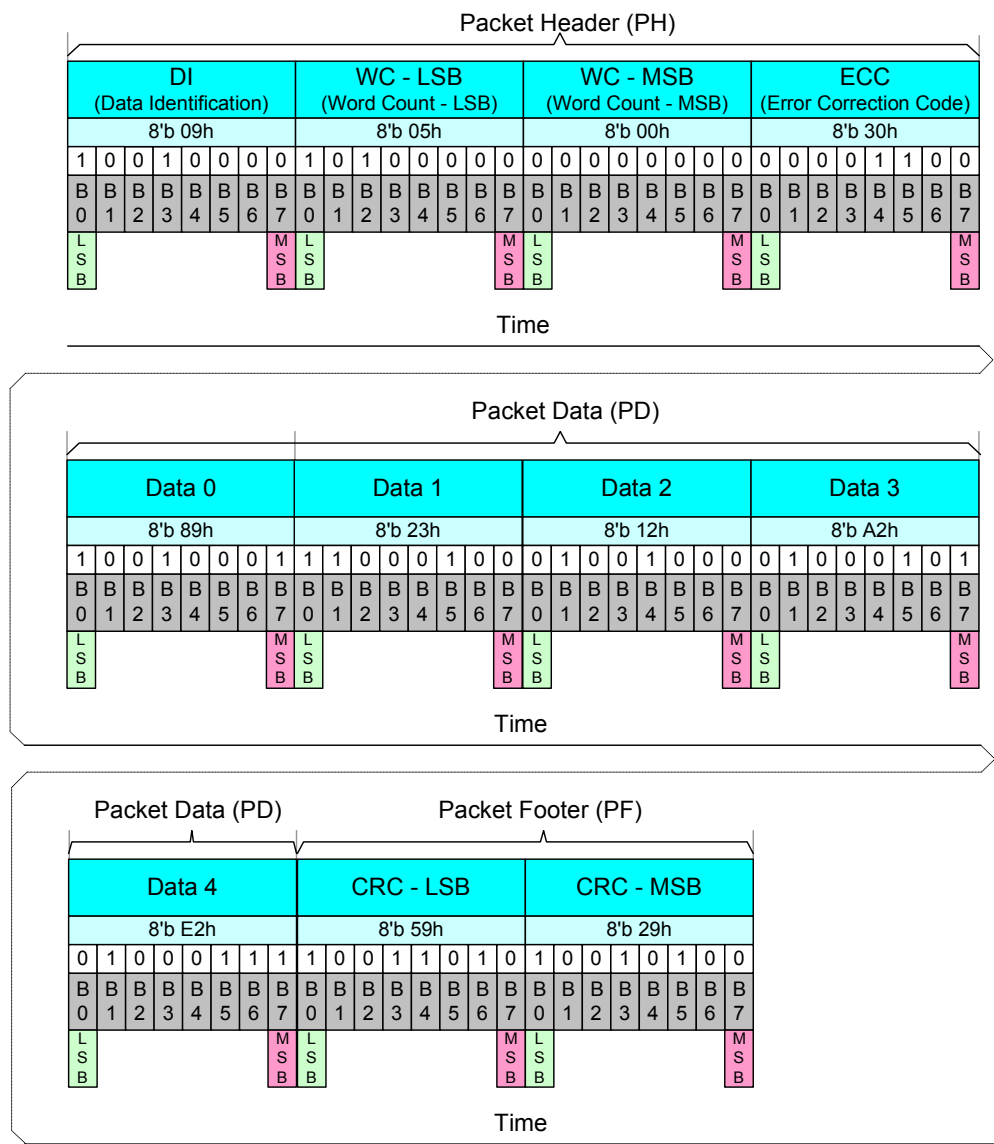


Figure 87: Null Packet, No Data (NP-L) - Example

3.12.42. End of Transmission Packet (EoTP)

“End of Transmission Packet” (EoTP), which is defined in the Data Type (DT, 00 1000b) and optional in the interface level, is always used in a Short Packet (SPa) from the MPU to the display module. The purpose of this command is to terminate the high Speed Data Transmission (HSDT) mode properly when the EoTP is added after the last payload packet before “End of Transmission” (EoT).

The MPU can decide if it wants to use the “End of Transmission Packet” (EoTP) or not. The display shall have the capability to support both. That is, if the MPU applies the EoTP, it shall report the “DSI Protocol Violation Error” when the EoTP is not detected in the High-Speed (HS). The display module error reporting shall be enabled/disabled statistically, according to the module application.

The display module will/will not receive “End of Transmission Packet” (EoTP) from the MPU during the Low Power Data Transmission (LPDT) mode before “Mark-1” (= leaving Escape mode), which ends the Low Power Data Transmission (LPDT) mode.

The display module is not allowed to send “End of Transmission Packet” (EoTP) to the MPU during the Low Power Data Transmission (LPDT) mode.

The summary of the receiving and transmitting EoTP is listed below.

Table 22: Receiving and Transmitting EoTP during LPDT

Direction	Display Module (DM) in High Speed Data Transmission (HSDT)	Display Module (DM) in Low Power Data Transmission (LPDT)
MPU => Display Module	With or Without EoTP is Supported	With or Without EoTP is Supported
Display Module => MPU	HS Mode is not available (EoTP is not available)	EoTP cannot be sent by the Display Module (DM)

Short Packet (SPa) uses a fixed format as follows:

- Data Identification (DI)
 - o Virtual Channel (VC, DI [7...6]): 00b
 - o Data Type (DT, DI [5...0]): 00 1000b
- Packet Data (PD)
 - o Data 0: 0Fhex
 - o Data 1: 0Fhex
- Error Correction Code (ECC)
 - o ECC: 01hex



Figure 1 illustrates the packet structure for the proposed protocol, showing two scenarios based on the destination node's address (D_n) and the source node's address (n).

The top diagram shows the structure for $D_n = \pm n = 0$ and 1 . The packet sequence is: LP-11 (green triangle), SOT (purple hexagon), LPa (Long Packet) (purple hexagon), SPa, EoTP (red hexagon), EOT (purple hexagon), and LP-11 (green triangle). A bracket labeled "Sent Packets" spans from the start of LPa to the end of SPa, EoTP.

The bottom diagram shows the structure for $D_n = \pm n = 0$ and 1 . The packet sequence is: LP-11 (green triangle), SOT (purple hexagon), SPa (Short Packet) (purple hexagon), SPa (Short Packet) (purple hexagon), SPa, EoTP (red hexagon), EOT (purple hexagon), and LP-11 (green triangle). A bracket labeled "Sent Packets" spans from the start of the first SPa to the end of SPa, EoTP.

Figure 89: End of Transmission Packet (EoTP) - Examples

3.12.43. Packet from the Display Module to the MPU

3.12.44. Used Packet Types

The display module can use Short Packets (SPa) or Long Packets (LPa) when it returns information to the MPU after the MPU requests information from the Display Module. This information can be a response of the Display Command Set (DCS) (See the chapter “Display Command Set (DCS) Read, No Parameter” (DCSRN-S)) or an Acknowledge with Error Report (See the chapter: “Acknowledge with Error Report (AwER)” (AwER)).

The used packet type is defined in the Data Type (DT). See the chapter “Data Type (DT)”. If the maximum size of the Packet Data (PD) could be sent in one packet, then the display module cannot separate returned bytes into several packets.

Both cases are illustrated below for reference purpose.

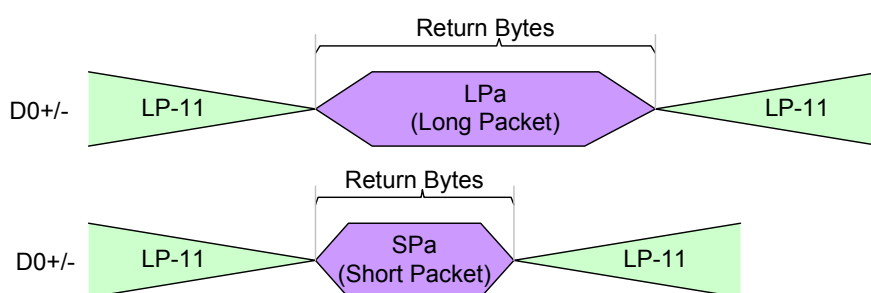


Figure 90: Return Bytes in a Single Packet

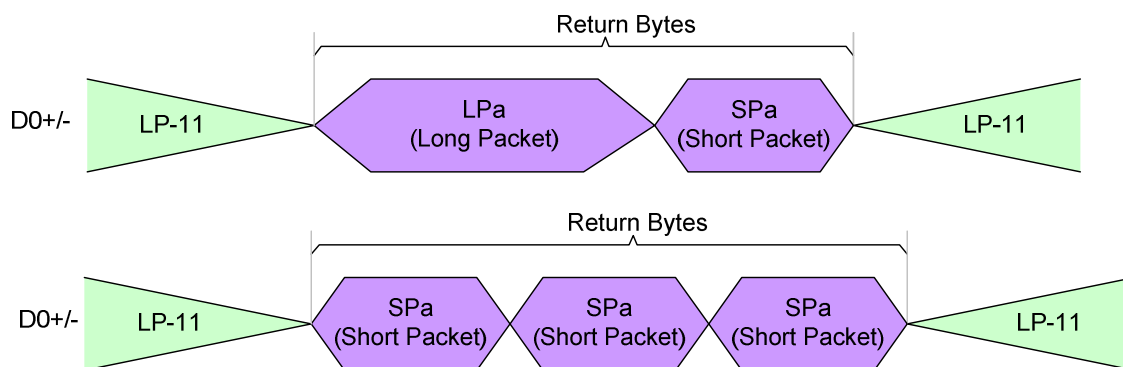


Figure 91: Return Bytes in Several Packets – Not Allowed

Exception:

The display module returns 2 packets (1st packet: Data, 2nd Packet: Acknowledge with Error Report) to the MPU when the display module receives a read command (see the chapter “Display Command Set (DCS) Read, No Parameter (DCSRN-S)”), in which a single bit error is detected and corrected by the EEC (see bit 8 in “Table 24: Acknowledge with Error Report (AwER) for Short Packet (SPa) Response”).

These returned packets are illustrated below for reference purpose.

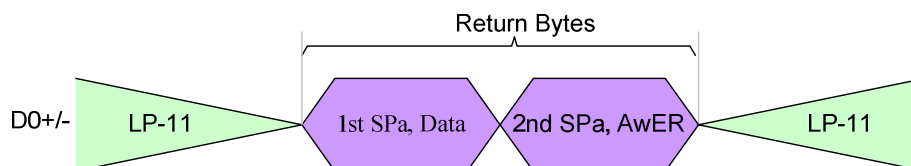


Figure 92: Exception when Return Bytes in Several Packets

AwER = Acknowledge with Error Report

3.12.45. Acknowledge with Error Report (AwER)

“Acknowledge with Error Report” (AwER), which is defined in the Data Type (DT, 00 0010b), is always transmitted through a Short Packet (SPa) from the display module to the MPU. The 16 bits in the Packet Data (PD) can indicate the current error(s) if one or more than one bit(s) is/are set to 1, as defined in the following table.

Table 23: Acknowledge with Error Report (AwER) for Long Packet (LPa) Response

Bit	Description
0	SoT Error
1	SoT Sync Error
2	EoT Sync Error
3	Escape Mode Entry Command Error
4	Low-Power Transmit Sync Error
5	Any Protocol Timer Time-Out
6	False Control Error
7	Contention is Detected on the Display Module
8	ECC Error, single-bit (detected and corrected)
9	ECC Error, multi-bit (detected, not corrected)
10	Checksum Error
11	DSI Data Type (DT) Not Recognized
12	DSI Virtual Channel (VC) ID Invalid
13	Invalid Transmission Length
14	Reserved, Set to 0 internally
15	DSI Protocol Violation

Table 24: Acknowledge with Error Report (AwER) for Short Packet (SPa) Response

Bit	Description
0	SoT Error
1	SoT Sync Error
2	EoT Sync Error
3	Escape Mode Entry Command Error
4	Low-Power Transmit Sync Error
5	Any Protocol Timer Time-Out
6	False Control Error
7	Contention is Detected on the Display Module
8	ECC Error, single-bit (detected and corrected)
9	ECC Error, multi-bit (detected, not corrected)
10	Reserved, Set to 0 internally (Only for Long Packet (LP))
11	DSI Data Type (DT) Not Recognized
12	DSI Virtual Channel (VC) ID Invalid
13	Invalid Transmission Length
14	Reserved, Set to 0 internally
15	DSI Protocol Violation

These errors are included in all packages, which are received from the MPU to the display module, before the Bus Turnaround (BTA).

The display module ignores the received packet which includes an error or errors.

Acknowledge with Error Report (AwER) in a Short Packet (SPa) is defined as:

- Data Identification (DI)
 - o Virtual Channel (VC, DI [7...6]): 00b
 - o Data Type (DT, DI [5...0]): 00 0010b
- Packet Data (PD)
 - o Bit 8: ECC Error, single-bit (detected and corrected)
 - o AwER: 0100h
- Error Correction Code (ECC)

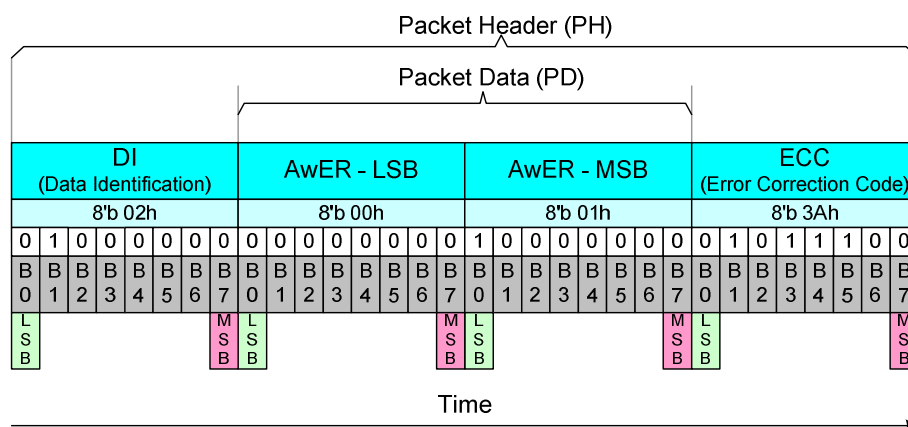


Figure 93: Acknowledge with Error Report (AwER) – Example

It is possible that the display module receives several packets, which include errors, from the MPU before the MPU performs the Bus Turnaround (BTA). Some examples are illustrated below for reference purpose.

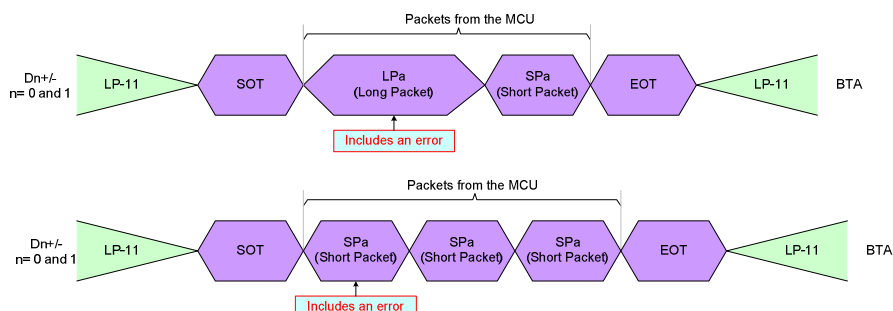


Figure 94: Errors Packets

Therefore, a method is needed to check if there are errors in the previous packets. These errors of the previous packets are indicated by “Read Display Signal Mode (0Eh)” and “Read Number of the Errors on DSI (05h)” commands. If a received packet includes an error, the bit D0 of the “Read Display Signal Mode (0Eh)” command will be set to 1.

The numbers of the packets, including an **ECC or CRC** error, are calculated in the RDNUMED register, which can read the “Read Number of the Errors on DSI (05h)” command. This command also sets the RDNUMED register to 00h and the bit D0 of the “Read Display Signal Mode (0Eh)” command to 0 after the MPU has read the RDNUMED register from the display module.

The functionality of the RDNUMED register is illustrated below for reference purpose.

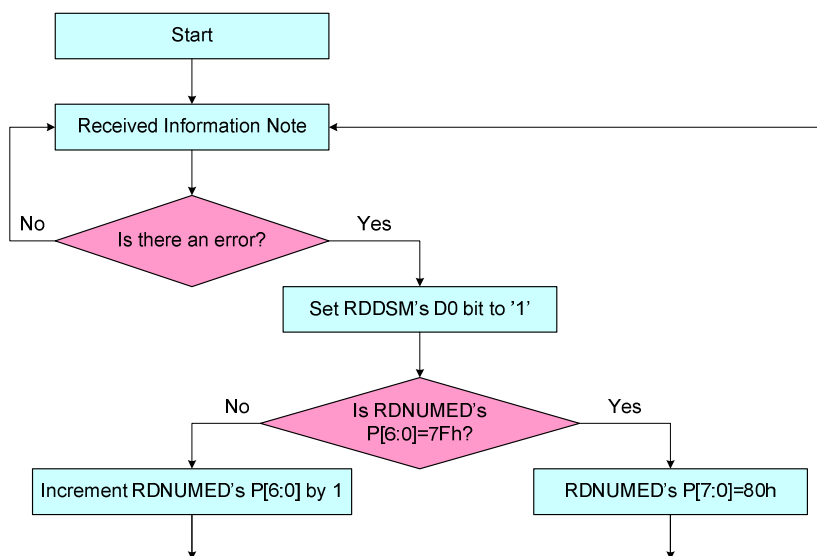


Figure 95: Flow Chart for Errors on DSI^{Note}

^{Note} 1. This information can be Interface or Packet Level Communication but it is always from the MPU to the display module in this case.

2. CRC or ECC error

3.12.46. DCS Read Long Response (DCSRR-L)

“DCS Read Long Response” (DCSRR-L), which is defined in the Data Type (DT, 011100b), is always used in a Long Packet (LPa) from the display module to the MPU. “DCS Read Long Response” (DCSRR-L) is used when the display module wants to respond to a DCS Read command, which the MPU has sent to the display module.

A Long Packet (LPa), which includes 5 data bytes of the Packet Data (PD), is defined as:

- Data Identification (DI)
 - o Virtual Channel (VC, DI [7...6]): 00b
 - o Data Type (DT, DI [5...0]): 01 1100b
- Word Count (WC)
 - o Word Count (WC): 0005hex
- Error Correction Code (ECC)
- Packet Data (PD):
 - o Data 0: 89hex
 - o Data 1: 23hex
 - o Data 2: 12hex
 - o Data 3: A2hex
 - o Data 4: E2hex
- Packet Footer (PF)

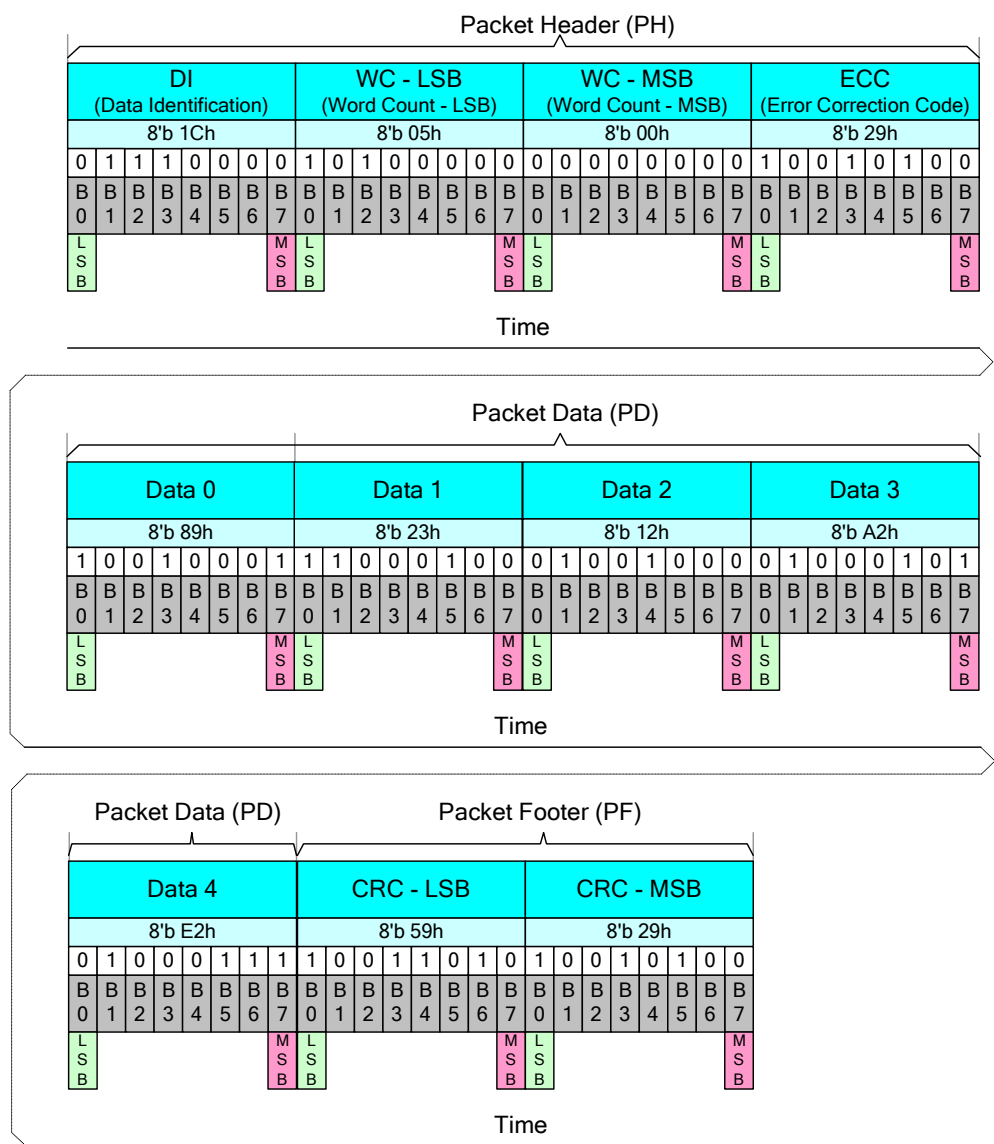


Figure 96: DCS Read Long Response (DCSRR-L) - Example

3.12.47. DCS Read Short Response, 1 Byte Returned (DCSRR1-S)

“DCS Read Short Response, 1 Byte Returned”, which is defined in the Data Type (DT, 10 0001b), (DCSRR1-S) is always used in a Short Packet (SPa) from the display module to the MPU. “DCS Read Short Response, 1 Byte Returned (DCSRR1-S) is used when the display module wants to respond to a DCS Read command, which the MPU has sent to the display module.

A Short Packet (SPa) is defined as:

- Data Identification (DI)
 - o Virtual Channel (VC, DI [7...6]): 00b
 - o Data Type (DT, DI [5...0]): 10 0001b
- Packet Data (PD)
 - o Data 0: 45hex
 - o Data 1: 00hex (Always)
- Error Correction Code (ECC)

This is defined on the Short Packet (SP) as follows.

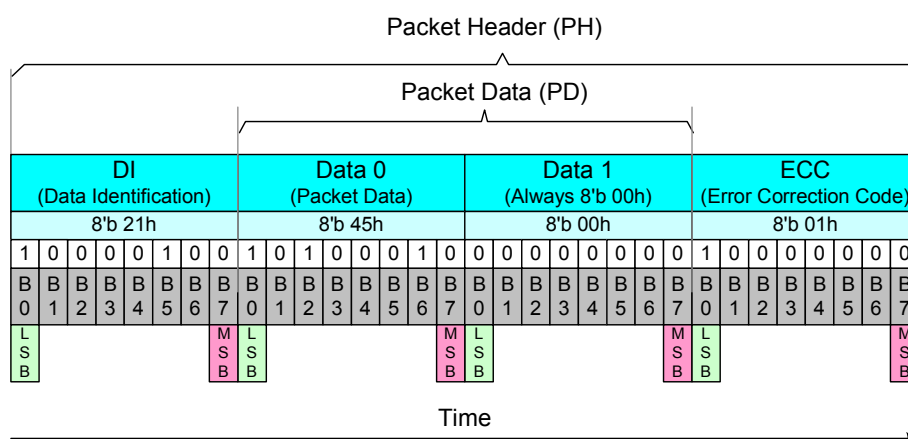


Figure 97: DCS Read Short Response, 1 Byte Returned (DCSRR1-S) - Example

3.12.48. DCS Read Short Response, 2 Bytes Returned (DCSRR2-S)

“DCS Read Short Response, 2 Bytes Returned” (DCSRR2-S) is always used in a Short Packet (SPa), which is defined in the Data Type (DT, 10 0010b), from the display module to the MPU. “DCS Read Short Response, 2 Bytes Returned” (DCSRR2-S) is used when the display module wants to respond to a DCS Read command, which the MPU has sent to the display module.

A Short Packet (SPa) is defined as:

- Data Identification (DI)
 - o Virtual Channel (VC, DI [7...6]): 00b
 - o Data Type (DT, DI [5...0]): 10 0010b
- Packet Data (PD)
 - o Data 0: 45hex
 - o Data 1: 32hex
- Error Correction Code (ECC)

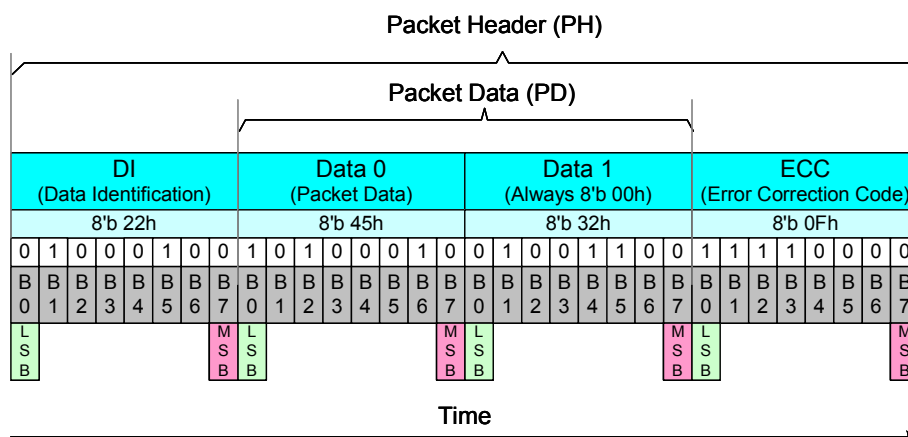


Figure 98: DCS Read Short Response, 2 Bytes Returned (DCSRR2-S) - Example

3.12.49. Communication Sequences

3.12.50. General

The communication sequences can be done on interface or packet levels between the MPU and the display module. See chapters “Interface Level Communication” and “Packet Level Communication”.

This communication sequence description is for DSI data lanes (DSI-D0+/- and DSI-D1+/-), and it is assumed that the needed low level communication is done on DSI clock lanes (DSI-CLK+/-) automatically. See the chapter “DSI-CLK Lanes”.

Functions of the interface level communication are described in the following table.

Table 25: Interface Level Communication

Interface Mode	Abbreviation	Interface Action Description
Low Power	LP-11	Stop State
	LPDT	Low Power Data Transmission
	ULPS	Ultra-Low Power State
	RAR	Remote Application Reset
	TEE	Tearing Effect Event
	ACK	Acknowledge (No Error)
	BTA	Bus Turnaround
High Speed	HSDT	High speed Data Transmission

Functions of the packet level communication are described in the following table.

Table 26: Packet Level Communication

Interface Mode	Abbreviation	Packet Size	Interface Action Description
MPU	DCSW1-S	Short Packet	DCS Write, 1 Parameter
	DCSWN-S	Short Packet	DCS Write, No Parameter
	DCSW-L	Long Packet	DCS Write Long
	DCSRN-S	Short Packet	DCS Read, No Parameter
	SMRPS-S	Short Packet	Set Maximum Return Packet Size
	NP-L	Long Packet	Null Packet, No Data
	EoTP	Short Packet	End of Transmission Packet
Display Module (ILI9806G)	AwER	Short Packet	Acknowledge with Error Packet
	DCSRR-L	Long Packet	DCS Read Long Response
	DCSRR1-S	Short Packet	DCS Read Short Response
	DCSRR2-S	Short Packet	DCS Read Short Response

3.12.51. Sequences

3.12.52. DCS Write, 1 Parameter Sequence

A Short Packet (SPa) of “Display Command Set (DCS) Write, 1 Parameter (DCSW1-S)” is defined in the chapter “Display Command Set (DCS) Write, 1 Parameter (DCSW1-S)”, and examples of sequences on how this packet is used is described in the following tables.

Table 27: DCS Write, 1 Parameter Sequence – Example 1

DCS Write, 1 Parameter Sequence – Example 1						
Line	MPU		Information Direction	Display Module (ILI9806G)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	DCSW1-S	LPDT	→	--	--	
3	--	LP-11	→	--	--	End

Table 28: DCS Write, 1 Parameter Sequence – Example 2

DCS Write, 1 Parameter Sequence – Example 2						
Line	MPU		Information Direction	Display Module (ILI9806G)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	DCSW1-S	HSDT	→	--	--	
3	EoTP	HSDT	→	--	--	End of Transmission Packet
4	--	LP-11	→	--	--	End

Table 29: DCS Write, 1 Parameter Sequence – Example 3

DCS Write, 1 Parameter Sequence – Example 3						
Line	MPU		Information Direction	Display Module (ILI9806G)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	DCSW1-S	HSDT	→	--	--	
3	EoTP	HSDT	→	--	--	End of Transmission Packet
4	--	LP-11	→	--	--	
5	--	BTA	↔	BTA	--	Interface Control Change from MPU to the display module
6	--	--	←	LP-11	--	If No Error → Go to Line 8 If Error Occurs → Go to Line 13
7						
8	--	--	←	ACK	--	No Error
9	--	--	←	LP-11	--	
10	--	BTA	↔	BTA	--	Interface Control Change from the display module to MPU
11	--	LP-11	→	--	--	End
12						
13	--	--	←	LPDT	AwER	Error Report
14	--	--	←	LP-11	--	
15	--	BTA	↔	BTA	--	
16	--	LP-11	→	--	--	End

3.12.53. DCS Write, No Parameter Sequence

A Short Packet (SPa) of “Display Command Set (DCS) Write, No Parameter (DCSWN-S)” is defined in the chapter “Display Command Set (DCS) Write, No Parameter (DCSWN-S)”, and examples of sequences on how this packet is used are described in the following tables.

Table 30: DCS Write, No Parameter Sequence – Example 1

DCS Write, No Parameter Sequence – Example 1						
Line	MPU		Information Direction	Display Module (ILI9806G)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	DCSWN-S	LPDT	→	--	--	
3	--	LP-11	→	--	--	End

Table 31: DCS Write, No Parameter Sequence – Example 2

DCS Write, No Parameter Sequence – Example 2						
Line	MPU		Information Direction	Display Module (ILI9806G)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	DCSWN-S	HSDT	→	--	--	
3	EoTP	HSDT	→	--	--	End of Transmission Packet
4	--	LP-11	→	--	--	End

Table 32: DCS Write, No Parameter Sequence – Example 3

DCS Write, 1 Parameter Sequence – Example 3						
Line	MPU		Information Direction	Display Module (ILI9806G)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	DCSWN-S	HSDT	→	--	--	
3	EoTP	HSDT	→	--	--	End of Transmission Packet
4	--	LP-11	→	--	--	
5	--	BTA	↔	BTA	--	Interface Control Change from MPU to the display module
6	--	--	←	LP-11	--	If No Error → Go to Line 8 If Error Occurs → Go to Line 13
7						
8	--	--	←	ACK	--	No Error
9	--	--	←	LP-11	--	
10	--	BTA	↔	BTA	--	Interface Control Change from the display module to MPU
11	--	LP-11	→	--	--	End
12						
13	--	--	←	LPDT	AwER	Error Report
14	--	--	←	LP-11	--	
15	--	BTA	↔	BTA	--	
16	--	LP-11	→	--	--	End

3.12.54. DCS Write Long Sequence

A Long Packet (LPa) of “Display Command Set (DCS) Write Long (DCSW-L)” is defined in the chapter “Display Command Set (DCS) Write Long (DCSW-L)”, and examples of sequences on how this packet is used are described in the following tables.

Table 33: DCS Write Long Sequence – Example 1

DCS Write Long Sequence – Example 1						
Line	MPU		Information Direction	Display Module (ILI9806G)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	DCSW-L	LPDT	→	--	--	
3	--	LP-11	→	--	--	End

Table 34: DCS Write Long Sequence – Example 2

DCS Write Long Sequence – Example 2						
Line	MPU		Information Direction	Display Module (ILI9806G)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	DCSRN-S	HSDT	→	--	--	
3	EoTP	HSDT	→	--	--	End of Transmission Packet
4	--	LP-11	→	--	--	End

Table 35: DCS Write Long Sequence – Example 3

DCS Write Long Sequence – Example 3						
Line	MPU		Information Direction	Display Module (ILI9806G)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	DCSRN-S	HSDT	→	--	--	
3	EoTP	HSDT	→	--	--	End of Transmission Packet
4	--	LP-11	→	--	--	
5	--	BTA	↔	BTA	--	Interface Control Change from MPU to the display module
6	--	--	←	LP-11	--	If No Error → Go to Line 8 If Error Occurs → Go to Line 13
7						
8	--	--	←	ACK	--	No Error
9	--	--	←	LP-11	--	
10	--	BTA	↔	BTA	--	Interface Control Change from the display module to MPU
11	--	LP-11	→	--	--	End
12						
13	--	--	←	LPDT	AwER	Error Report
14	--	--	←	LP-11	--	
15	--	BTA	↔	BTA	--	

16	--	LP-11	➔	--	--	End
----	----	-------	---	----	----	-----

Table 36: DCS Write Long Sequence – Example 4^{Note}

DCS Write Long Sequence – Example 4						
Line	MPU		Information Direction	Display Module (ILI9806G)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	DCSW-L	HSDT	→	--	--	Memory Write (2Ch)
3	DCSW-L	HSDT	→	--	--	Memory Write Continue (3Ch)
4	DCSW-L	HSDT	→	--	--	Memory Write Continue (3Ch)
5	DCSW1-S	HSDT	→	--	--	Memory Write Continue (3Ch) with 1 Parameter
6	EoTP	HSDT	→	--	--	End of Transmission Packet
7	--	LP-11	→	--	--	End

3.12.55. DCS Read, No Parameter Sequence

A Short Packet (SPa) of “Display Command Set (DCS) Read, No Parameter (DCSRN-S)” is defined in the chapter “Display Command Set (DCS) Read, No Parameter (DCSRN-S)”, and examples of sequences on how this packet is used are described in the following tables.

Table 37: DCS Read, No Parameter Sequence – Example 1

DCS Read, No Parameter Sequence – Example 1						
Line	MPU		Information Direction	Display Module (ILI9806G)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	SMRPS-S	HSDT	→	--	--	Defined how many data byte is wanted to read : 1 byte
3	DCSRN-S	HSDT	→	--	--	Wanted to get a response ID1 (DAh)
4	EoTP	HSDT	→	--	--	End of Transmission Packet
5	--	LP-11	→	--	--	
6	--	BTA	↔	BTA	--	Interface Control Change from MPU to the display module
7	--	--	←	LP-11	--	If No Error → Go to Line 9 If Error Occurs → Go to Line 14 If Error is Corrected by ECC → Go to Line 19
8						
9	--	--	←	LPDT	DCSRR1-S	Response 1 byte return
10	--	--	←	LP-11	--	
11	--	BTA	↔	BTA	--	Interface Control Change from the display module to MPU
12	--	LP-11	→	--	--	End
13						
14	--	--	←	LPDT	AwER	Error Report
15	--	--	←	LP-11	--	
16	--	BTA	↔	BTA	--	Interface Control Change from the display module to MPU
17	--	LP-11	→	--	--	End
18						

^{Note} This is an example that image data are sent in 4 packets.

19	--	--	←	LPDT	DCSRR1-S	Response 1 byte return
20	--	--	←	LPDT	AwER	Error Report (Error is corrected by ECC)
21	--	--	←	LP-11	--	
22	--	BTA	↔	BTA	--	Interface Control Change from the display module to MPU
23	--	LP-11	→	--	--	End

Table 38: DCS Read, No Parameter Sequence – Example 2

DCS Read, No Parameter Sequence – Example 2						
Line	MPU		Information Direction	Display Module (ILI9806G)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	SMRPS-S	HSDT	→	--	--	Defined how many data byte is wanted to read : 200 bytes
3	DCSRN-S	HSDT	→	--	--	Wanted to get a response "Memory Read" (2Eh)
4	EoTP	HSDT	→	--	--	End of Transmission Packet
5	--	LP-11	→	--	--	
6	--	BTA	↔	BTA	--	Interface Control Change from MPU to the display module
7	--	--	←	LP-11	--	If No Error → Go to Line 9 If Error Occurs → Go to Line 14 If Error is Corrected by ECC → Go to Line 19
8						
9	--	--	←	LPDT	DCSRR-L	Response 200 byte return
10	--	--	←	LP-11	--	
11	--	BTA	↔	BTA	--	Interface Control Change from the display module to MPU
12	--	LP-11	→	--	--	End
13						
14	--	--	←	LPDT	AwER	Error Report
15	--	--	←	LP-11	--	
16	--	BTA	↔	BTA	--	Interface Control Change from the display module to MPU
17	--	LP-11	→	--	--	End
18						
19	--	--	←	LPDT	DCSRR-S	Response 200 byte return
20	--	--	←	LPDT	AwER	Error Report (Error is corrected by ECC)
21	--	--	←	LP-11	--	
22	--	BTA	↔	BTA	--	Interface Control Change from the display module to MPU
23	--	LP-11	→	--	--	End

3.12.56. Null Packet, No Data Sequence

A Long Packet (LPa) of “Null Packet, No Data (NP-L)” is defined in the chapter “Null Packet, No Data (NP-L)”, and an example of sequence on how this packet is used is described in the following table.

Table 39: Null Packet, No Data Sequence - Example

Null Packet, No Data Sequence – Example						
Line	MPU		Information Direction	Display Module (ILI9806G)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	NP-L	HSDT	→	--	--	Only High Speed Data Transmission is used
3	EoTP	HSDT	→	--	--	End of Transmission Packet
4	--	LP-11	→	--	--	End

3.12.57. End of Transmission Packet

A Short Packet (SPa) of “End of Transmission (EoTP)” is defined in the chapter “End of Transmission Packet (EoTP)”, and an example of sequence on how this packet is used is described in the following table.

Table 40: End of Transmission Packet – Example

End of Transmission Packet – Example						
Line	MPU		Information Direction	Display Module (ILI9806G)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	NP-L	HSDT	→	--	--	Only High Speed Data Transmission is used
3	EoTP	HSDT	→	--	--	End of Transmission Packet
4	--	LP-11	→	--	--	End

3.12.58. 16 Bit/Pixel Writing

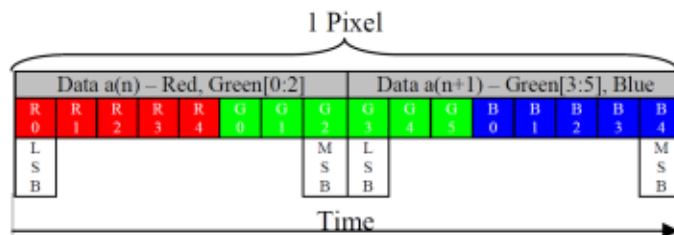


Figure 99: One Pixel Bit and Write Color Orders

The MPU can send the following packet to the display module.

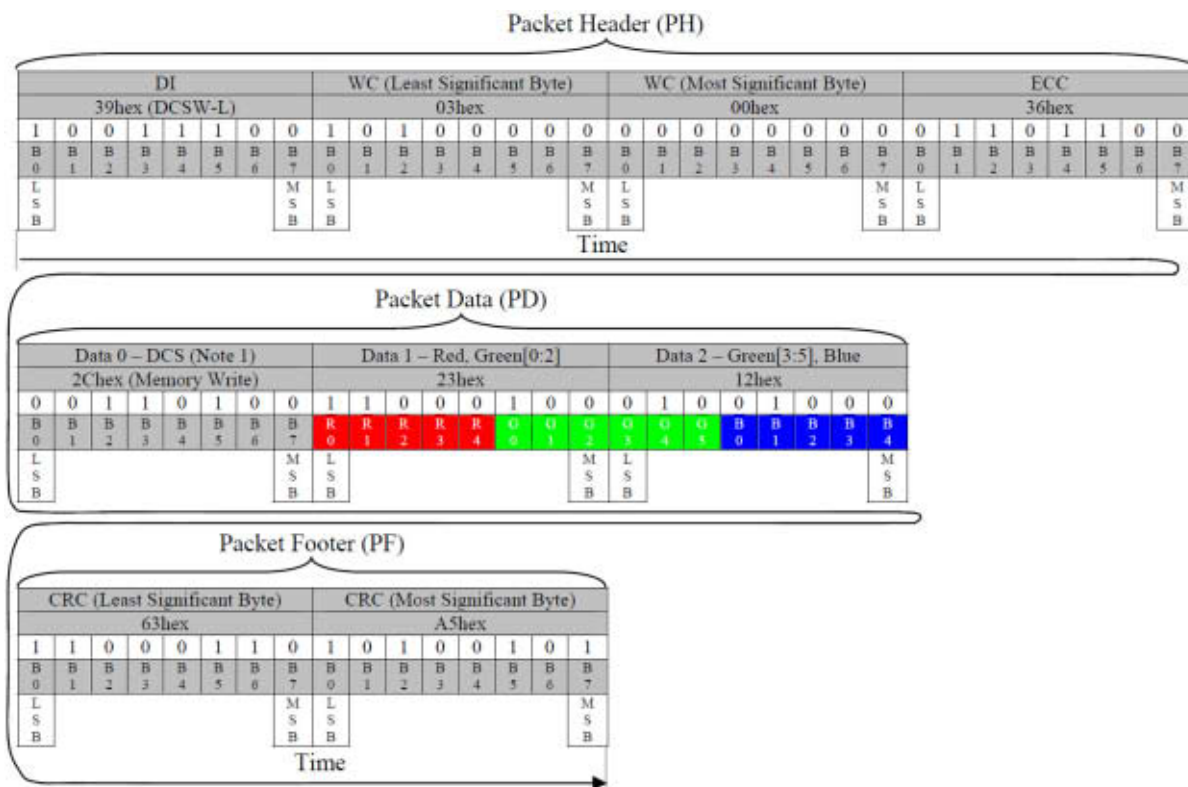


Figure 100: One Pixel Write (DCSW-L) – Example 1^{Note}

- ^{Note}
1. DCS (Data 0) can be Memory Write (2Ch) or Memory Write Continue (3Ch) command.
 2. It is possible that one pixel information is split into different packets which end and star as follows: RG – GB (2 packets).
 3. A packet can include several pixels (not just one pixel as in this example).

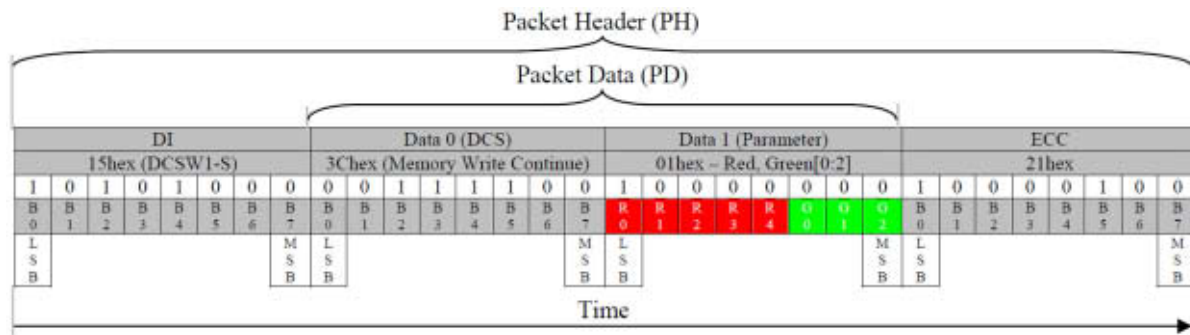


Figure 101: Red/Green [0:2] Subpixel Write (DCSW1-S) – Example 2^{Note 1}

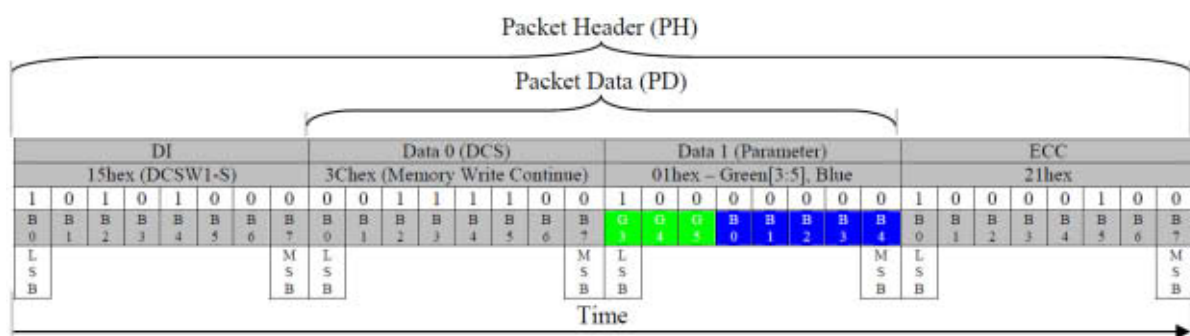


Figure 102: Green [3:5]/Blue Subpixel Write (DCSW1-S) – Example 3^{Note 2}

3.12.59. 24 Bit/Pixel Writing

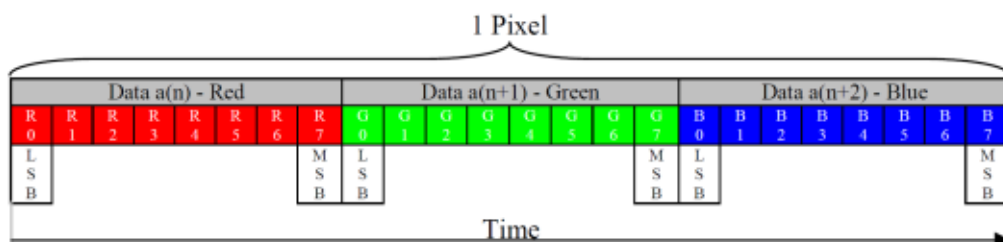


Figure 103: One Pixel Bit and Color Write Orders

The MPU can send the following packet to the display module.

^{Note 1} DCS (Data 0) can also be "Memory Write" (2Ch) command.

^{Note 2} 1. DCS (Data 0) cannot be "Memory Write" (2Ch) command. It must always be "Memory Write Continue" (3Ch).
2. Previous data byte is R [0:4] G [0:2].

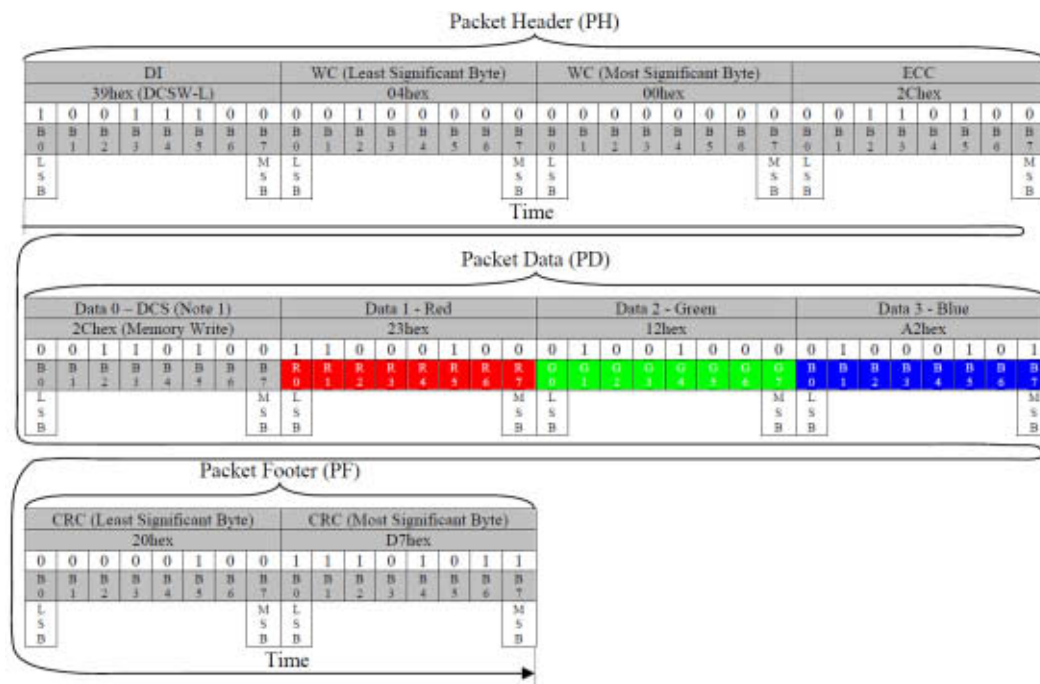


Figure 104: One Pixel Write (DCSW-L) – Example^{Note}

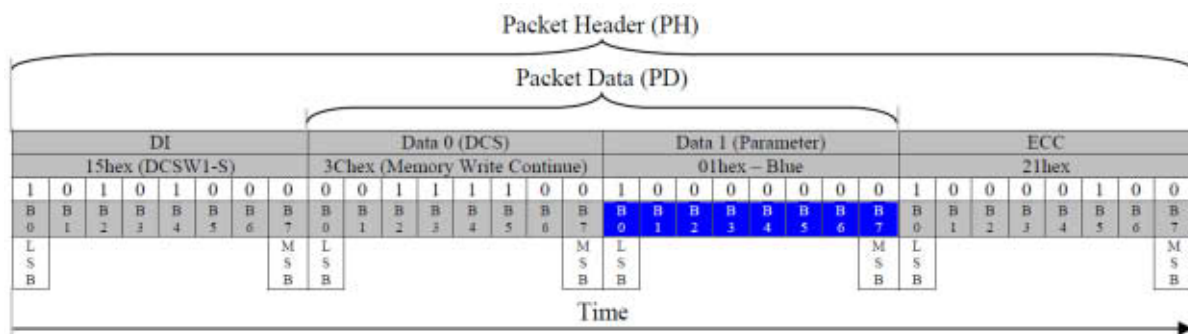


Figure 105: Blue Subpixel Write (DCSW1-S) – Example 2

Notes:

1. DCS (Data 0) cannot be “Memory Write” (2Ch) command. It must always be “Memory Write Continue” (3Ch)
2. Previous data byte is G [0:7].

- ^{Note}
1. DCS (Data 0) can be Memory Write (2Ch) or Memory Write Continue (3Ch) command.
 2. It is possible that one pixel information is split in two or three different packets which end and start as follows:
 - R – GB (2 packets)
 - RG – B (2 packets)
 - R – G – B (3 packets)
 3. A packet can include several pixels (not just one pixel as in this example).

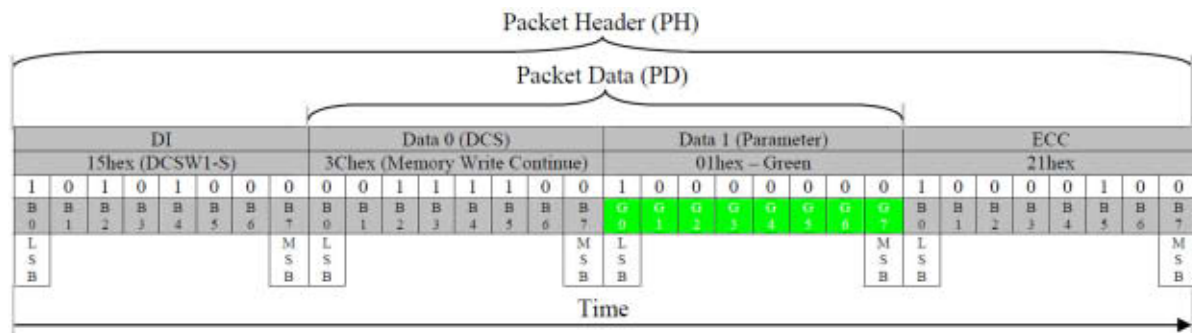


Figure 106: Green Subpixel Write (DCSW1-S) – Example 3

Notes:

1. DCS (Data 0) cannot be “Memory Write” (2Ch) command. It must always be “Memory Write Continue” (3Ch)
2. Previous data byte is R [0:7].

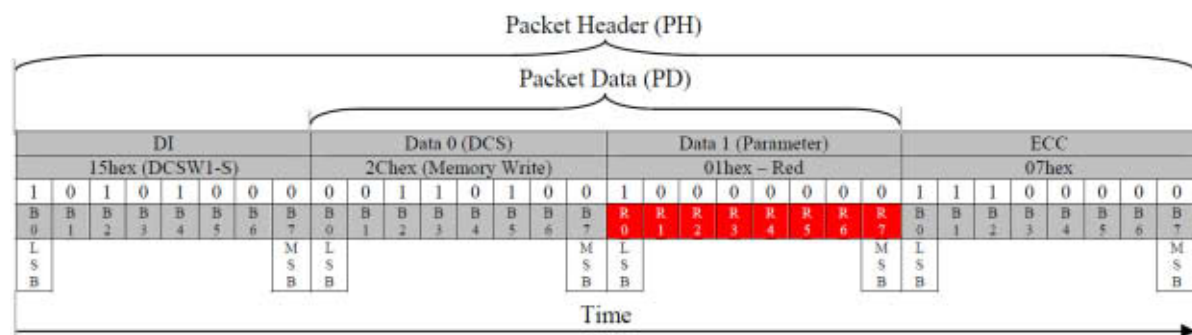


Figure 107: Red Subpixel Write (DCSW1-S) – Example 4

Notes:

1. DCS (Data 0) can also be “Memory Write Continue” (3Ch) command.
2. Previous data byte is B [0:7].

3.12.60. 24 bit/pixel Reading

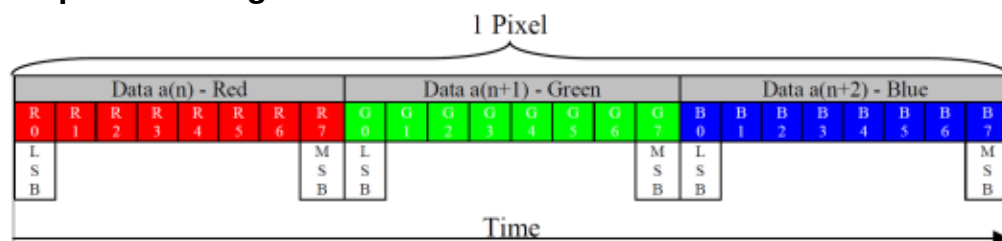


Figure 108: One Pixel Bit and Color Read Order

The display module can send following packets to the MPU after the MPU has sent a read command “Memory Read (2Eh)” or “Memory Read Continue (3Eh)”.

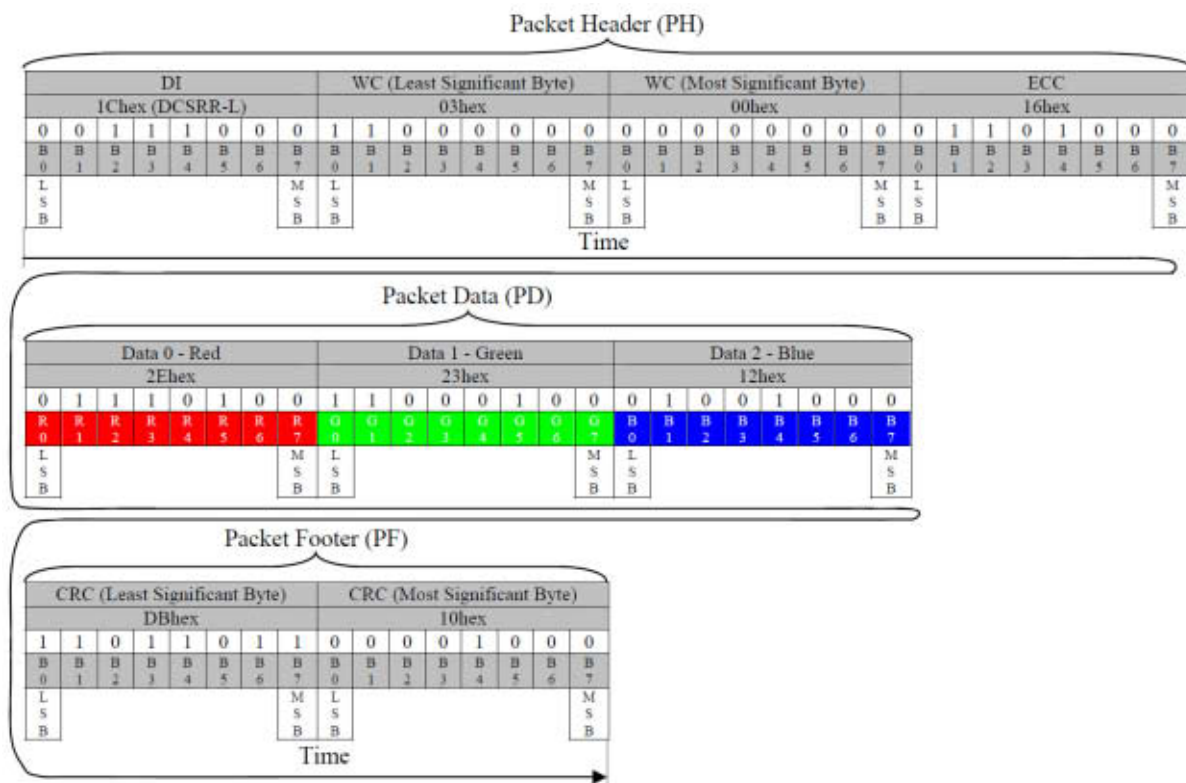


Figure 109: One Pixel Read Response (DCSRR-L) – Example 1

Note: It is possible that one pixel information is split in two or three different packets:

- R – GB (2 packets)
- RG – B (2 packets)
- R – G – B (3 packets)

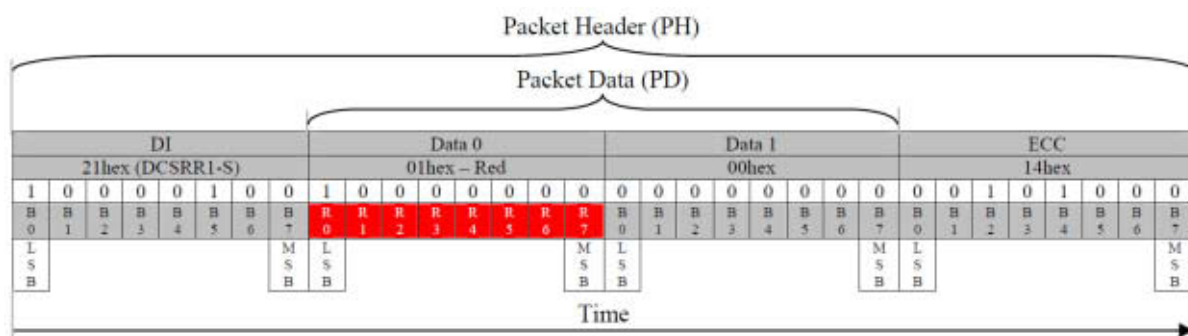


Figure 110: Red Subpixel Response (DCSRR1-S) – Example 2

Notes:

1. Data 1 is always 00h.
2. Previous data byte is B [0:7].

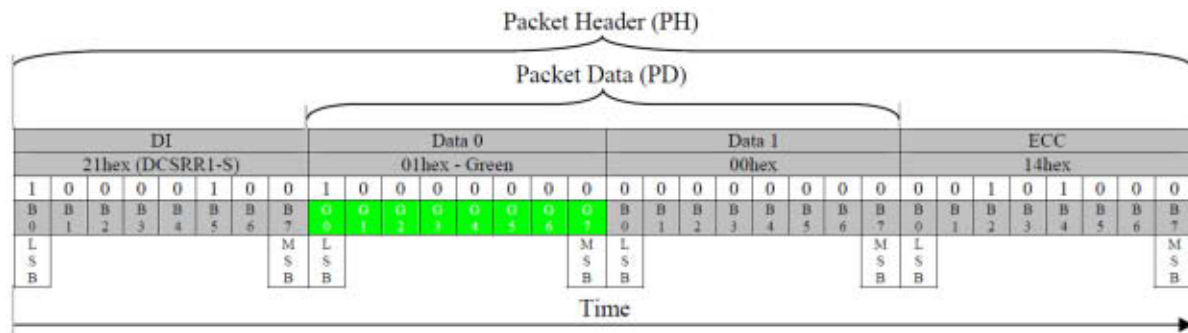


Figure 111: Green Subpixel Response (DCSRR1-S) – Example 3

Notes:

1. Data 1 is always 00h.
2. Previous data byte is R [0:7].

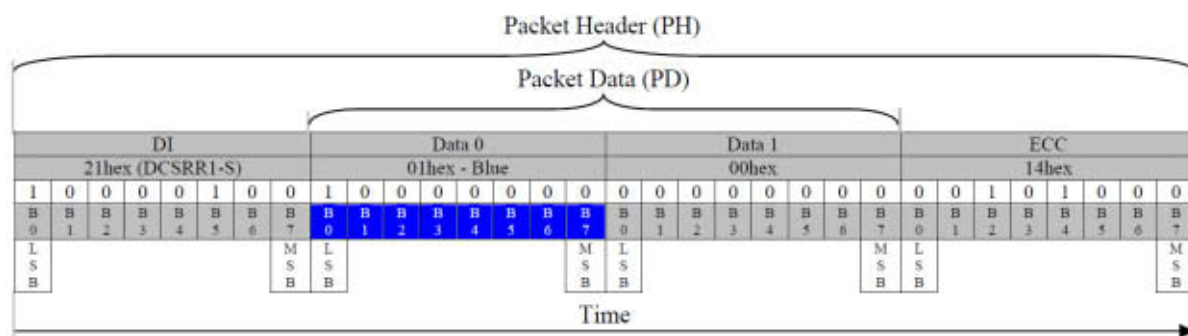


Figure 112: Blue Subpixel Response (DCSRR1-S) – Example 4

Notes:

1. Data 1 is always 00h.
2. Previous data byte is G [0:7].

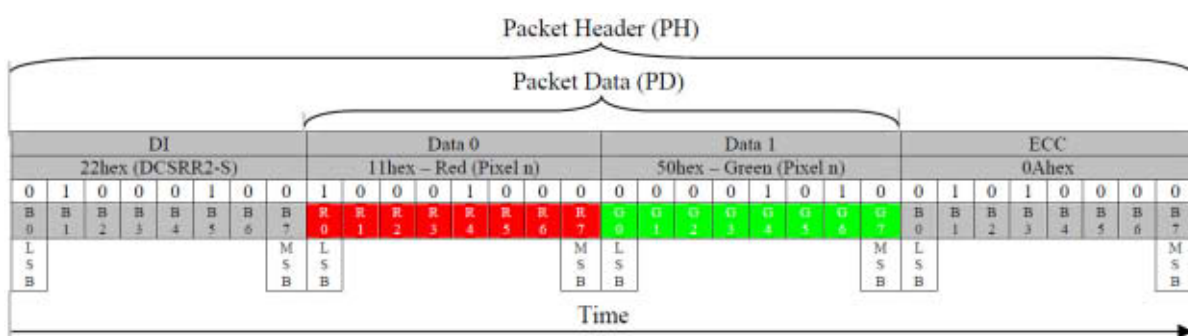


Figure 113: Red and Green Subpixels Response (DCSRR2-S) – Example 5



Note: Previous data byte is R [0:7].



Note: Previous data byte is G [0:7].

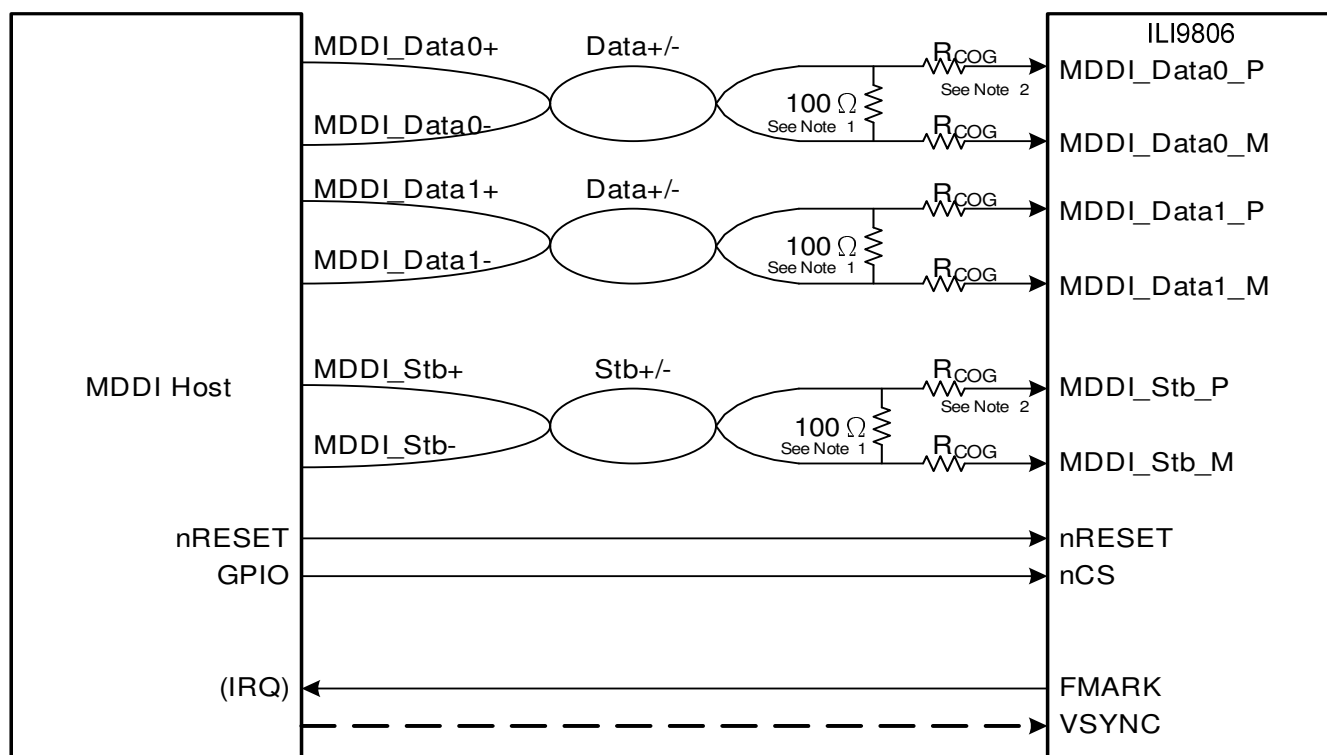
3.13. MDDI (Mobile Display Digital Interface)

MDDI (Mobile display digital interface) is a differential small amplitude serial interface for high-speed data transfer via following 6 lines: Stb+/- (MDDI_STB_P, MDDI_STB_M), Data+/- (MDDI_DATA0_P/ MDDI_DATA0_M, MDDI_DATA1_P/ MDDI_DATA1_M),.

The specifications of MDDI supported by the ILI9806G are compatible to the MDDI specifications disclosed by VESA, Video Electronics Standards Association. The following are the specifications particular to the ILI9806G's MDDI.

ILI9806G MDDI Specifications

- MDDI specification version V1.2 , support Type- II (2 Data Lanes)
- High-speed, differential, small-amplitude data transfer via Stb+/-, Data0+/-, Data1+/- lines
- MDDI client: the ILI9806G enables direct connection to the base band (BB) chip without bridge chip
- Cost-performance optimized interface for mobile display systems
 1. Only internal mode (one client) and Forward Link are supported
 2. Hibernation mode to save power consumption
 3. Tearing-free moving picture display via TE/VSYSNC interface
 4. Moving picture display with low power consumption, realized by the features 2 ~ 3
 5. Shutdown mode for saving power consumption in the standby state



Notes:

1. An external end resistor of 100 ohm is necessary between Data+ and Data- lines

2. Make the COG wiring resistances of Data+/-, Stb+/- lines as small as possible (RCOG < 10 ohm).

MDDI Link Protocol (Packets Supported by the ILI9806G)

The MDDI Link Protocol of the ILI9806G is compliant with the MDDI specifications disclosed by VESA. See the MDDI specifications by VESA for details on the MDDI Link Protocol.

The MDDI packets supported by the ILI9806G are listed in Table 41.

The MDDI packets supported by the ILI9806G are as follows. Do not send packets not supported by the ILI9806G in the system incorporating the ILI9806G.

Refer to MDDI packet structure, sub-frame header packet is placed in front of a sub-frame and some sub-frame construct media-frame together. The following table describes 10 types of packet which is supported in ILI9806G.

Table 41: List of Supported MDDI Packets

Packet	Function	Direction
Sub-frame header packet	Header of each sub frame	Forward
Register access packet	Register setting	Forward
Video stream packet	Video data transfer	Forward
Filler packet	Fill empty packet space	Forward
Reverse link encapsulation packet	Reverse data packet	Reverse
Round-trip delay measurement packet	Host->client->host delay check	Forward/Reverse
Client capability packet	Capability of client check	Reverse
Client request and status packet	Information about client status	Reverse
Forward link skew calibration packet	Propagation delay calibration	Forward
Link shutdown packet	End of frame	Forward

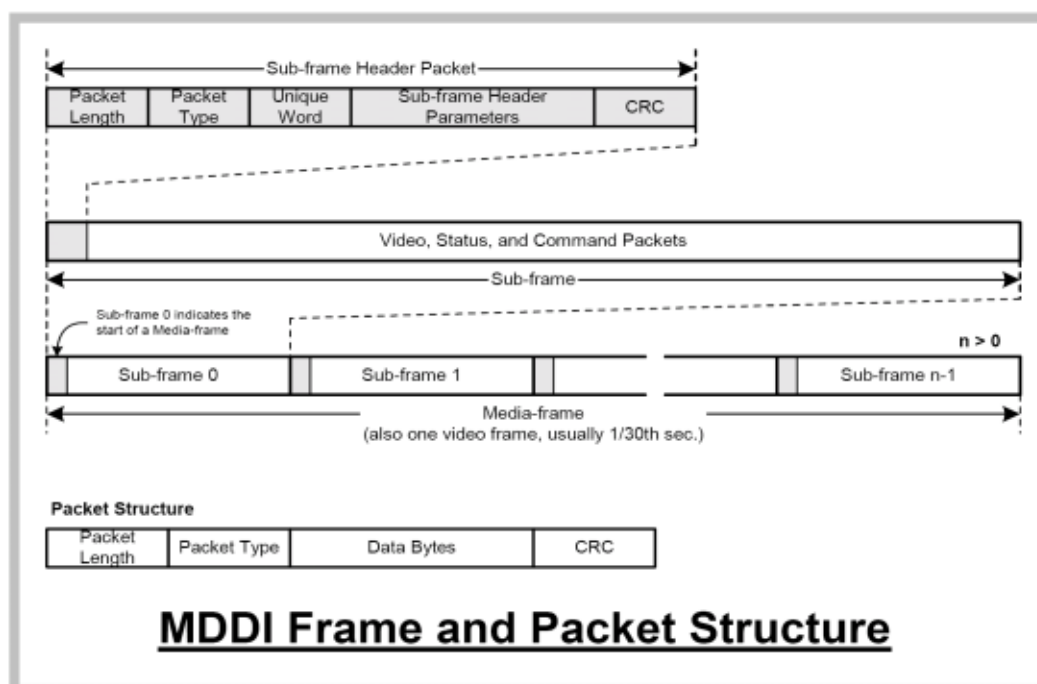


Figure 116: Forward Link Structure

Sub-frame Header Packet

The Sub-Frame Header Packet is the first packet of every sub-frame.

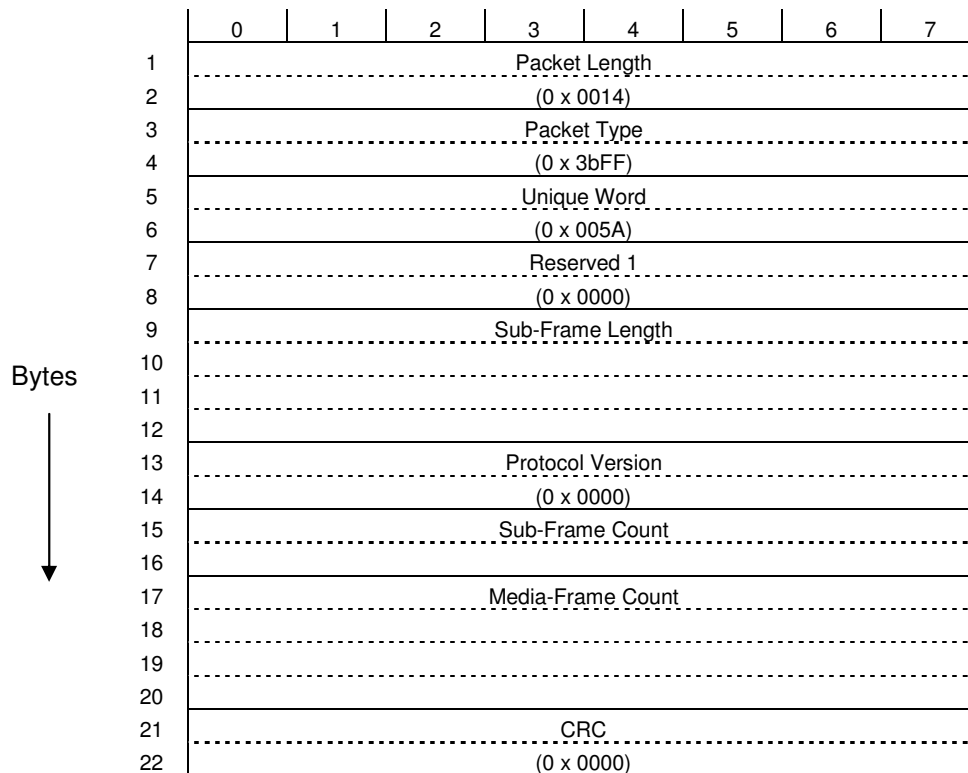
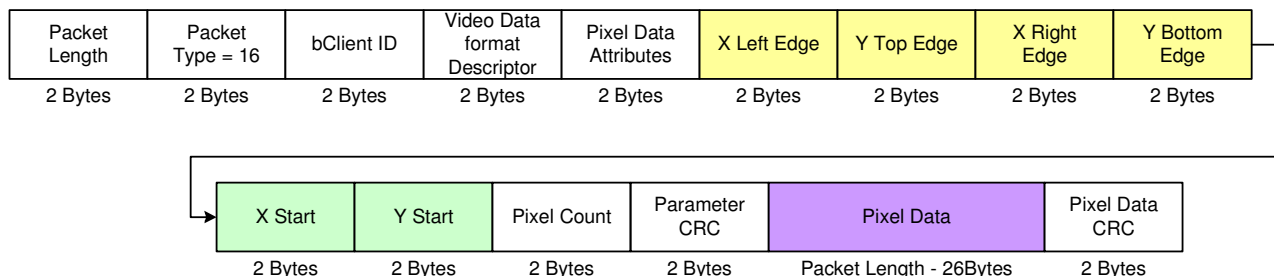


Figure 117: Sub-Frame Header Packet

Video Stream Packet

The ILI9806G writes image data to the RAM via Video Stream Packet. The window and RAM addresses are set via Register Access Packet.



	0	1	2	3	4	5	6	7
1	Packet Length							
2								
3	Packet Type							
4	(0x0010)							
5	bClient ID							
6	(0 x 0000)							
7	Video Data Format Descriptor							
8								
9	Bit0	Bit1	Pixel Data Attributes					
10								
11	X Left Edge							
12								
13	Y Top Edge							
14								
15	X Right Edge							
16								
17	Y Bottom Edge							
18								
19	X Start							
20								
21	Y Start							
22								
23	Pixel Count							
24								
25	Parameter CRC							
26								
	Pixel Data (Packet Length - 26 bytes)							
	CRC							

Figure 118: Example of Video Stream Packet Fields^{Note}

^{Note} The parameters colored in gray are not supported by the ILI9806G.

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Video Data Format Descriptor: This sets the pixel data format. 2 bytes that contain a 16-bit unsigned integer that specifies the format of each pixel in the Pixel Data in the present stream in the present packet.

The bits[15:13]=010: the video data consist of an array of color pixels in raw RGB format where the number of bits per pixel of red is defined by bits 11 through 8, the number of bits per pixel of green is defined by bits 7 through 4, and the number of bits per pixel of blue is defined by bits 3 through 0.

The bit 12=1: each pixel in Pixel Data is packed up against the previous pixel leaving no unused bits.

[15:13]	[12]	[11:8]	[7:4]	[3:0]	
010	1	0x5	0x6	0x5	Packed 16bpp RGB format (R:G:B = 5:6:5)
010	1	0x6	0x6	0x6	Packed 18bpp RGB format (R:G:B = 6:6:6)
010	1	0x8	0x8	0x8	Packed 24bpp RGB format (R:G:B = 8:8:8)
Others					Setting disabled

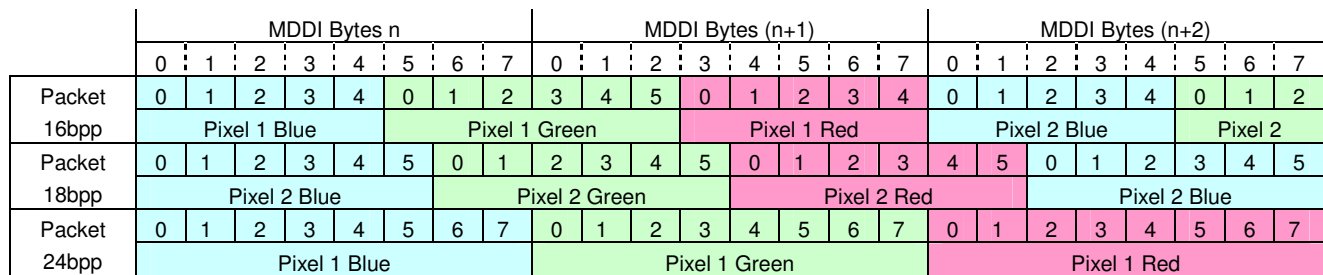


Figure 119: Video Data Format

Pixel Data Attributes: the image data sent via Video Stream Packet is recognized as the data written in the ILI9806G according to the setting in [1:0] bits in this field.

Table 42: Pixel Data Attributes

Pixel Data Attributes	Bits [1:0]	Description
0 x 0000	00	Setting disabled
0 x 0001	01	Setting disabled
0 x 0002	10	Setting disabled
0 x 0003	11	The Video Stream Packet data is recognized as the data written in the ILI9806G.

Register Access Packet

The Register Access Packet is used when setting instructions to the ILI9806G. (detail see below example).

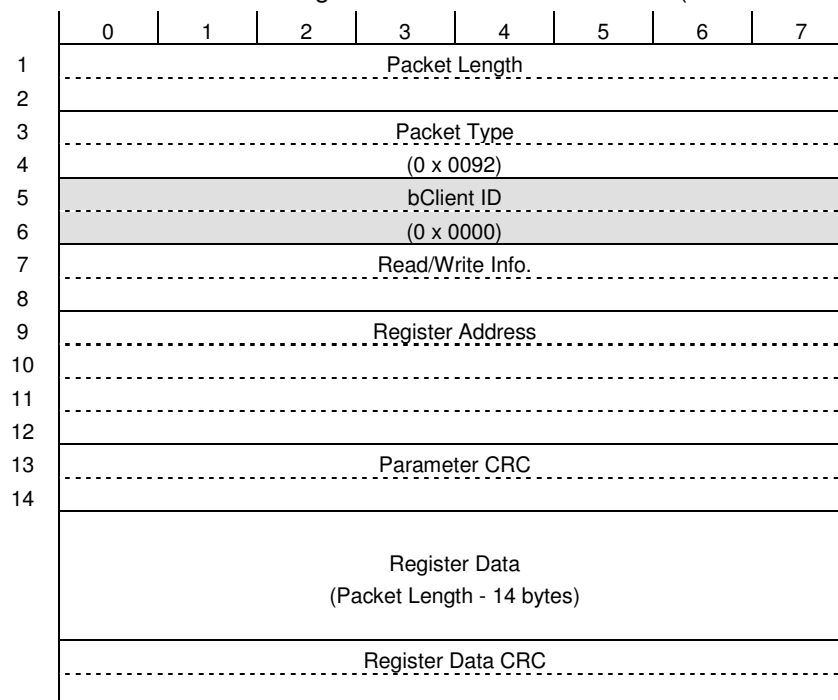


Figure 120: Register Access Packet^{Note}

Read/Write Info: Read or Write information in register access. The ILI9806G supports the following access setting.

Bits [15:14]	Bits [13:00]	Description
2'b00	0 x n	Write one register by register access packet
2'b01	0 x n	Reserved
2'b10	0 x n	Read one register by register access packet
2'b11	0 x n	Response to read

Register Address: The index of the register to be accessed is set in the Register Address area, and the Register Address Packet is directed to the ILI9806G, or the sub display as determined by the setting in the Register Address area.

Bits [31:16]	Description
16'h0000	The Register Access Packet is directed to the ILI9806G via the main-display interface.
16'h0001 ~ 16'h7FFF	Setting disabled

Bits [15:0]	Description
16'h0000~16'h FFFF	Bits [15:0] are used as index [15:0].

Register Data: The data for register access is written in the Register Data area. The length of the Register Data Packet depends on the parameter length of the command.

^{Note} The parameters colored in gray are not supported by the ILI9806G.

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	0	1	2	3	4	5	6	7
1	Packet Length					(0 x 16)		
2						(0 x 00)		
3	Packet Type					(0 x 92)		
4						(0 x 00)		
5	bClient ID					(0 x 00)		
6						(0 x 00)		
7	Read/Write Info.					(0 x 01)		
8						(0 x 00)		
9	Register Address					(index ID [7:0])		
10						(index ID [15:8])		
11						(0 x 00) → Main Panel (ILI9806G)		
12						(0 x 00)		
13	Parameter CRC							
14								
15	Register Data List (Various Length)					1 st Parameter		
16						0 x 00		
17						0 x 00		
18						0 x 00		
19						2 nd Parameter		
20						0 x 00		
21						0 x 00		
22						0 x 00		
23	Parameter CRC							
24								

Figure 121: Example of Register Access Packet (write to the ILI9806G)^{Note}

Register Access Packet Restrictions

The internal RAM of the ILI9806G is accessible via the Video Stream Packet. RAM access data is not included in the Register Access Packet.

^{Note} The parameters colored in gray are not supported by the ILI9806G.

Link Shutdown Packet

The Link Shutdown Packet is sent from the host to the client to indicate that the MDDI data transmission and strobe will be shut down and go into a low-power hibernation state.

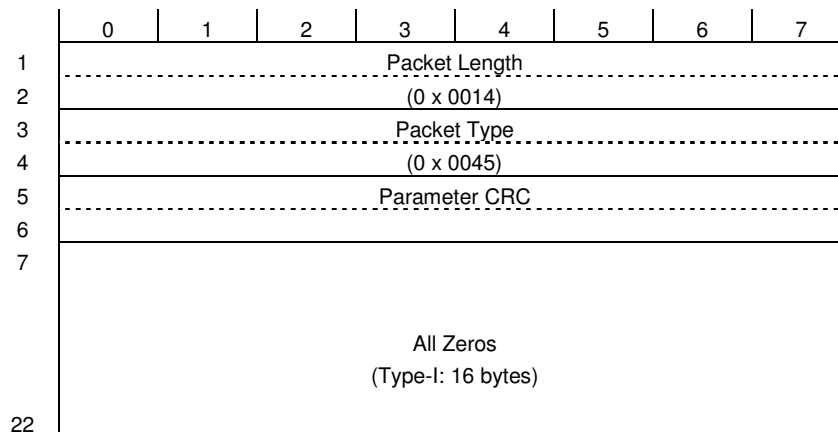


Figure 122: Link Shutdown Packet

Filler Packet

A Filler Packet is sent when no other information is available to be sent on the forward or reverse link.

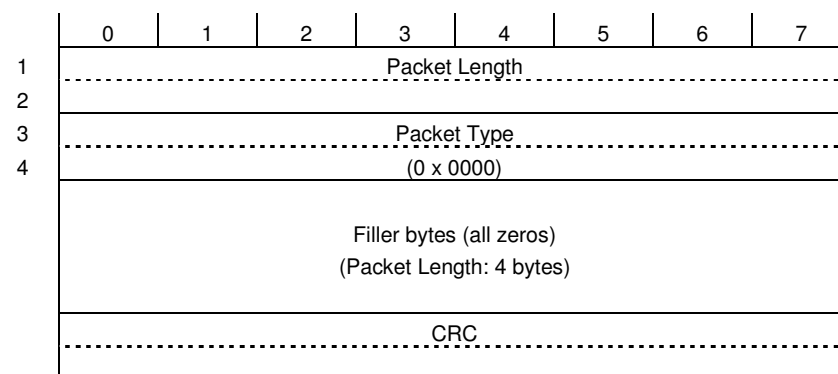


Figure 123: Filler Packet

Hibernation Setting

The client MDDI supports the Hibernation setting. There are two ways to cancel the Hibernation setting selected according to the condition of use. The two cancellation methods are listed below and described in detail in the following page.

Hibernation Cancellation	
Method	Description
Host-initiated wake up	In power-saving mode such as standby
TE-initiated wake up	Reduced power consumption in transferring moving picture data Host-initiated wake up triggered by the output from TE.

The Hibernation setting and cancellation sequence must be compatible with the VESA-MDDI specifications.

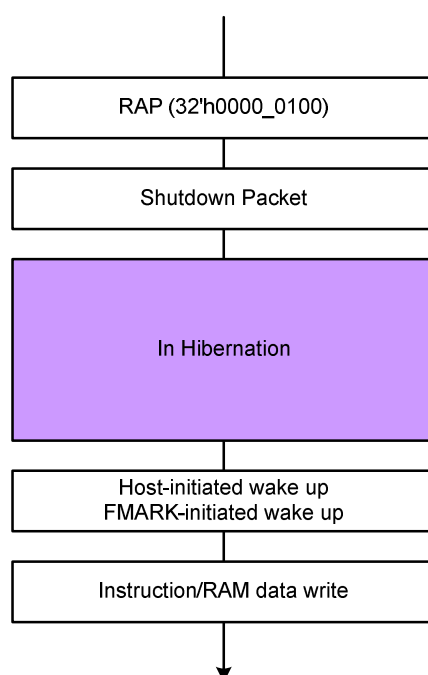


Figure 124: Hibernation Mode Sequence

The host initiated wake up is described below without contention from the client trying to wake up at the same time. The following sequence of events is illustrated in the figure below.

- A. The host sends a Link Shutdown Packet to inform the client that the link will transition to the low power hibernation state.
- B. Following the CRC of the Link Shutdown Packet, the host toggles MDDI_Stb for 64 cycles to allow processing in the client to finish before it stops MDDI_Stb from toggling which stops the recovered clock in the client device. During the interval, the host initially sets MDDI_Data0 to the logical zero level, and then disables the MDDI_Data0 output in the range of 16 to 48 MDDI_Stb cycles (including output disable propagation delays) after the CRC. It may be desirable for the client to place its high-speed receivers for MDDI_Data0 and MDDI_Stb into a low power state any time after 48 MDDI_Stb cycles after the CRC and before point C.
- C. The host enters the low power hibernation state by disabling the MDDI_Data0 and MDDI_Stb drivers and by placing the host controller into a low power hibernation state. It is also allowable for MDDI_Stb to be driven to the logical zero level or to continue toggling during hibernation. The client is also in the low power hibernation state.
- D. After a while, the host begins the line restart sequence by enabling the MDDI_Data0 and MDDI_Stb driver outputs. The host drives MDDI_Data0 to the logical one level and MDDI_Stb to the logical zero level for at least 200nsec after MDDI_Data0 reaches the valid logical one level and MDDI_Stb reaches the valid logical zero level before driving pulses on MDDI_Stb. This gives the client sufficient time to prepare to receive high speed pulses on MDDI_Stb. The client first detects the wake up pulse using a low power differential receiver having a +125mV input offset voltage.
- E. The host drivers are fully enabled and MDDI_Data0 is being driven to the logical one level. The host begins to toggle MDDI_Stb in a manner consistent with having the logical zero level on MDDI_Data0 for a duration of 150 MDDI_Stb cycles.
- F. The host drives MDDI_Data0 to the logical zero level for 50 MDDI_Stb cycles. The client begins to look for the Sub frame Header Packet after MDDI_Data0 is at the logical zero level for 40 MDDI_Stb cycles.
- G. The host begins to transmit data on the forward link by sending a Sub-frame Header packet. Beginning at point G the MDDI host generates MDDI_Stb based on the logic level on MDDI_Data0 so that proper data-strobe encoding commences from point G.

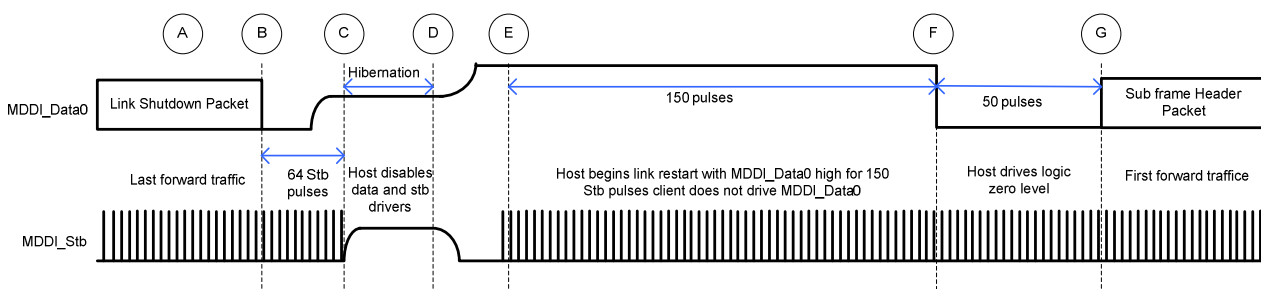


Figure 125: Host Initiated Wake-up without Contention

3.14. Display Data Format

3.14.1. 3-line Serial Interface

The 3-line/9-bit serial bus interface of the ILI9806G can be used by setting the external pin IM [3:0] to X011.

The Figure 126 is an interface with 8080 MPU system interface.

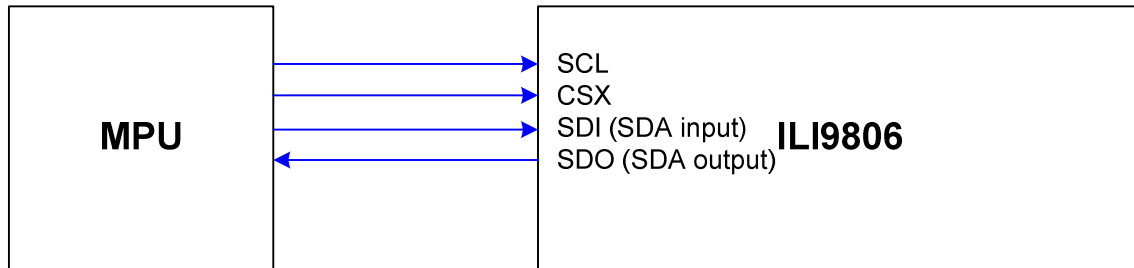


Figure 126: 3-line Serial Interface

The display data formats available for this type of color depth are:

- 65K-Colors, RGB 5, 6, 5 bits input data (Set Standard Command 3Ah, DBI [2:0] = 101)
- 262K-Colors, RGB 6, 6, 6 bits input data (Set Standard Command 3Ah, DBI [2:0] = 110)
- 16.7M colors, RGB 8, 8, 8 bits input (Set Standard Command 3Ah, DBI [2:0] = 111)

3.14.2. SPI Data for 3-bit/pixel (RGB 1-1-1 bits input), 8-color

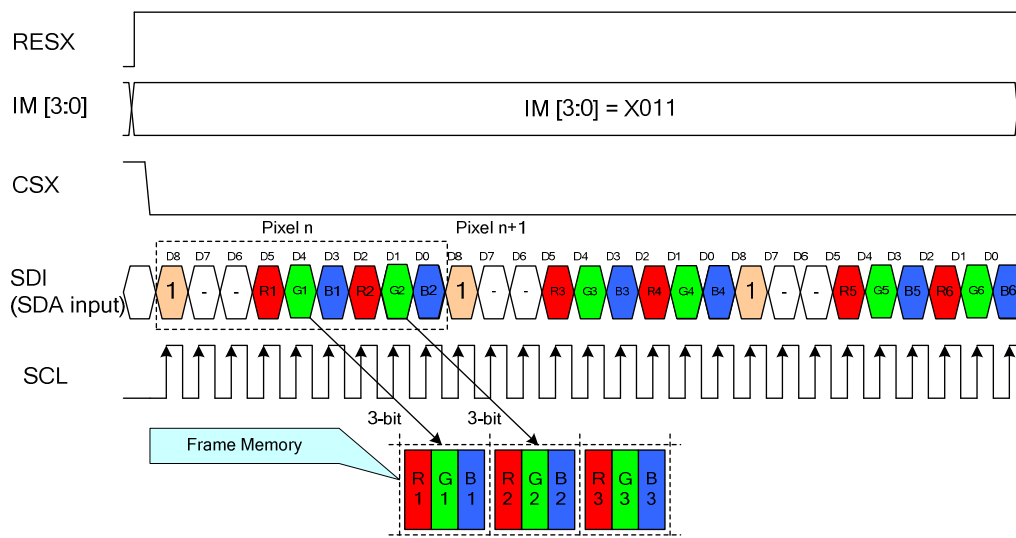


Figure 127: SPI Data for 3-bit/pixel (RGB 1-1-1 bits input), 8-color

Notes:

1. One pixel data contains 3-bit color depth information.
2. '-' = void

3.14.3. SPI Data for 16-bit/pixel (RGB 5-6-5 bits input), 65K-color

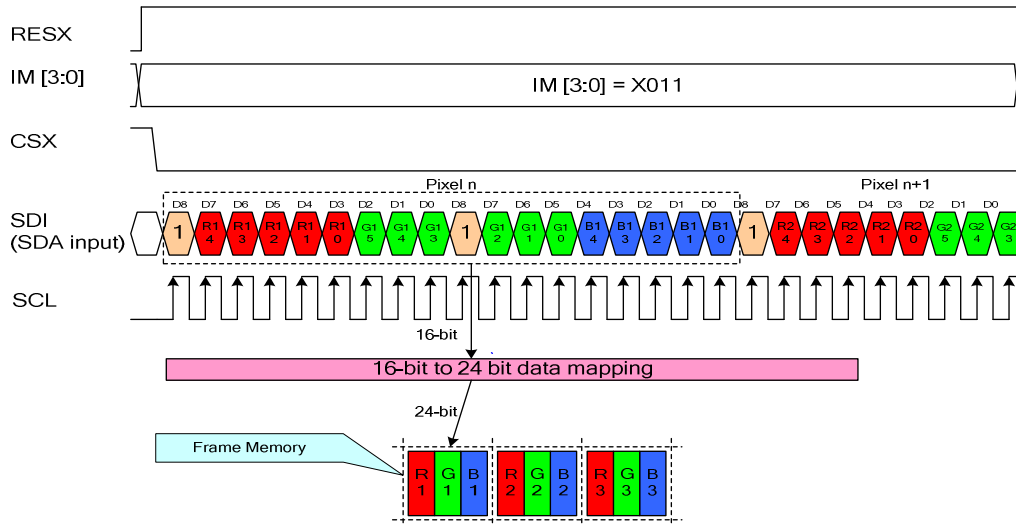


Figure 128: SPI Data for 16-bit/pixel (RGB 5-6-5 bits input), 65K-color

Notes:

1. One pixel data contains 16-bit color depth information.
2. The most significant bits are: R x 4, G x 5 and B x 4.
3. The least significant bits are: R x 0, G x 0 and B x 0.

3.14.4. SPI Data for 18-bit/pixel (RGB 6-6-6 bits input), 262K-color

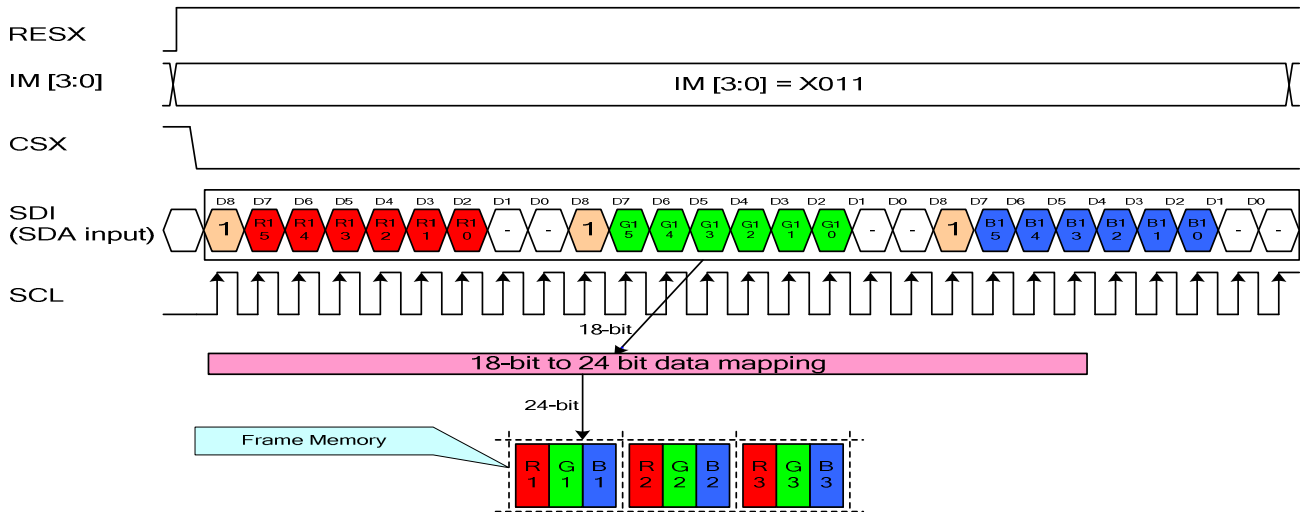


Figure 129: SPI Data for 18-bit/pixel (RGB 6-6-6 bits input), 262K-color

Notes:

1. One pixel data contains 18-bit color depth information.
2. The most significant bits are: R x 5, G x 5 and B x 5.
3. The least significant bits are: R x 0, G x 0 and B x 0.
- 4: '-' = void

3.14.5. SPI Data for 24-bit/pixel (RGB 8-8-8 bits input), 16.7M-color

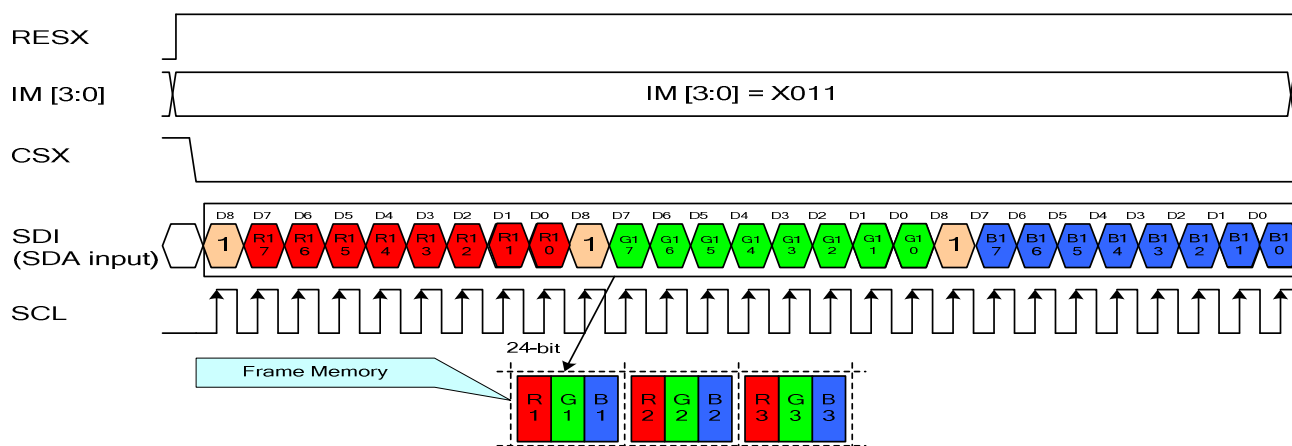


Figure 130: SPI Data for 24-bit/pixel (RGB 8-8-8 bits input), 16.7M-color

Notes:

1. One pixel data contains 24-bit color depth information.
2. The most significant bits are: R x 7, G x 7 and B x 7.
3. The least significant bits are: R x 0, G x 0 and B x 0.

Read data through 3-line SPI mode

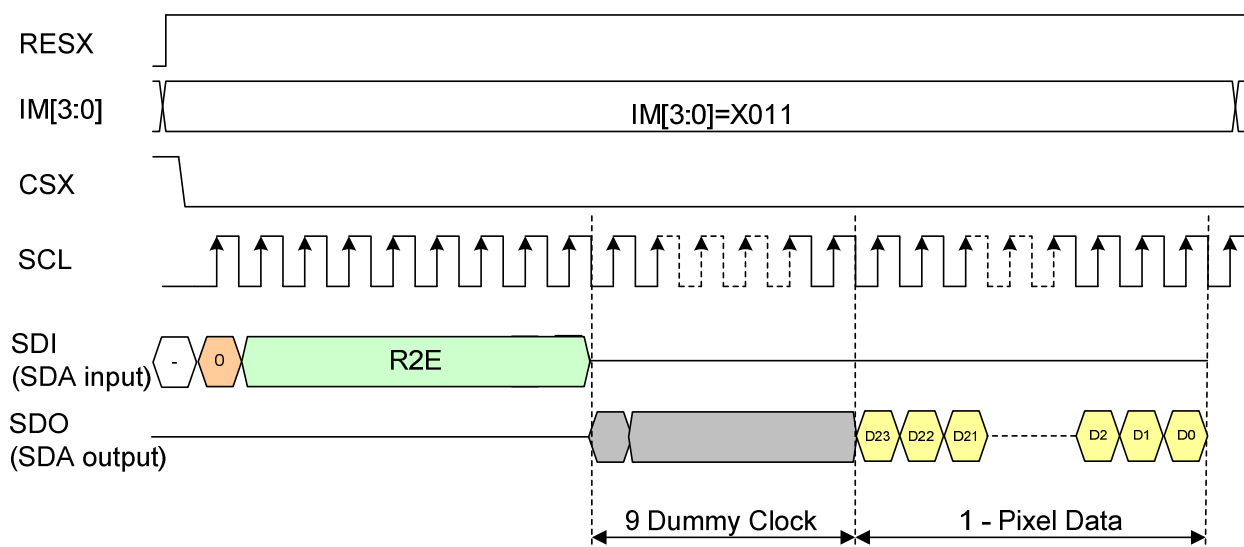


Figure 131: 3-line SPI Mode Read Data

Note: '-' = void

3.14.6. 8-bit Parallel MPU Interface

The DBI TYPE B 8-bit parallel bus interface of the ILI9806G can be used by setting the external pin IM [3:0] to 0000.

The Figure 132 shows this system interface.

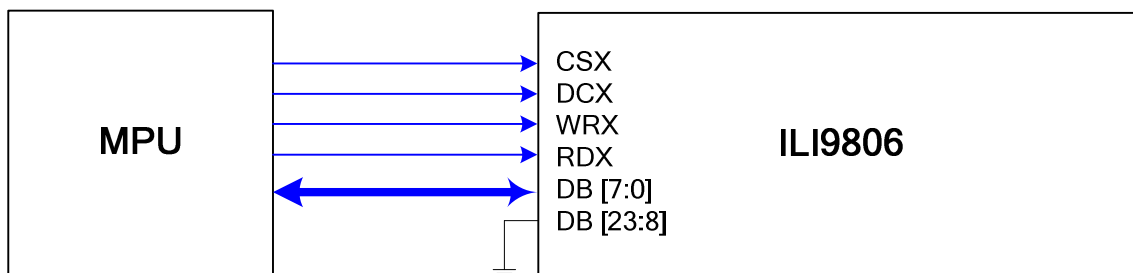


Figure 132: 8-bit Parallel MPU Interface

The display data formats available for this type of color depth are:

- 65K-Colors, RGB 5, 6, 5 bits input data (Set Standard Command 3Ah, DBI [2:0] = 101)
- 262K-Colors, RGB 6, 6, 6 bits input data (Set Standard Command 3Ah, DBI [2:0] = 110)
- 16.7M-Colors, RGB 8, 8, 8 bits input data (Set Standard Command 3Ah, DBI [2:0] = 111)

3.14.7. 8-bit Data Bus for 16-bit/pixel (RGB 5-6-5 bits input), 65K-color

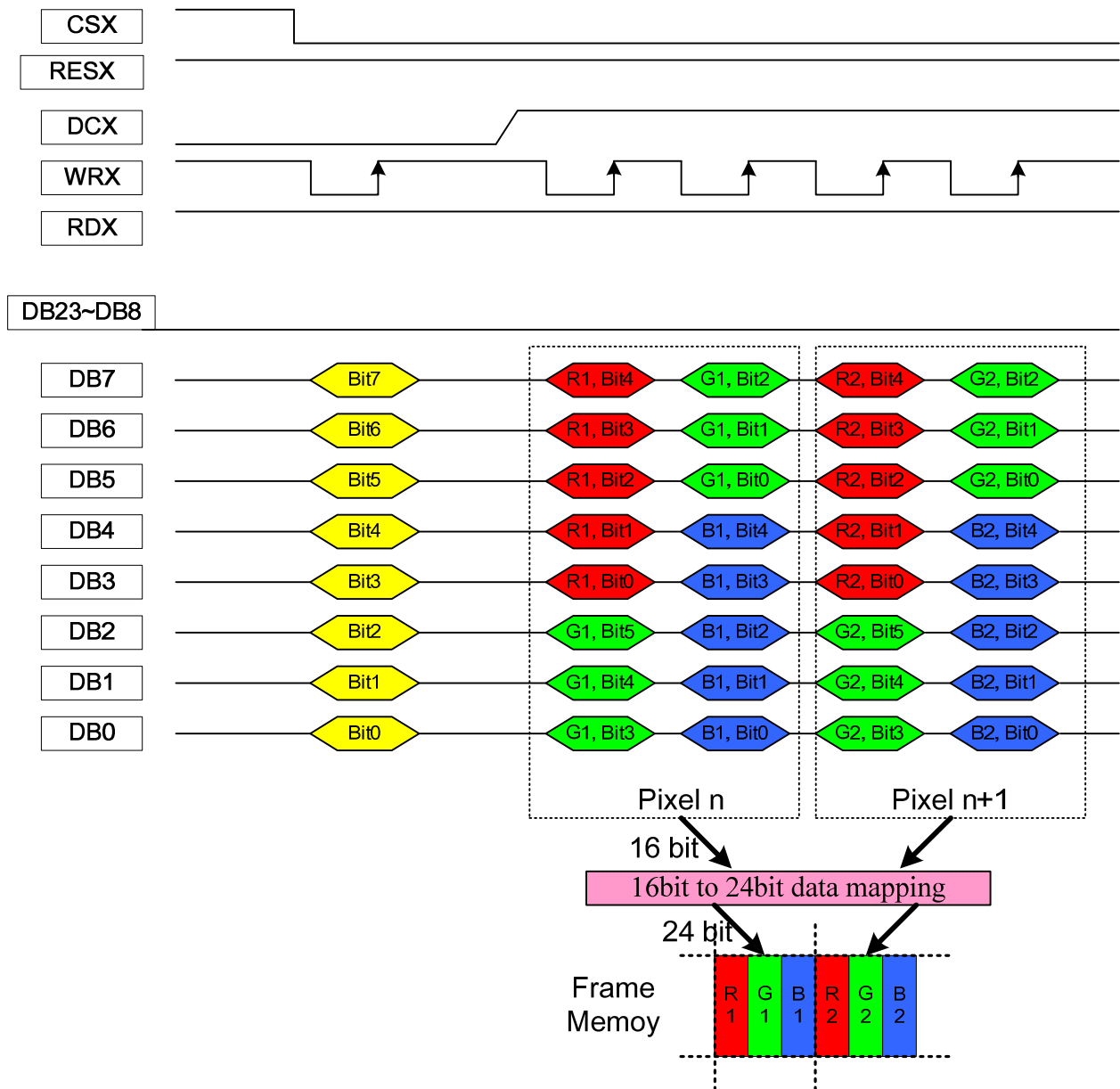


Figure 133: 8-bit Data Bus for 16-bit/pixel (RGB 5-6-5 bits input), 65K-color

Notes:

1. The data order is as follows: MSB = DB7, LSB = DB0 and picture data is MSB = Bit 5, LSB = Bit 0 for Green data and MSB = Bit 4, LSB = Bit 0 for Red and Blue data.
2. 2-times transfer is used to transmit 1 pixel data to the 16-bit color depth information.
3. '-' = void

3.14.8. 8-bit Data Bus for 18-bit/pixel (RGB 6-6-6 bits input), 262K-color

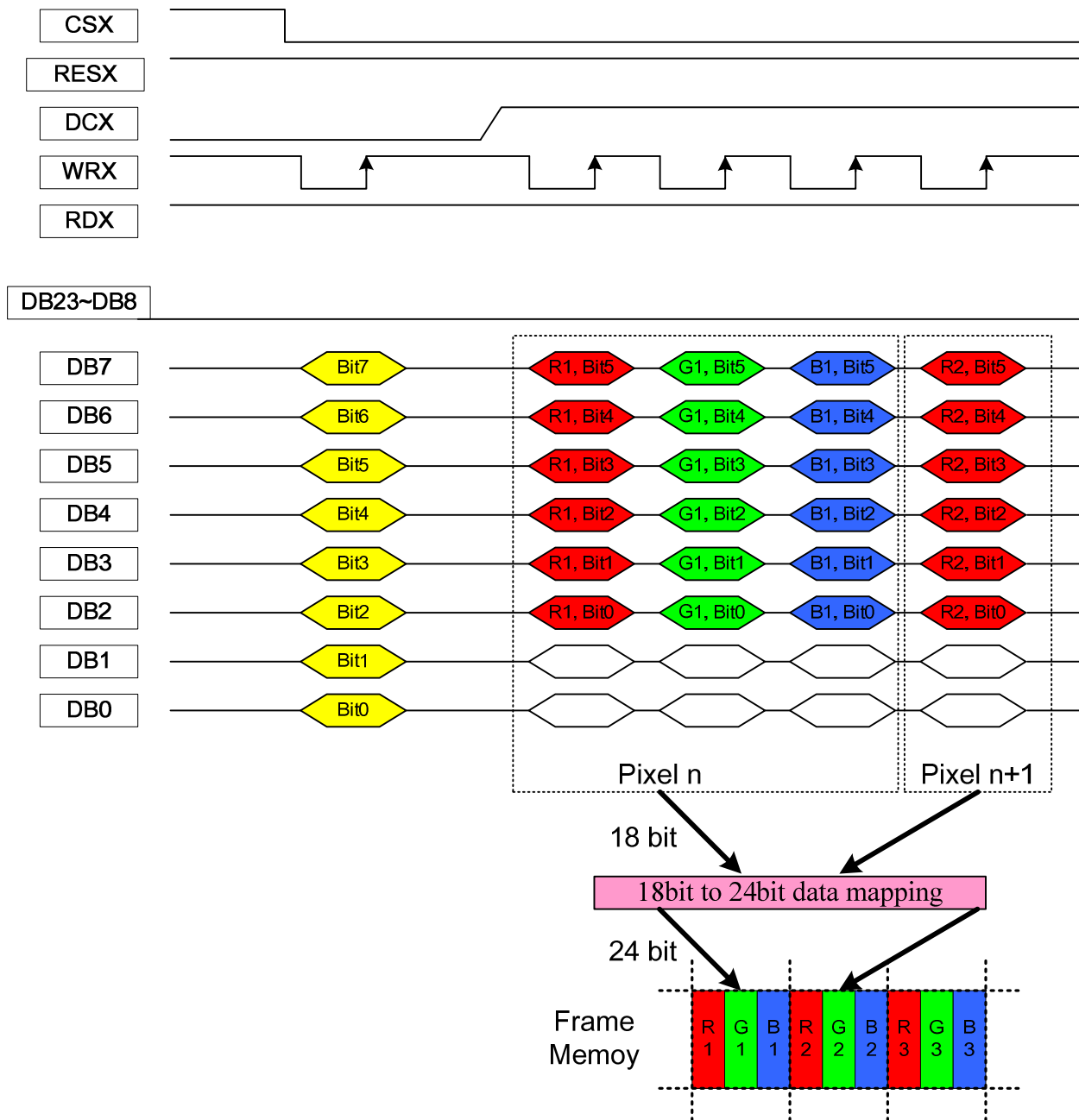


Figure 134: 8-bit Data Bus for 18-bit/pixel (RGB 6-6-6 bits input), 262K-color

Notes:

1. The data order is as follows: MSB = DB7, LSB = DB0 and picture data is MSB = Bit 5, LSB = Bit 0 for Green, Red and Blue data.
2. 3-times transfer is used to transmit 1 pixel data to the 18-bit color depth information.
3. '-' = void

3.14.9. 8-bit Data Bus for 24-bit/pixel (RGB 8-8-8 bits input), 16.7M-color

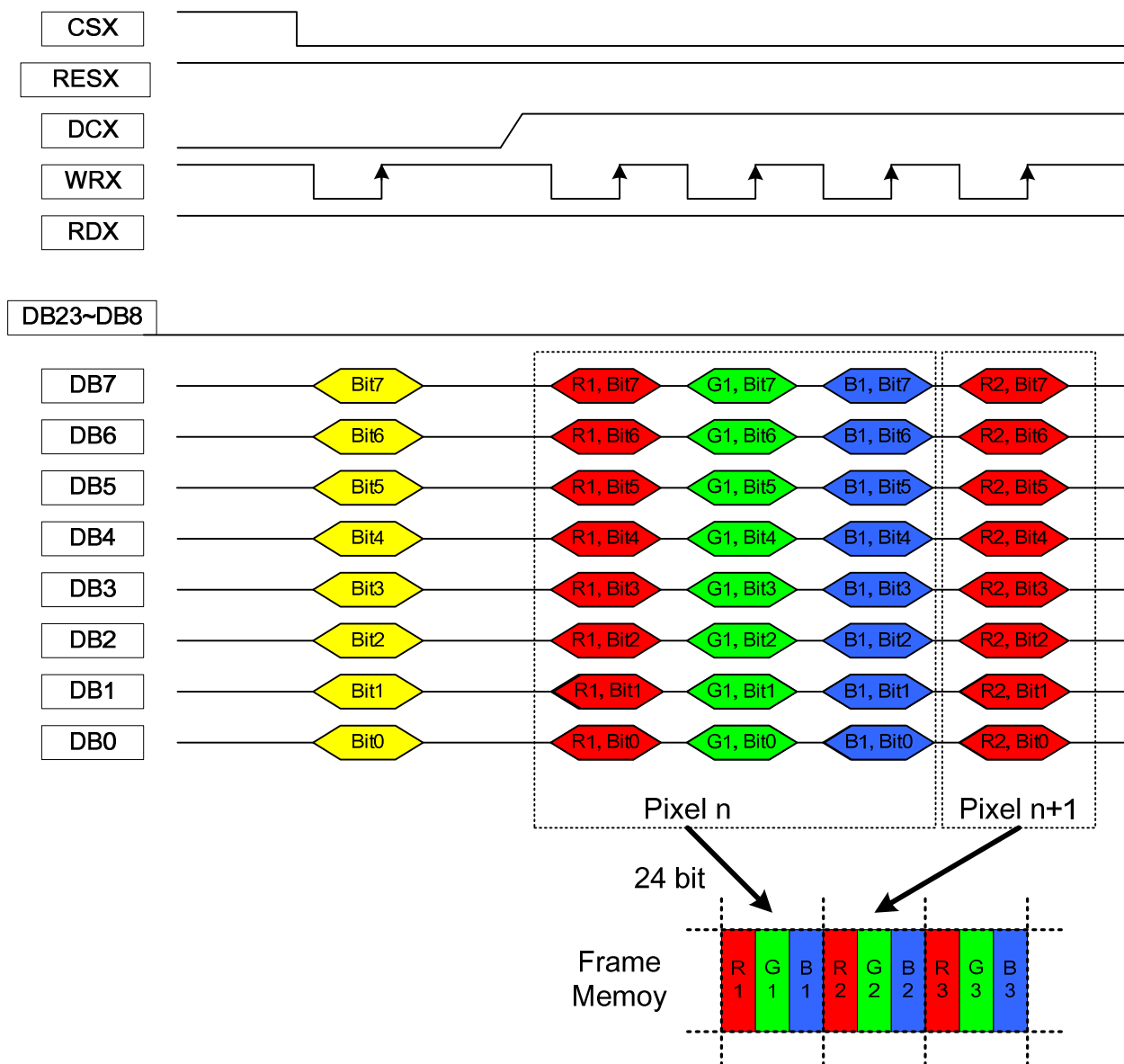


Figure 135: 8-bit Data Bus for 24-bit/pixel (RGB 8-8-8 bits input), 16.7M-color

Notes:

1. The data order is as follows: MSB = DB7, LSB = DB0 and picture data is MSB = Bit 7, LSB = Bit 0 for Green, Red and Blue data.
2. 3-times transfer is used to transmit 1 pixel data to the 24-bit color depth information.
3. '-' = void

3.14.10. 9-bit Parallel MPU Interface

The DBI TYPE B 9-bit parallel bus interface of the ILI9806G can be used by setting the external pin IM [3:0] to 1100.

The Figure 136 shows this system interface.

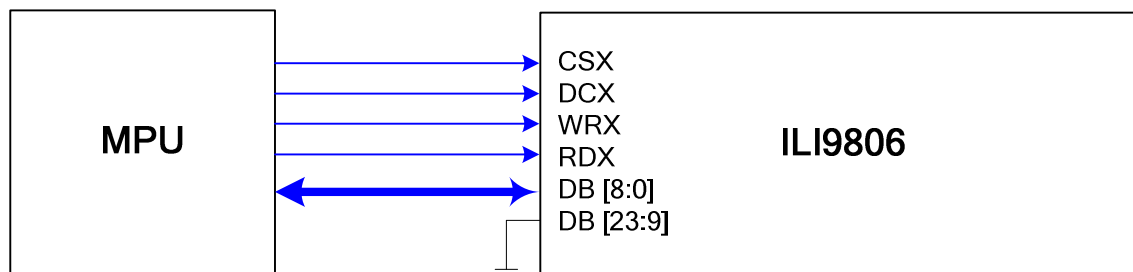


Figure 136: 9-bit Parallel MPU Interface

The display data formats available for this type of color depth are:

- 65K-Colors, RGB 5, 6, 5 bits input data (Set Standard Command 3Ah, DBI [2:0] = 101)
- 262K-Colors, RGB 6, 6, 6 bits input data (Set Standard Command 3Ah, DBI [2:0] = 110)
- 16.7M-Colors, RGB 8, 8, 8 bits input data (Set Standard Command 3Ah, DBI [2:0] = 111)

3.14.11. 9-bit Data Bus for 16-bit/pixel (RGB 5-6-5 bits input), 65K-color

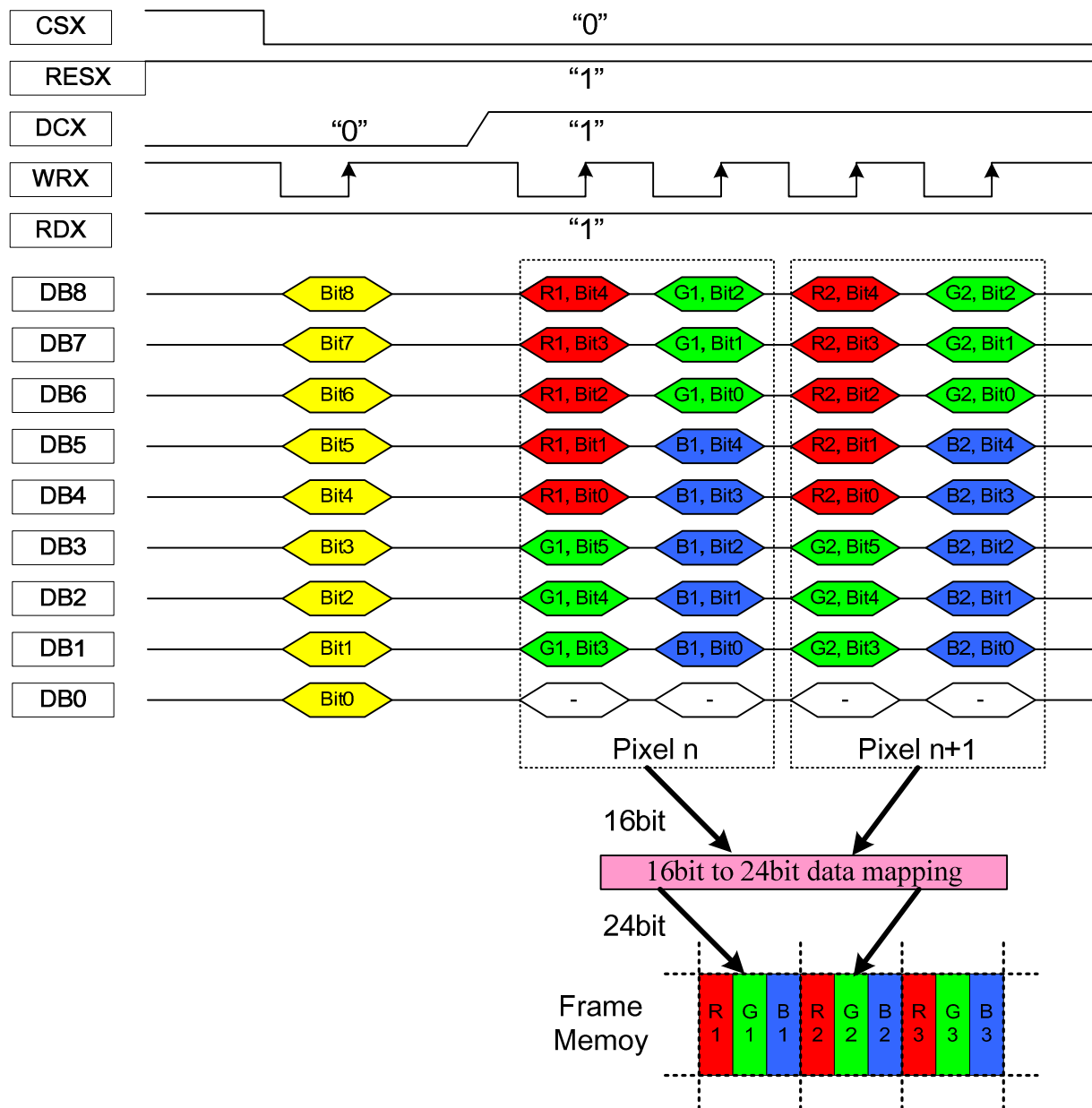


Figure 137: 9-bit Data Bus for 16-bit/pixel (RGB 5-6-5 bits input), 65K-color

Notes:

1. The data order is as follows: MSB = DB8, LSB = DB0, and picture data is MSB = Bit 5, LSB = Bit 0 for Green, MSB = Bit 4, LSB = Bit 0 for Red and Blue data.
2. 2-times transfer is used to transmit 1 pixel data to the 16-bit color depth information.
3. '-' = void

3.14.12. 9-bit Data Bus for 18-bit/pixel (RGB 6-6-6 bits input), 262K-color

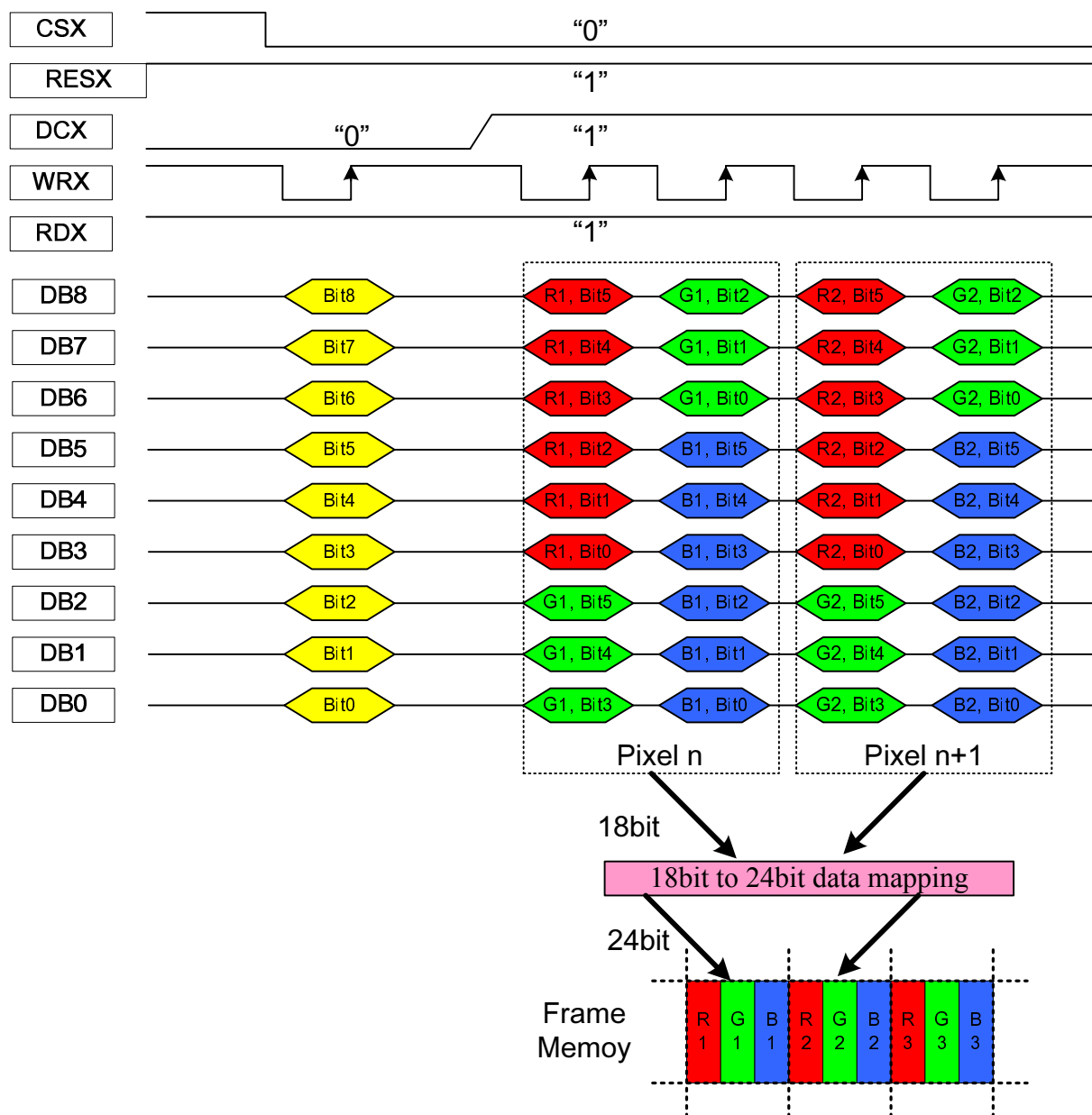


Figure 138: 9-bit Data Bus for 18-bit/pixel (RGB 6-6-6 bits input), 262K-color

Notes:

1. The data order is as follows: MSB = DB8, LSB = DB0, and picture data is MSB = Bit 5, LSB = Bit 0 for Green, Red and Blue data.
2. 2-times transfer is used to transmit 1 pixel data to the 18-bit color depth information.
3. '-' = void

3.14.13. 9-bit Data Bus for 24-bit/pixel (RGB 8-8-8 bits input), 16.7M-color

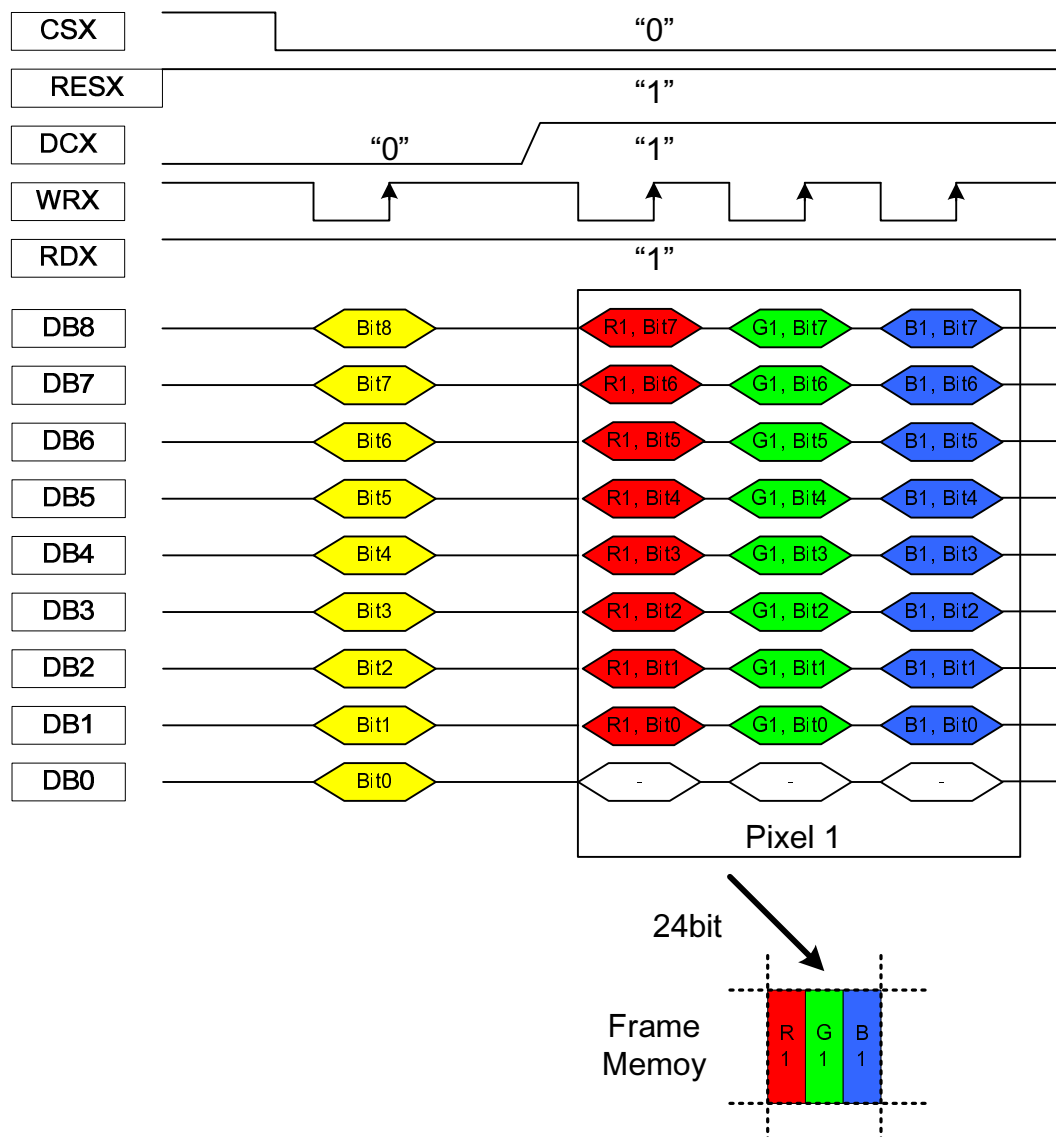


Figure 139: 9-bit Data Bus for 24-bit/pixel (RGB 8-8-8 bits input), 16.7M-color

Notes:

1. The data order is as follows: MSB = DB8, LSB = DB0, and picture data is MSB = Bit 7, LSB = Bit 0 for Green, Red and Blue data.
2. 3-times transfer is used to transmit 1 pixel data to the 24-bit color depth information.
3. '-' = void

3.14.14. 16-bit Parallel MPU Interface

The DBI TYPE B 16-bit parallel bus interface of the ILI9806G can be used by setting the external pin IM [3:0] to 0001. The Figure 140 shows this system interface.

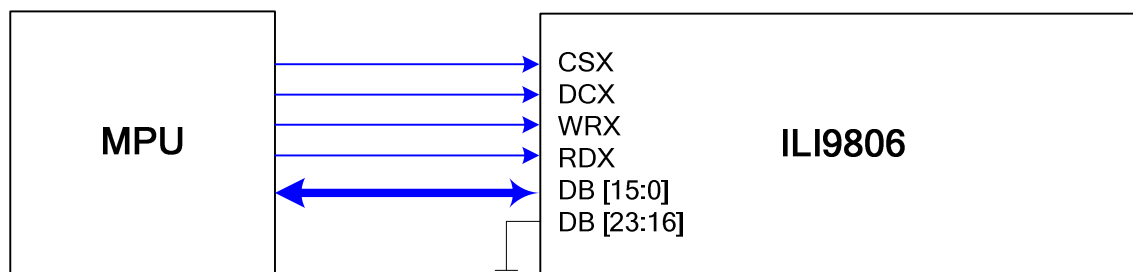


Figure 140: 16-bit Parallel MPU Interface

The display data formats available for this type of color depth are:

- 65K-Colors, RGB 5, 6, 5 bits input data (Set Standard Command 3Ah, DBI [2:0] = 101)
- 262K-Colors, RGB 6, 6, 6 bits input data (Set Standard Command 3Ah, DBI [2:0] = 110)
- 16.7M-Colors, RGB 8, 8, 8 bits input data (Set Standard Command 3Ah, DBI [2:0] = 111)

3.14.15. 16-bit Data Bus for 16-bit/pixel (RGB 5-6-5 bits input), 65K-color

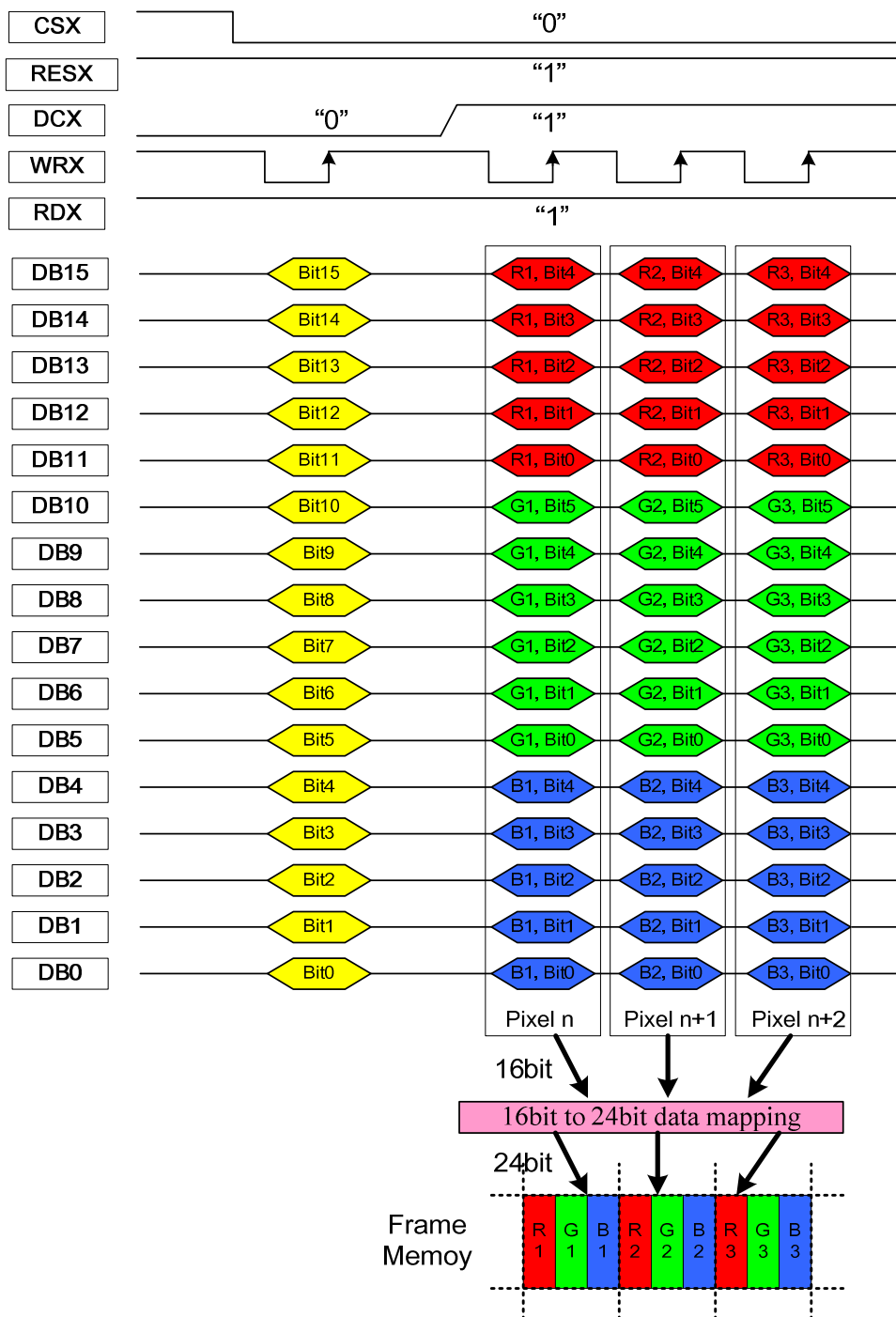


Figure 141: 16-bit Data Bus for 16-bit/pixel (RGB 5-6-5 bits input), 65K-color

Notes:

1. The data order is as follows: MSB = DB15, LSB = DB0 and picture data is MSB = Bit 5, LSB = Bit 0 for Green data and MSB = Bit 4, LSB = Bit0 for Red and Blue data.
2. 1-time transfer is used to transmit 1 pixel data to the 16-bit color depth information.
3. '-' = void

3.14.16. 16-bit Data Bus for 18-bit/pixel (RGB 6-6-6 bits input), 262K-color

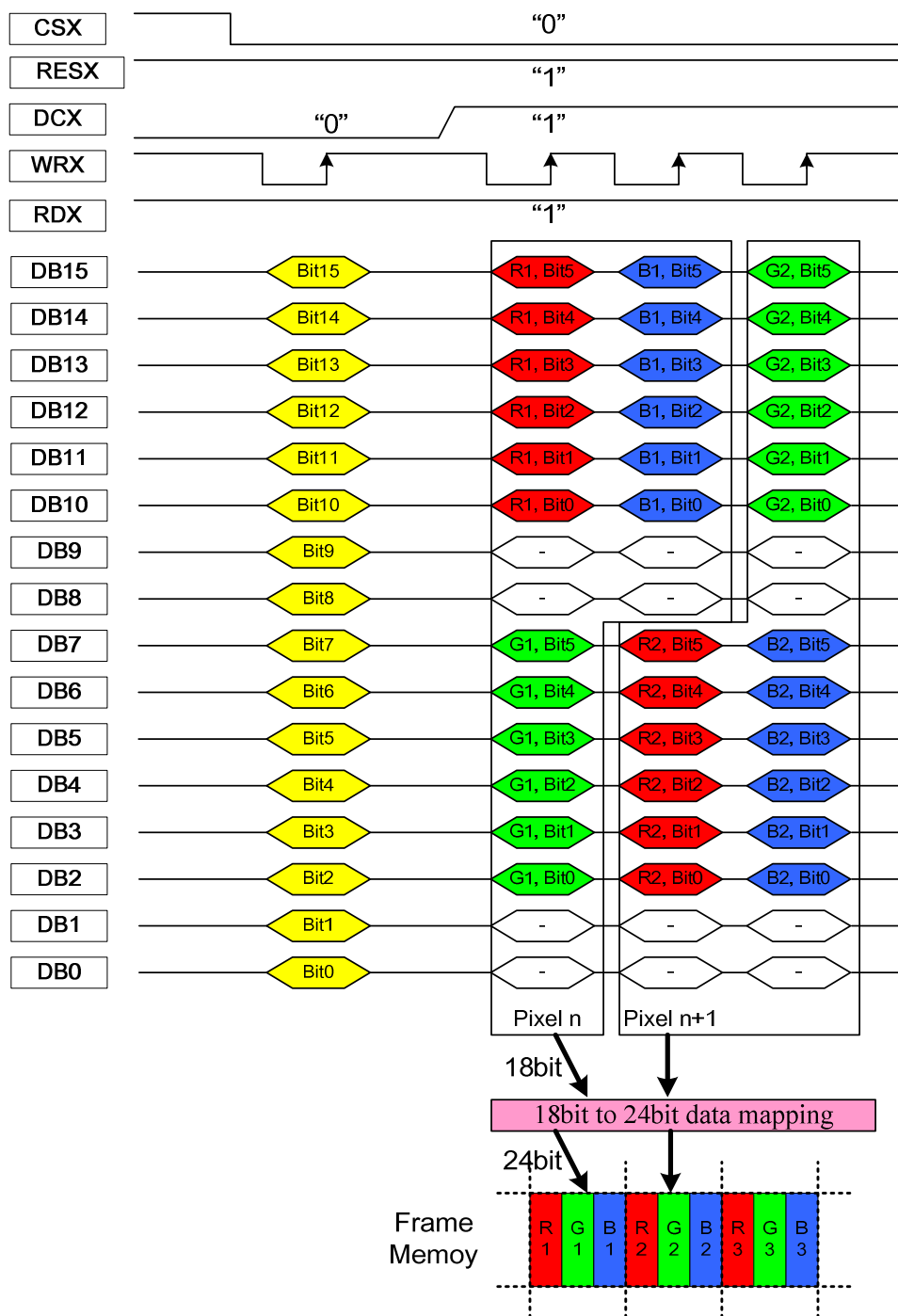


Figure 142: 16-bit Data Bus for 18-bit/pixel (RGB 6-6-6 bits input), 262K-color

Notes:

1. The data order is as follows: MSB = DB15, LSB = DB0, and picture data is MSB = Bit 5, LSB = Bit 0 for Green, Red and Blue data.
2. 3-times transfer is used to transmit 2 pixel data to the 18-bit color depth information.
3. '-' = void

3.14.17. 16-bit Data Bus for 24-bit/pixel (RGB 8-8-8 bits input), 16.7M-color

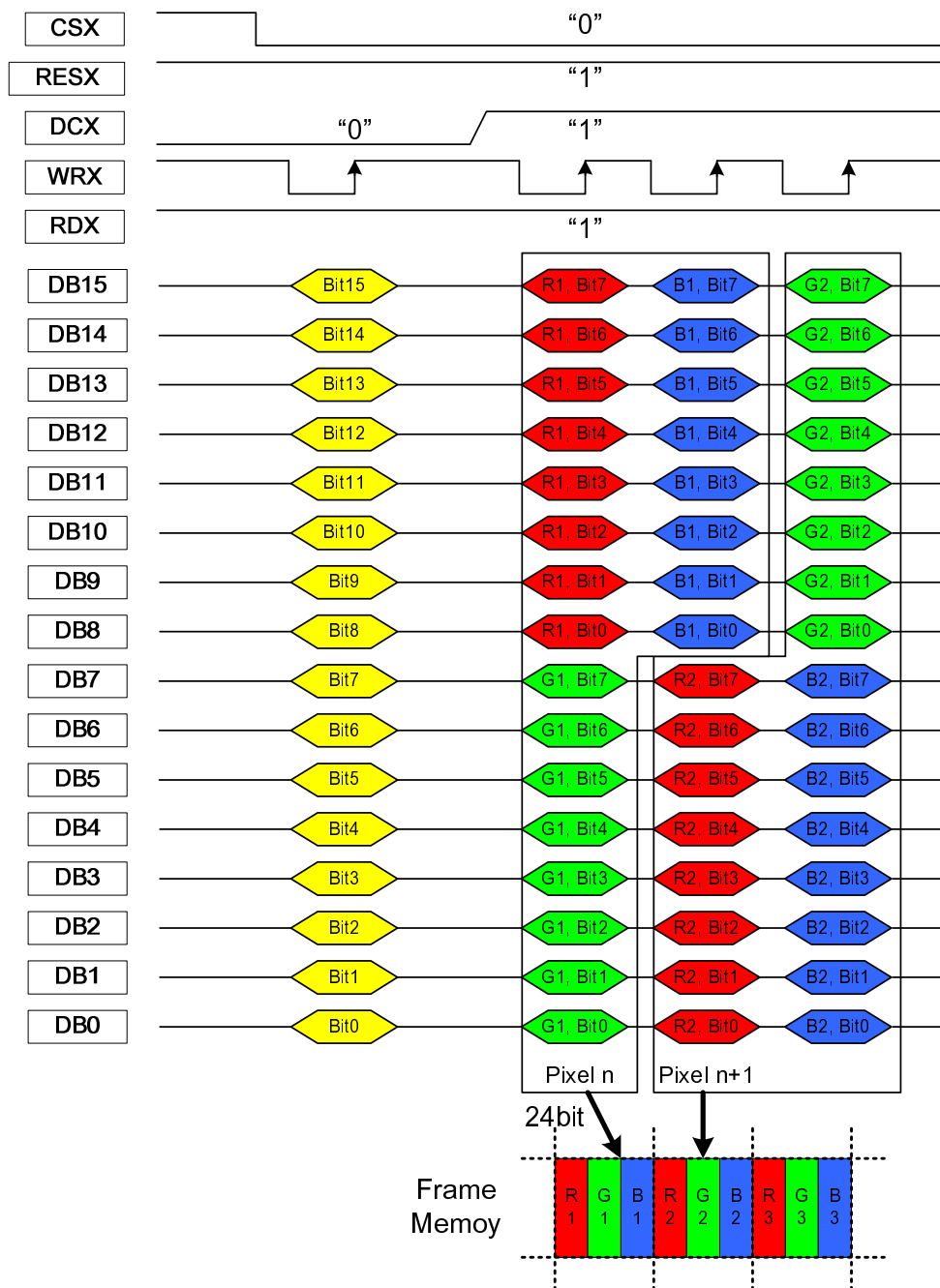


Figure 143: 16-bit Data Bus for 24-bit/pixel (RGB 8-8-8 bits input), 16.7M-color

Notes:

1. The data order is as follows: MSB = DB15, LSB = DB0, and picture data is MSB = Bit 7, LSB = Bit 0 for Green, Red and Blue data.
2. 3-times transfer is used to transmit 2 pixel data to the 24-bit color depth information.
3. '-' = void

3.14.18. 18-bit Parallel MPU Interface

The DBI TYPE B 18-bit parallel bus interface of the ILI9806G can be used by setting the external pin IM [3:0] to 1101. The Figure 144 shows this system interface.

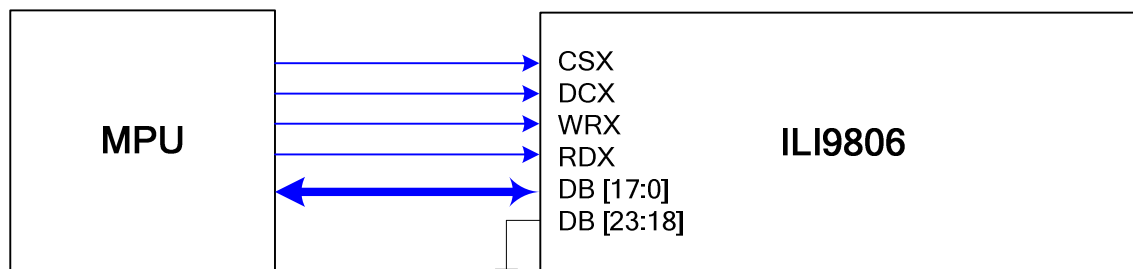


Figure 144: 18-bit Parallel MPU Interface

The display data formats available for this type of color depth are:

- 65K-Colors, RGB 5, 6, 5 bits input data (Set Standard Command 3Ah, DBI [2:0] = 101)
- 262K-Colors, RGB 6, 6, 6 bits input data (Set Standard Command 3Ah, DBI [2:0] = 110)
- 16.7M-Colors, RGB 8, 8, 8 bits input data (Set Standard Command 3Ah, DBI [2:0] = 111)

3.14.19. 18-bit Data Bus for 16-bit/pixel (RGB 5-6-5 bits input), 65K-color

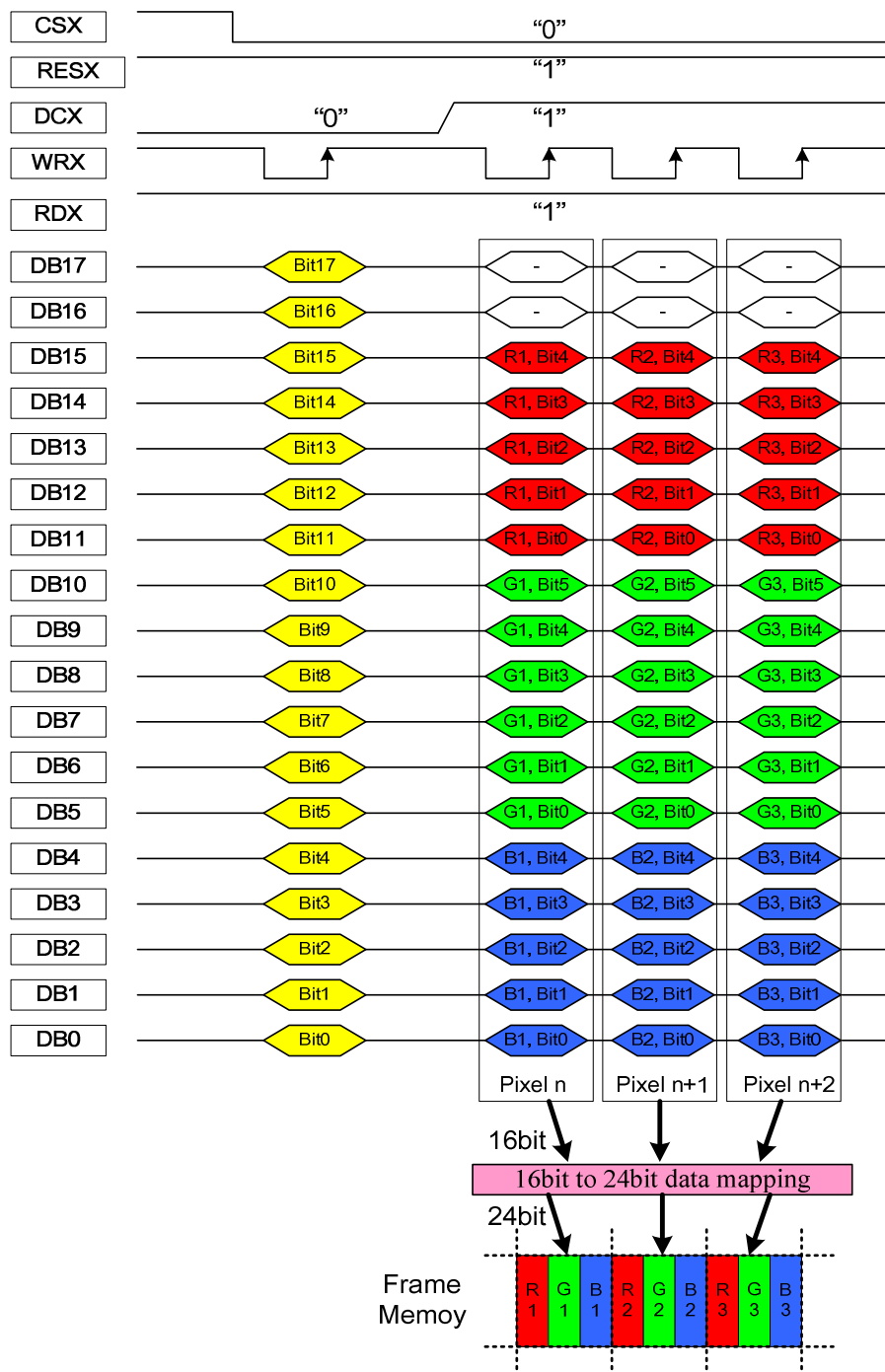


Figure 145: 18-bit Data Bus for 16-bit/pixel (RGB 5-6-5 bits input), 65K-color

Notes:

1. The data order is as follows: MSB = DB17, LSB = DB0, and picture data is MSB = Bit 5, LSB = Bit 0 for Green and MSB = Bit4, LSB = Bit0 for Red and Blue data.
2. 1-time transfer is used to transmit 1 pixel data to the 16-bit color depth information.
3. '-' = void

3.14.20. 18-bit Data Bus for 18-bit/pixel (RGB 6-6-6 bits input), 262K-color

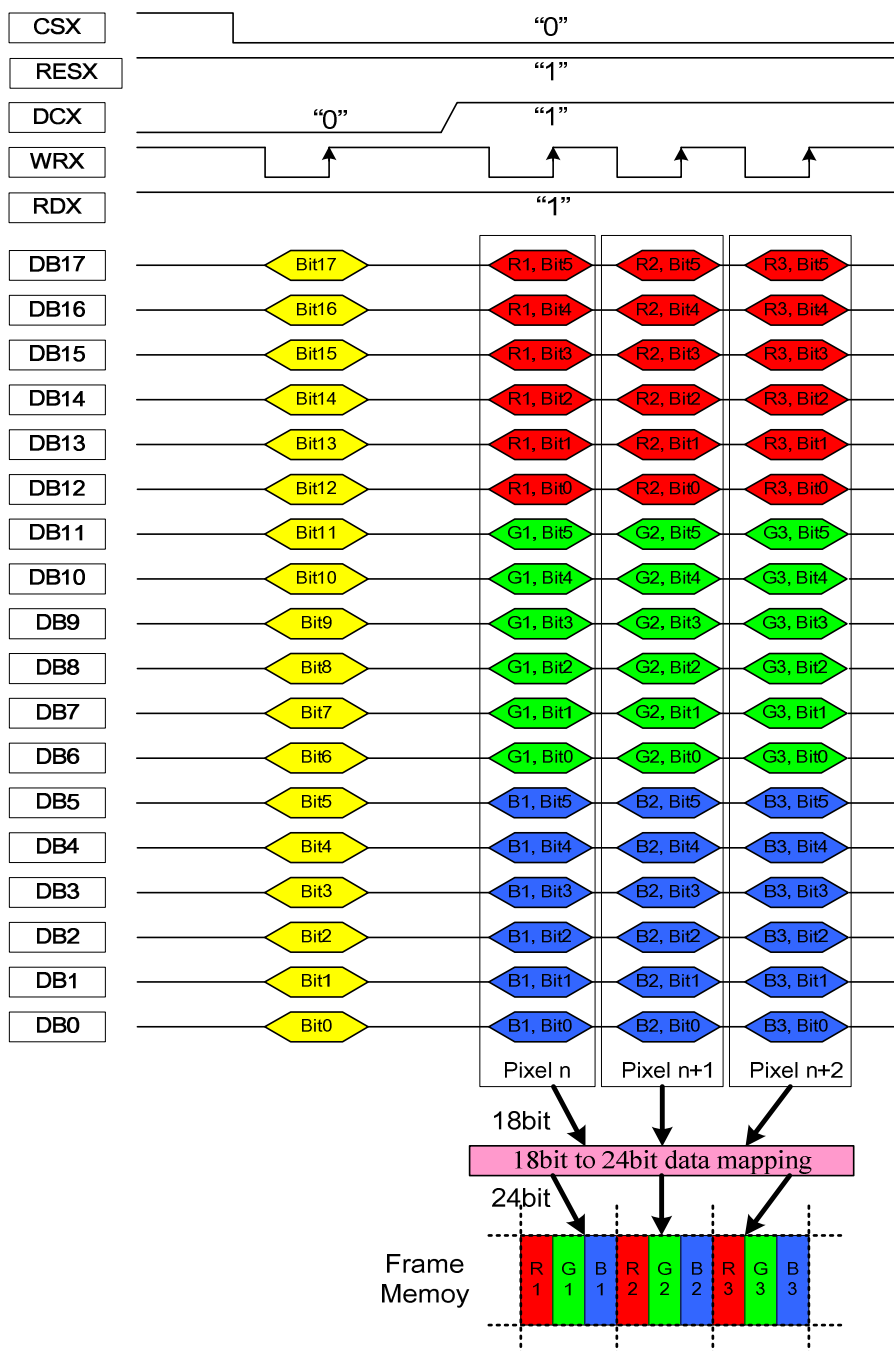


Figure 146: 18-bit Data Bus for 18-bit/pixel (RGB 6-6-6 bits input), 262K-color

Notes:

1. The data order is as follows: MSB = DB17, LSB = DB0, and picture data is MSB = Bit 5, LSB = Bit 0 for Green, Red and Blue data.
2. 1-time transfer is used to transmit 1 pixel data to the 18-bit color depth information.
3. '-' = void

3.14.21. 18-bit Data Bus for 24-bit/pixel (RGB 8-8-8 bits input), 16.7M-color

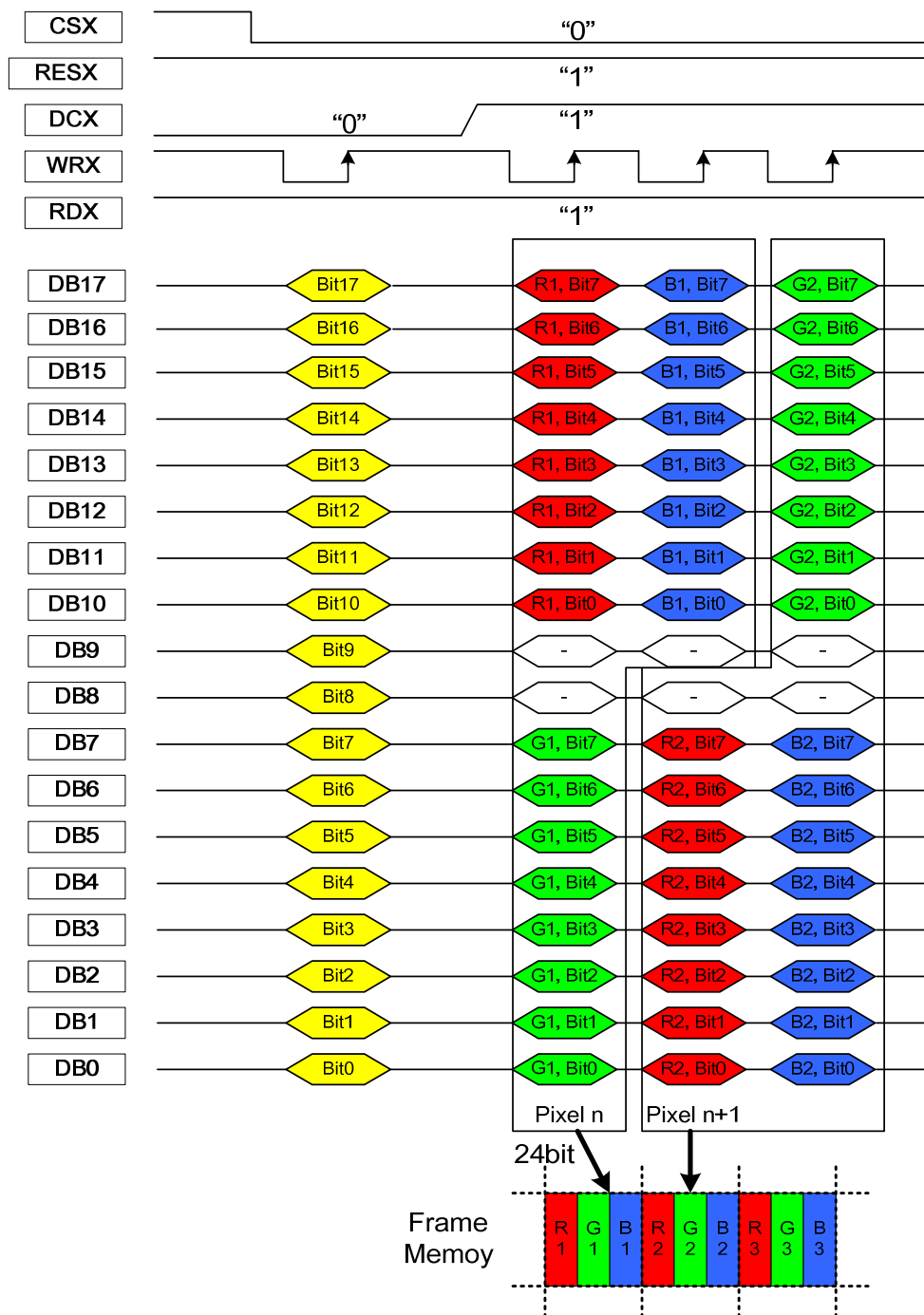


Figure 147: 18-bit Data Bus for 24-bit/pixel (RGB 8-8-8 bits input), 16.7M-color

Notes:

1. The data order is as follows: MSB = DB17, LSB = DB0, and picture data is MSB = Bit 7, LSB = Bit 0 for Green, Red and Blue data.
2. 2-times transfer is used to transmit 1 pixel data to the 24-bit color depth information.
3. '-' = void

3.14.22. 24-bit Parallel MPU Interface

The DBI TYPE B 24-bit parallel bus interface of the ILI9806G can be used by setting the external pin IM [3:0] to 0010. The Figure 148 shows this system interface.

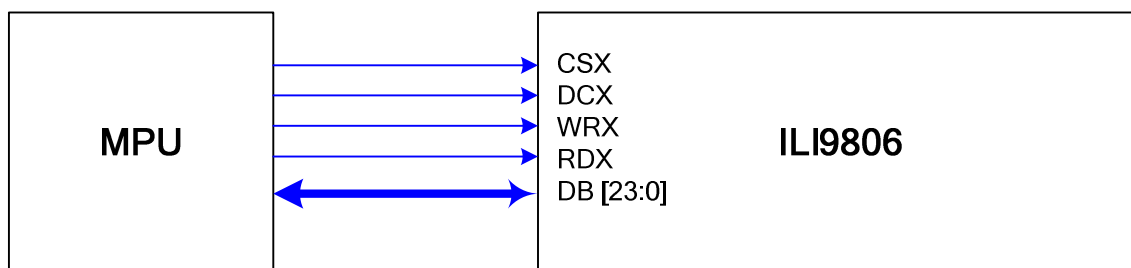


Figure 148: 24-bit Parallel MPU Interface

The display data format available for this type of color depth is:

- 16.7M-Colors, RGB 8, 8, 8 bits input data (Set Standard Command 3Ah, DBI [2:0] = 111)

3.14.23. 24-bit Data Bus for 24-bit/pixel (RGB 8-8-8 bits input), 16.7M-color

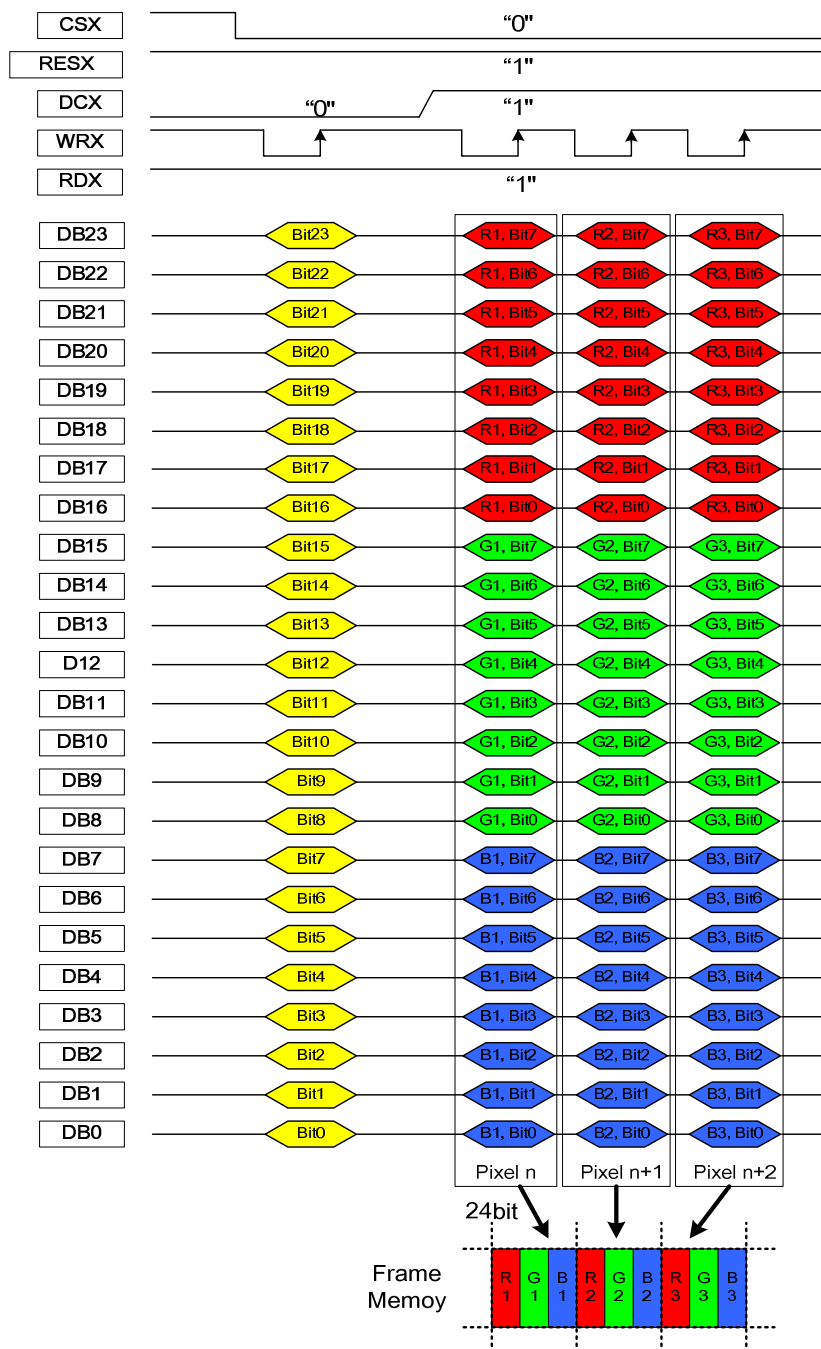


Figure 149: 24-bit Data Bus for 24-bit/pixel (RGB 8-8-8 bits input), 16.7M-color

Notes:

1. The data order is as follows: MSB = DB23, LSB = DB0 and picture data is MSB = Bit 7, LSB = Bit 0 for Green, Red and Blue data.
2. 1-time transfer is used to transmit 1 pixel data to the 24-bit color depth information.
3. '-' = void

3.14.24. DPI (RGB) Interface

3.14.25. 16-bit/pixel 65K colors order on the DPI Interface

The 16-bit RGB interface is selected by setting the DPI [2:0] bits to 101. The display operation is synchronized with VSYNC, HSYNC and DCK signals. Display data is transferred to the internal GRAM through the 16-bit RGB data bus in synchronization with the display operation.

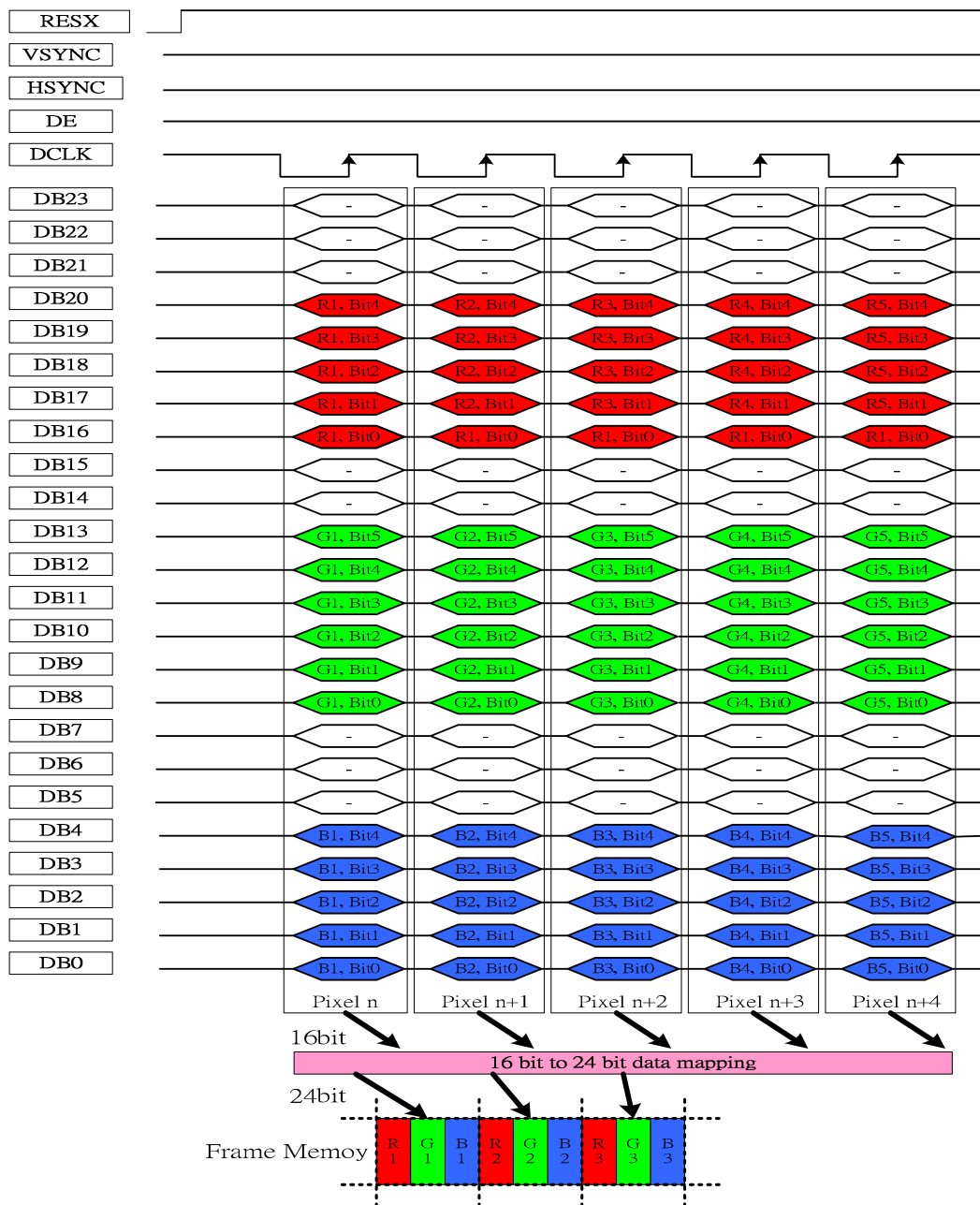


Figure 150: 16-bit/pixel 65K Colors Order on the DPI Interface

Notes:

1. The data order is as follows: MSB = DB23, LSB = DB0, and picture data is MSB = Bit 5, LSB = Bit 0 for Green, MSB = Bit 4, LSB = Bit 0 for Red and Blue data.
2. 1-time transfer is used to transmit 1 pixel data to the 16-bit color depth information.
3. '-' = void

3.14.26. 18-bit/pixel 262K Colors Order on the DPI Interface

The 18-bit RGB interface is selected by setting the DPI [2:0] bits to 110. The display operation is synchronized with VSYNC, HSYNC and DCK signals. Display data is transferred to the internal GRAM through the 18-bit RGB data bus in synchronization with the display operation

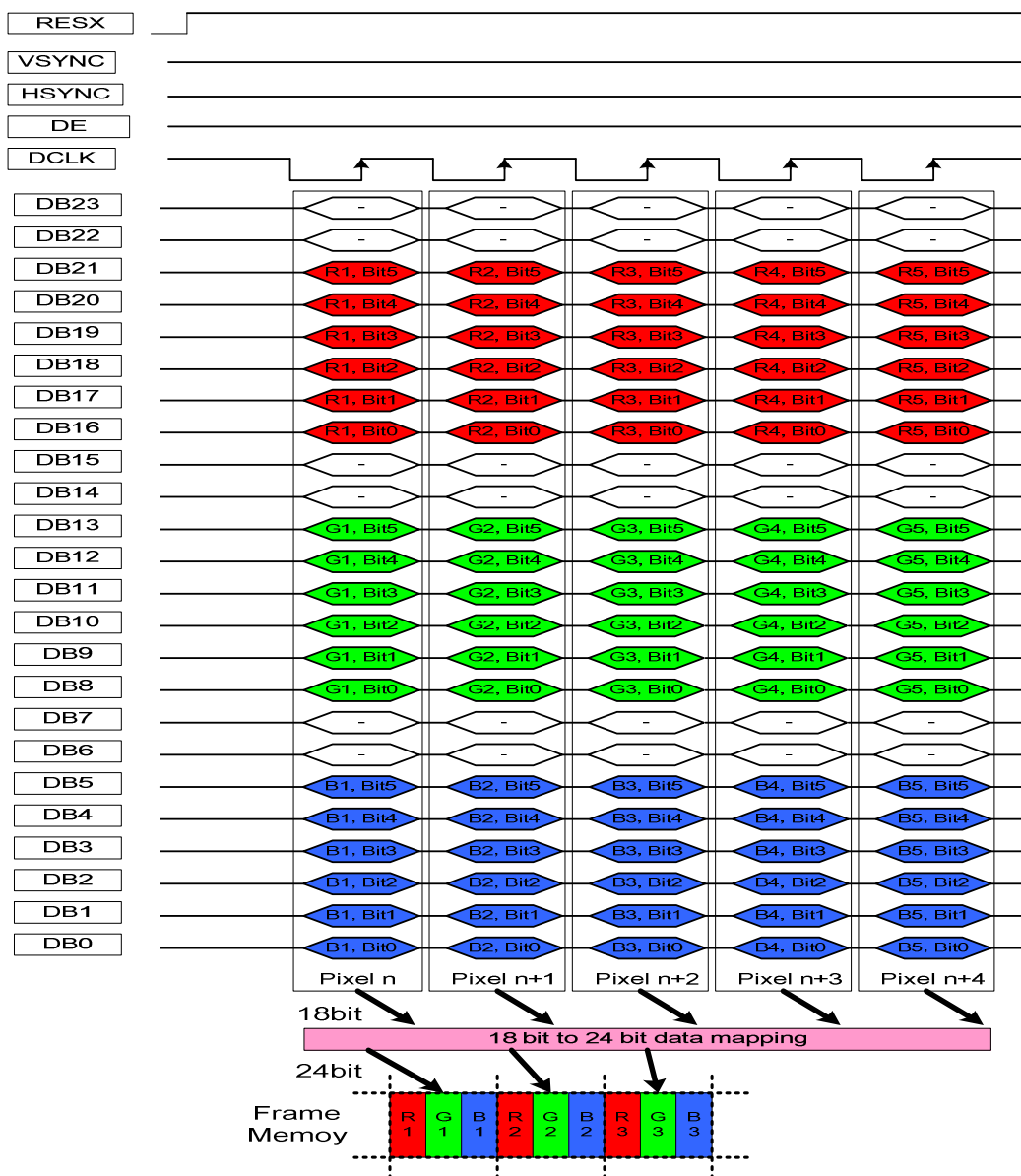


Figure 151: 18-bit/pixel 262K colors order on the DPI Interface

Notes:

1. The data order is as follows: MSB = DB23, LSB = DB0, and picture data is MSB = Bit 5, LSB = Bit 0 for Green, Red and Blue data.
2. 1-time transfer is used to transmit 1 pixel data to the 18-bit color depth information.
3. '-' = void

3.14.27. 24-bit/pixel 16.7M colors order on the DPI Interface

The 24-bit RGB interface is selected by setting the DPI [2:0] bits to 111. The display operation is synchronized with VSYNC, HSYNC and DCK signals. Display data is transferred to the internal GRAM through the 24-bit RGB data bus in synchronization with the display operation.

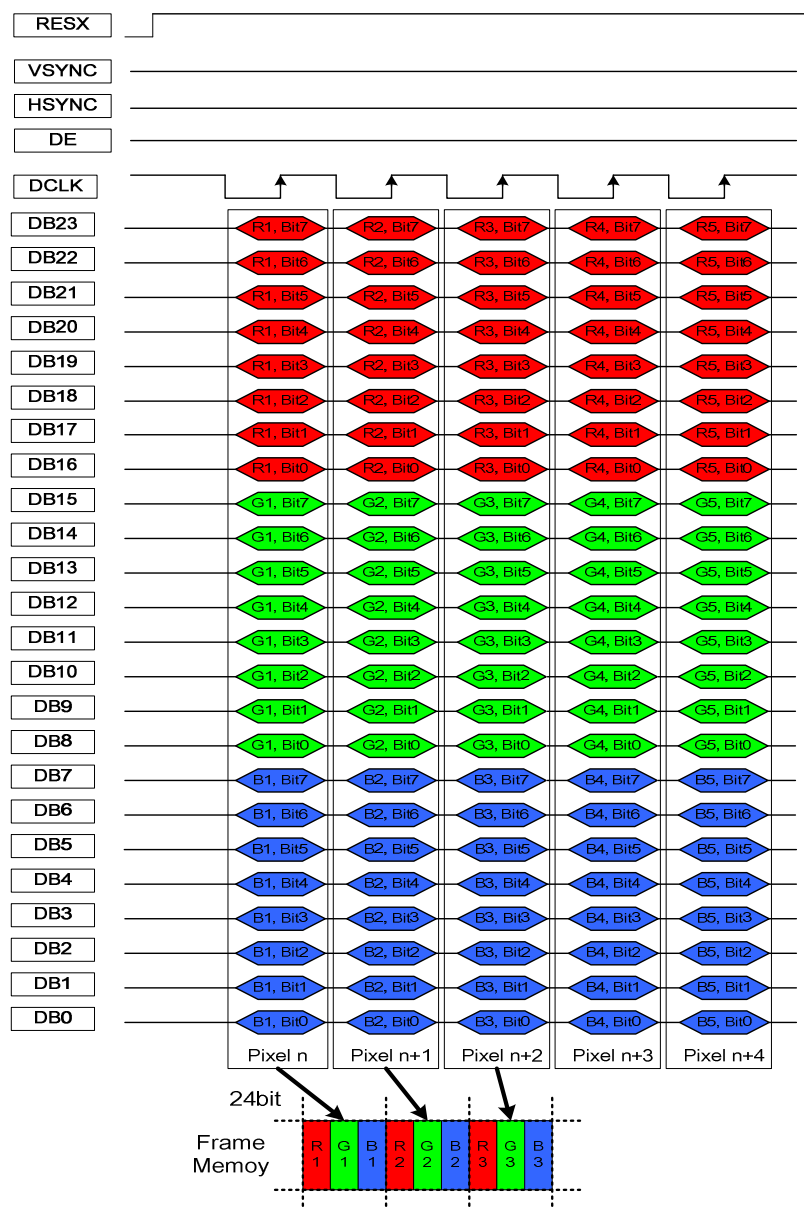


Figure 152: 24-bit/pixel 16.7M Colors Order on the DPI Interface

Notes:

1. The data order is as follows: MSB = DB23, LSB = DB0, and picture data is MSB = Bit 7, LSB = Bit 0 for Green, Red and Blue data.
2. 1-time transfer is used to transmit 1 pixel data to the 24-bit color depth information.

3.14.28. 16/18-bit Color Data Mapping to 24-bit Pixel Data Operation

Table 43 below lists settings for 24-bit data mapping. Set the EPF [1:0] bits of the register “Interface Setting (B8H)” that define three types of data formats for 24-bit data (pixel data r, g, b) mapping that pixel data is stored in the internal GRAM.

Table 43: 16/18-bit Color Data Mapping to 24-bit Pixel Data Operation

EPF [1:0]	Expand 16-bit color data (R,G,B) to 24-bit subpixel data (r, g, b)	Expand 18-bit color data (R,G,B) to 24-bit subpixel data (r, g, b)
00	“0” is written to the LSB. 8 bits subpixel, data r [7:0] = {16-bit color data R [4:0], 3'h0} 8 bits subpixel, data g [7:0] = {16-bit color data G [5:0], 2'h0} 8 bits subpixel, data b [7:0] = {16-bit color data B [4:0], 3'h0} (Note3): the data are converted as follows. 16-bit color data R [4:0] = 5'h1F, G [5:0] = 6'h3F, B [4:0] = 5'h1F → 24-bit pixel data r, g, b [7:0] = 24'hFFFFFF	“0” is written to the LSB. 8 bits subpixel, data r [7:0] = {18-bit color data R [5:0], 2'h0} 8 bits subpixel, data g [7:0] = {18-bit color data G [5:0], 2'h0} 8 bits subpixel, data b [7:0] = {18-bit color data B [5:0], 2'h0} (Note1): the data are converted as follows. 18-bit color data R [5:0] = 6'h3F, G [5:0] = 6'h3F, B [5:0] = 6'h3F → 24-bit pixel data r, g, b [7:0] = 24'hFFFFFF
01	“1” is written to the LSB. 8 bits subpixel, data r [7:0] = {16-bit color data R [4:0], 3'h7} 8 bits subpixel, data g [7:0] = {16-bit color data G [5:0], 2'h3} 8 bits subpixel, data b [7:0] = {16-bit color data B [4:0], 3'h7} (Note4): the data are converted as follows. 16-bit color data R [4:0] = 5'h0, G [5:0] = 6'h0, B [4:0] = 5'h0 → 24-bit pixel data r, g, b [7:0] = 24'h000000	“1” is written to the LSB. 8 bits subpixel, data r [7:0] = {18-bit color data R [5:0], 2'h3} 8 bits subpixel, data g [7:0] = {18-bit color data G [5:0], 2'h3} 8 bits subpixel, data b [7:0] = {18-bit color data B [5:0], 2'h3} (Note2): the data are converted as follows. 18-bit color data R [5:0] = 6'h0, G [5:0] = 6'h0, B [5:0] = 6'h0 → 24-bit pixel data r, g, b [7:0] = 24'h000000
10	The MSB value is written to the LSB. 8 bits subpixel, data r [7:0] = {16-bit color data R [4:0], R [4:2]} 8 bits subpixel, data g [7:0] = {16-bit color data G [5:0], G [5:4]} 8 bits subpixel, data b [7:0] = {16-bit color data B [4:0], B [4:2]}	The MSB value is written to the LSB. 8 bits subpixel, data r [7:0] = {18-bit color data R [5:0], R [5:4]} 8 bits subpixel, data g [7:0] = {18-bit color data G [5:0], G [5:4]} 8 bits subpixel, data b [7:0] = {18-bit color data B [5:0], B [5:4]}
11	Setting disabled	Setting disabled

	Frame memory data (24 bits)																							
	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
24-bit	R[7]	R[6]	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[7]	G[6]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[7]	B[6]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]
18-bit EPF[1:0]=00 (Note 1)	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	0	0	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	0	0	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]	0	0
18-bit EPF[1:0]=01 (Note 2)	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	1	1	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	1	1	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]	1	1
18-bit EPF[1:0]=10	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	R[5]	R[4]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	G[5]	G[4]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]	B[5]	B[4]
16-bit EPF[1:0]=00 (Note 3)	R[4]	R[3]	R[2]	R[1]	R[0]	0	0	0	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	0	0	B[4]	B[3]	B[2]	B[1]	B[0]	0	0	0
16-bit EPF[1:0]=01 (Note 4)	R[4]	R[3]	R[2]	R[1]	R[0]	1	1	1	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	1	1	B[4]	B[3]	B[2]	B[1]	B[0]	1	1	1
16-bit EPF[1:0]=10	R[4]	R[3]	R[2]	R[1]	R[0]	R[4]	R[3]	R[2]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	G[5]	G[4]	B[4]	B[3]	B[2]	B[1]	B[0]	B[4]	B[3]	B[2]

For example:

16-bit data mapping to 24-bit, EPF [1:0] = 10

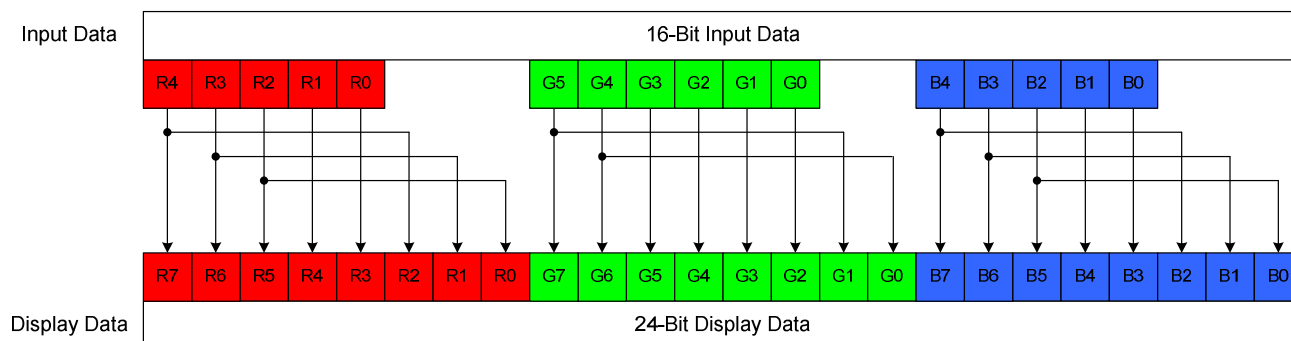


Figure 153: EPF [1:0] = 10, 16-bit data mapping to 24-bit

18-bit data mapping to 24-bit, EPF [1:0] = 10

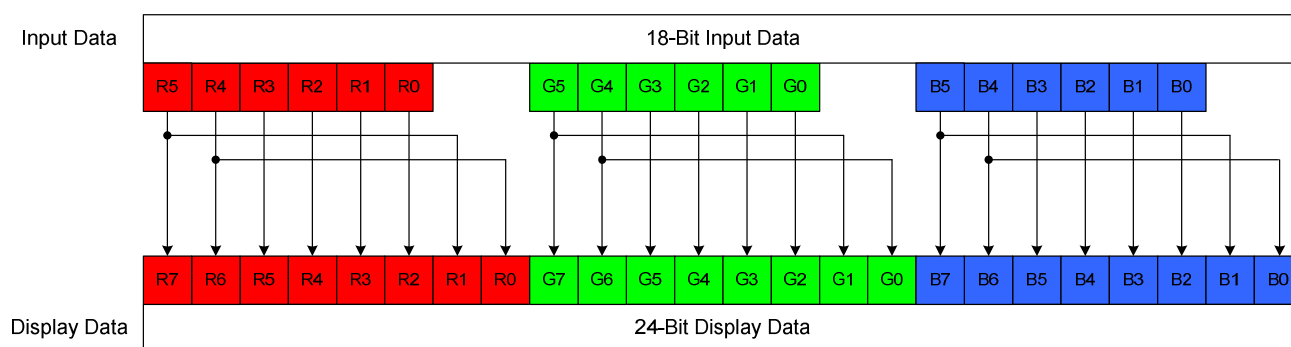


Figure 154: EPF [1:0] = 10, 18-bit data mapping to 24-bit

3.14.29. DSI Transmission Data Format

3.14.30. 16-bit per Pixel, Long Packet, Data Type 00 1110 (0Eh)

Packed Pixel Stream 16-Bit Format is a Long Packet used to transmit image data formatted as 16-bit pixels to a Video Mode display module. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte checksum. Pixel format is red (5 bits), green (6 bits), and blue (5 bits), in that order. Note that the Green component is split across two bytes. Within a color component, the LSB is sent first, the MSB last. With this format, pixel boundaries align with byte boundaries every two bytes. The total line width (displayed plus non-displayed pixels) should be a multiple of two bytes.

Normally, the ILI9806G has no frame buffer of its own, so all image data shall be supplied by the host processor at a sufficiently high rate to avoid flicker or other visible artifact.

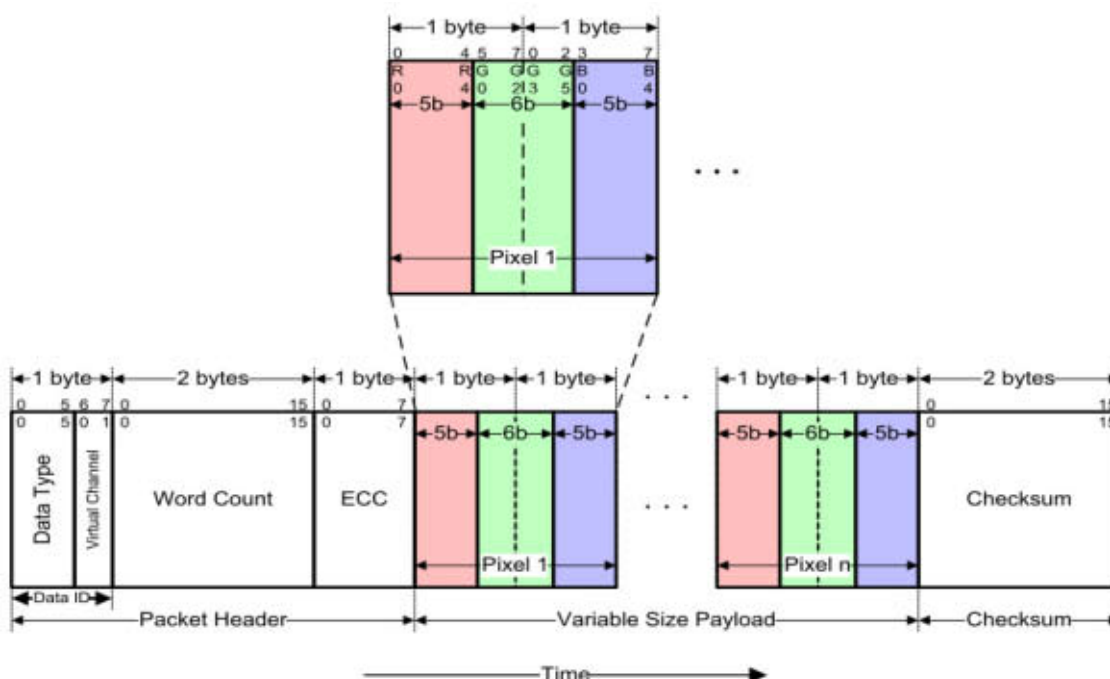


Figure 155: 16-bit per Pixel, Data Type 00 1110 (0Eh)

3.14.31. 18-bit per Pixel, Long Packet, Data Type = 01 1110 (1Eh)

Packed Pixel Stream 18-Bit Format (Packed) is a Long packet. It is used to transmit RGB image data formatted as pixels to a Video Mode display module that displays 18-bit pixels. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes, and a two-byte Checksum. Pixel format is red (6 bits), green (6 bits) and blue (6 bits), in that order. Within a color component, the LSB is sent first, the MSB last.

Note that pixel boundaries only align with byte boundaries every four pixels (nine bytes). Preferably, display modules employing this format have a horizontal extent (width in pixels) evenly divisible by four, so no partial bytes remain at the end of the display line data. If the active (displayed) horizontal width is not a multiple of four pixels, the transmitter shall send additional filled pixels at the end of the display line to make the transmitted width a multiple of four pixels. The receiving peripheral shall not display the filled pixels when refreshing the display device. For example, if a display device has an active display width of 399 pixels, the transmitter should send 400 pixels in one or more packets. The receiver should display the first 399 pixels and discard the last pixel of the transmission. With this format, the total line width (displayed and non-displayed pixels) should be a multiple of four 1246 pixels (nine bytes).

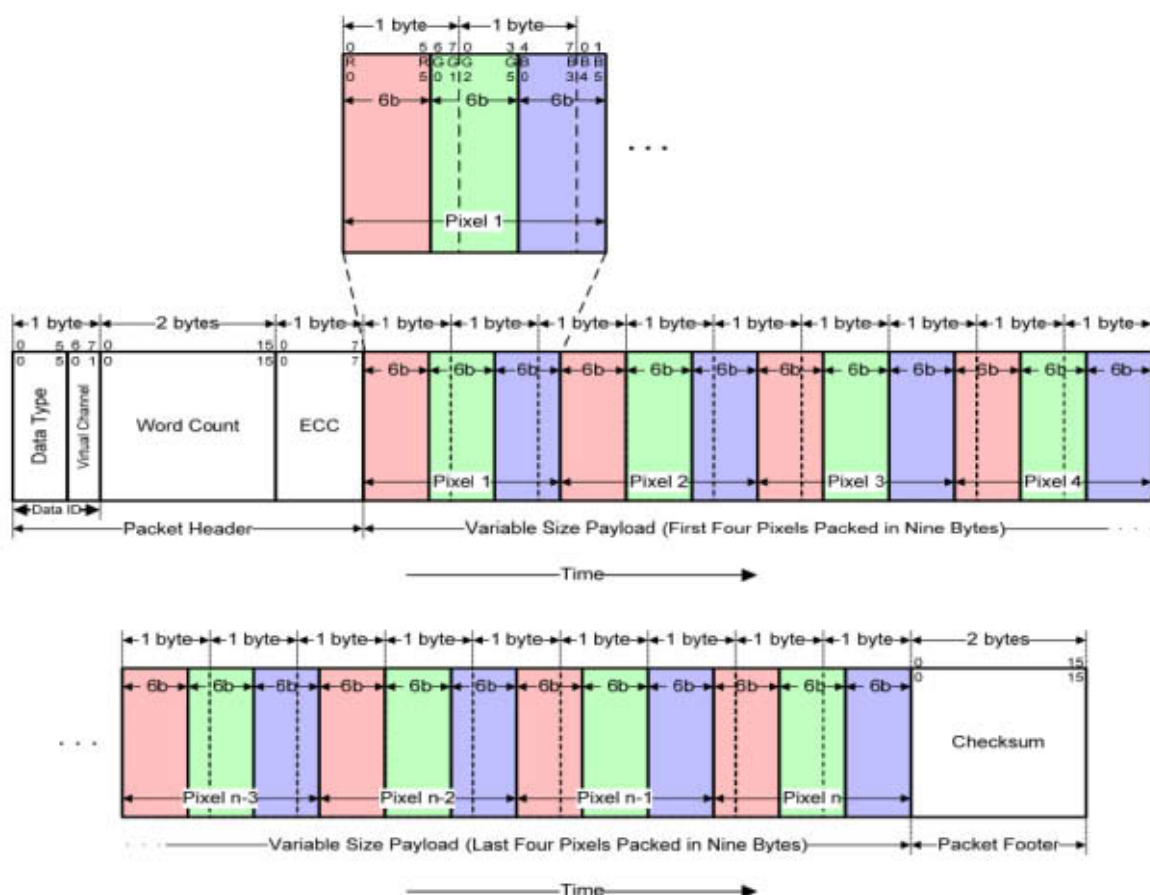


Figure 156: 18-bit per Pixel, Data Type = 01 1110 (1Eh)

3.14.32. 18-bit per Pixel, Long Packet, Data Type = 10 1110 (2Eh)

In the 18-bit Pixel Loosely Packed format, each R, G, or B color component is six bits but is shifted to the upper bits of the byte, such that the valid pixel bits occupy bits [7:2] of each byte. Bits [1:0] of each payload byte representing active pixels are ignored. As a result, each pixel requires three bytes as it is transmitted across the link. This requires more bandwidth than the “packed” format, but requires less shifting and multiplexing logic in the packing and unpacking functions on each end of the Link.

This format is used to transmit RGB image data formatted as pixels to a Video Mode display module that displays 18-bit pixels. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte Checksum. The pixel format is red (6 bits), green (6 bits) and blue (6 bits) in that order. Within a color component, the LSB is sent first, the MSB last.

With this format, pixel boundaries align with byte boundaries every three bytes. The total line width (displayed and non-displayed pixels) should be a multiple of three bytes.

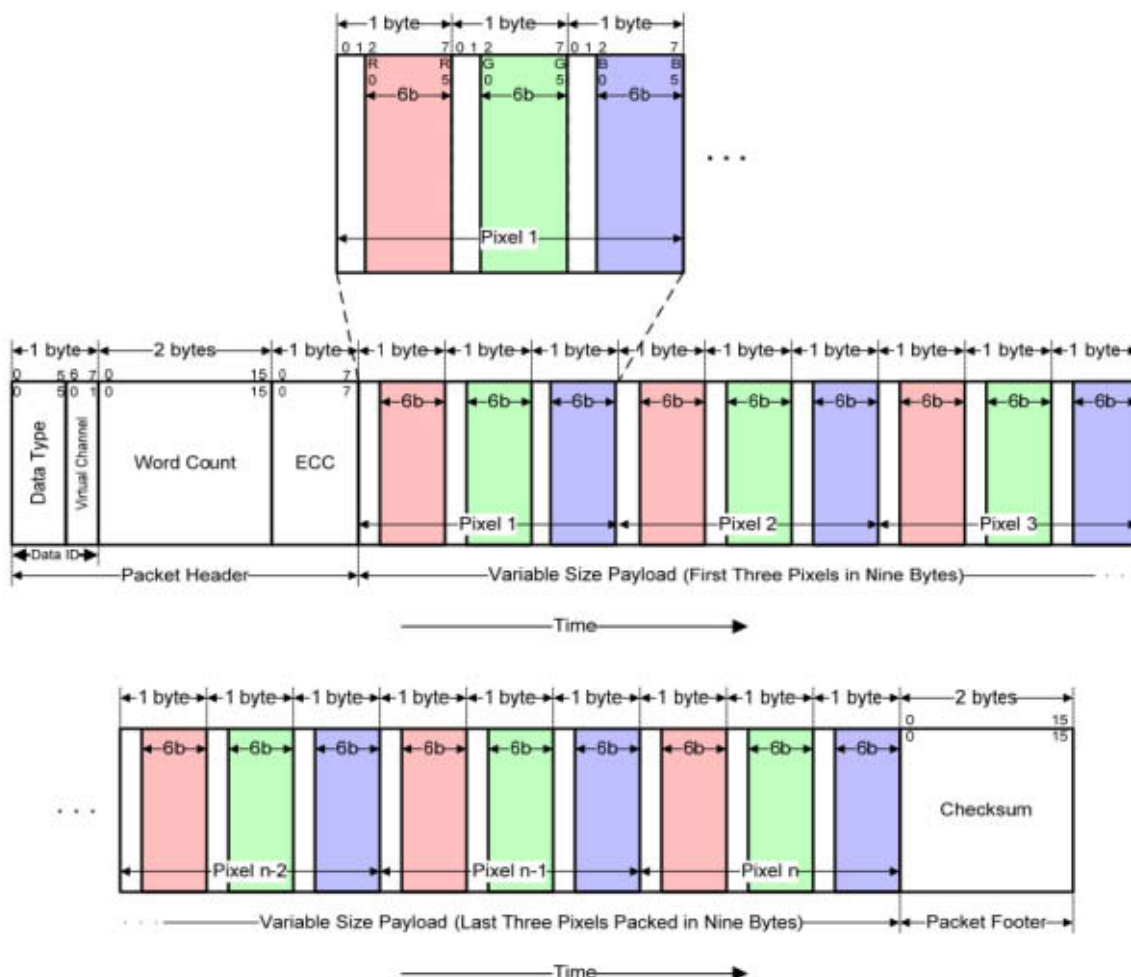


Figure 157: 18-bit per Pixel, Data Type = 10 1110 (2Eh)

3.14.33. 24-bit per Pixel, Long Packet, Data Type = 11 1110 (3Eh)

Packed Pixel Stream 24-Bit Format is a Long packet. It is used to transmit image data formatted as 24-bit pixels to a Video Mode display module. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte Checksum. The pixel format is red (8 bits), green (8 bits) and blue (8 bits), in that order. Each color component occupies one byte in the pixel stream; no components are split across byte boundaries. Within a color component, the LSB is sent first, the MSB last.

With this format, pixel boundaries align with byte boundaries every three bytes. The total line width (displayed and non-displayed pixels) should be a multiple of three bytes.

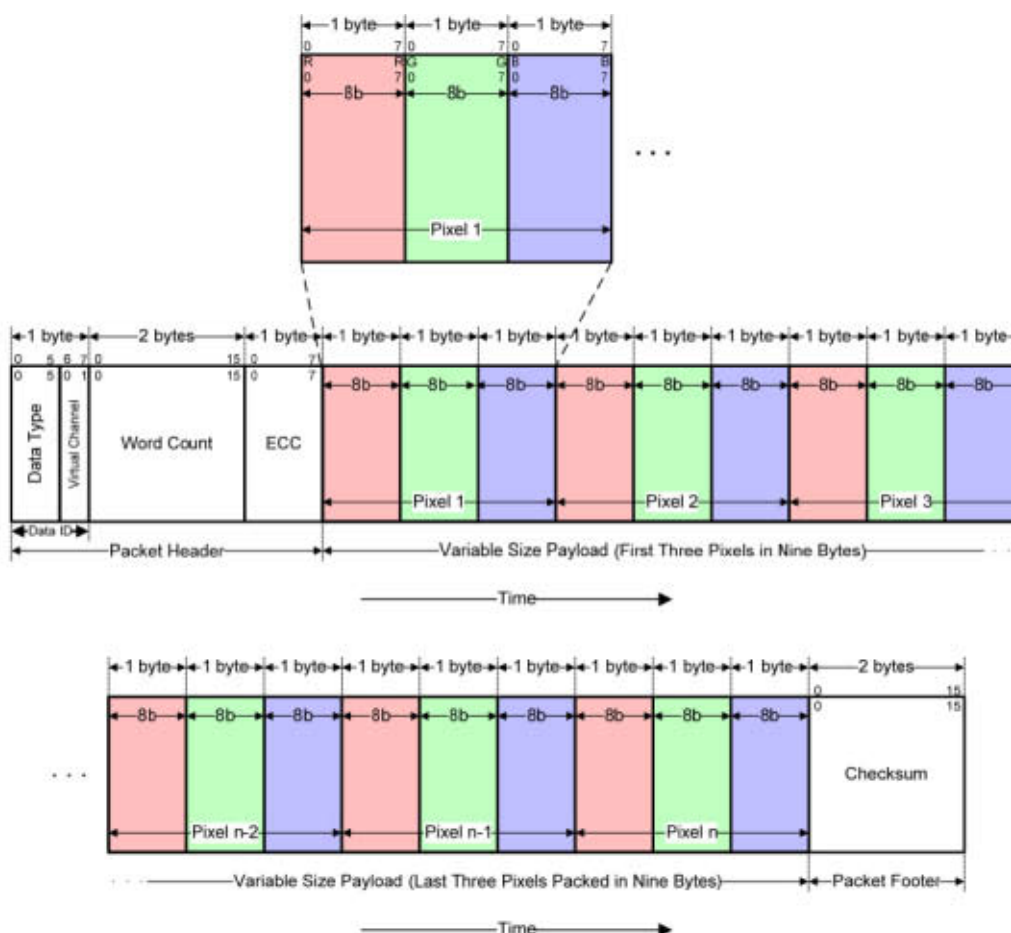


Figure 158: 24-bit per Pixel, Data Type = 11 1110 (3Eh)

4. Command

4.1. Command List

4.1.1. Standard Command List

Command Function	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
NOP	0	1	↑	xx	0	0	0	0	0	0	0	0	00h

Command Function	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Software Reset	0	1	↑	xx	0	0	0	0	0	0	0	1	01h

Command Function	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Read Display Identification Information	0	1	↑	xx	0	0	0	0	0	1	0	0	04h
	1	↑	1	xx	x	x	x	x	x	x	x	x	xx
	1	↑	1	xx	ID1 [7:0]								xx
	1	↑	1	xx	ID2 [7:0]								xx
	1	↑	1	xx	ID3 [7:0]								xx

Command Function	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Read Number of the Errors on DSI	0	1	↑	xx	0	0	0	0	0	1	0	1	05h
	1	↑	1	xx	x	x	x	x	x	x	x	x	xx
	1	↑	1	xx	P [7:0]								xx

Command Function	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Read Red color	0	1	↑	xx	0	0	0	0	0	1	1	0	06h
	1	↑	1	xx	x	x	x	x	x	x	x	x	xx
	1	↑	1	xx	R [7:0]								xx

Command Function	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Read Green color	0	1	↑	xx	0	0	0	0	0	1	1	1	07h
	1	↑	1	xx	x	x	x	x	x	x	x	x	xx
	1	↑	1	xx	G [7:0]								xx

Command Function	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Read Blue color	0	1	↑	xx	0	0	0	0	1	0	0	0	08h
	1	↑	1	xx	x	x	x	x	x	x	x	x	xx
	1	↑	1	xx	B [7:0]								xx

Command Function	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Read Display Status	0	1	↑	xx	0	0	0	0	1	0	0	1	09h
	1	↑	1	xx	x	x	x	x	x	x	x	x	xx
	1	↑	1	xx	D [31:24]								xx
	1	↑	1	xx	D [23:16]								xx
	1	↑	1	xx	D [15:8]								xx
	1	↑	1	xx	D [7:0]								xx

Command Function	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Read Power Mode	0	1	↑	xx	0	0	0	0	1	0	1	0	0Ah
	1	↑	1	xx	x	x	x	x	x	x	x	x	xx
	1	↑	1	xx	D [7:2]							0	0

Command Function	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Read Address Mode	0	1	↑	xx	0	0	0	0	1	0	1	1	0Bh
	1	↑	1	xx	x	x	x	x	x	x	x	x	xx
	1	↑	1	xx	D [7:0]								xx

Command Function	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Read Pixel Format	0	1	↑	xx	0	0	0	0	1	1	0	0	0Ch
	1	↑	1	xx	x	x	x	x	x	x	x	x	xx
	1	↑	1	xx	0	DPI [2:0]			0	DBI [2:0]			xx

Command Function	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Read Display Mode	0	1	↑	xx	0	0	0	0	1	1	0	1	0Dh
	1	↑	1	xx	x	x	x	x	x	x	x	x	xx
	1	↑	1	xx	D [7:0]								xx

Command Function	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Read Display signal Mode	0	1	↑	xx	0	0	0	0	1	1	1	0	0Eh
	1	↑	1	xx	x	x	x	x	x	x	x	x	xx
	1	↑	1	xx	D7	D6	D5	D4	D3	D2	D1	D0	xx

Command Function	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Read Display Self-Diagnostic Result	0	1	↑	xx	0	0	0	0	1	1	1	1	0Fh
	1	↑	1	xx	x	x	x	x	x	x	x	x	xx
	1	↑	1	xx	D [7:0]								xx

Command Function	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Sleep In	0	1	↑	xx	0	0	0	1	0	0	0	0	10h

Command Function	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Sleep Out	0	1	↑	xx	0	0	0	1	0	0	0	1	11h

Command Function	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Partial Mode On	0	1	↑	xx	0	0	0	1	0	0	1	0	12h

Command Function	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Normal Display Mode On	0	1	↑	xx	0	0	0	1	0	0	1	1	13h

Command Function	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Display Inversion Off	0	1	↑	xx	0	0	1	0	0	0	0	0	20h

Command Function	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Display Inversion ON	0	1	↑	xx	0	0	1	0	0	0	0	1	21h

Command Function	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
All Pixel Off	0	1	↑	xx	0	0	1	0	0	0	1	0	22h

Command Function	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
All Pixel On	0	1	↑	xx	0	0	1	0	0	0	1	1	23h

Command Function	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Gamma Curve Set	0	1	↑	xx	0	0	1	0	0	1	1	0	26h
	1	1	↑	xx	GC7	GC6	GC5	GC4	GC3	GC2	GC1	GC0	xx

Command Function	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Display Off	0	1	↑	xx	0	0	1	0	1	0	0	0	28h

Command Function	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Display ON	0	1	↑	xx	0	0	1	0	1	0	0	1	29h

Command Function	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Set Column Address	0	1	↑	xx	0	0	1	0	1	0	1	0	2Ah
	1	1	↑	xx	SC [15:8]								xx
	1	1	↑	xx	SC [7:0]								xx
	1	1	↑	xx	EC [15:8]								xx
	1	1	↑	xx	EC [7:0]								xx

Command Function	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Set Page Address	0	1	↑	xx	0	0	1	0	1	0	1	1	2Bh
	1	1	↑	xx	SP [15:8]							xx	
	1	1	↑	xx	SP [7:0]							xx	
	1	1	↑	xx	EP [15:8]							xx	
	1	1	↑	xx	EP [7:0]							xx	

Command Function	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Write Memory Start	0	1	↑	xx	0	0	1	0	1	1	0	0	2Ch
	1	1	↑	Image Data 1 [D23:D0]									xx
	1	1	↑	Image Data x [D23:D0]									xx
	1	1	↑	Image Data n [D23:D0]									xx

Command Function	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Memory Read	0	1	↑	xx	0	0	1	0	1	1	1	0	2Eh
	1	↑	1	xx	x	x	x	x	x	x	x	x	xx
	1	↑	1	Image Data 1 [D23:D0]									xx
	1	↑	1	Image Data x [D23:D0]									xx
	1	↑	1	Image Data n [D23:D0]									xx

Command Function	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Partial Area	0	1	↑	xx	0	0	1	1	0	0	0	0	30h
	1	1	↑	xx	SR [15:8]								xx
	1	1	↑	xx	SR [7:0]								xx
	1	1	↑	xx	ER [15:8]								xx
	1	1	↑	xx	ER [7:0]								xx

Command Function	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Vertical Scrolling Definition	0	1	↑	xx	0	0	1	1	0	0	1	1	33h
	1	1	↑	xx	TFA [15:8]								xx
	1	1	↑	xx	TFA [7:0]								xx
	1	1	↑	xx	VSA [15:8]								xx
	1	1	↑	xx	VSA [7:0]								xx
	1	1	↑	xx	BFA [15:8]								xx
	1	1	↑	xx	BFA [7:0]								xx

Command Function	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Tearing Effect Line OFF	0	1	↑	xx	0	0	1	1	0	1	0	0	34h

Command Function	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Tearing Effect Line ON	0	1	↑	xx	0	0	1	1	0	1	0	1	35h
	1	1	↑	xx	0	0	0	0	0	0	0	M	xx

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Command Function	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Memory Access Control	0	1	↑	xx	0	0	1	1	0	1	1	0	36h
	1	1	↑	xx	MY	MX	MV	ML	BGR	MH	SS	GS	xx

Command Function	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Vertical Scrolling Start Address	0	1	↑	xx	0	0	1	1	0	1	1	1	37h
	1	1	↑	xx	VSP [15:8]								xx
	1	1	↑	xx	VSP [7:0]								xx

Command Function	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Idle Mode Off	0	1	↑	xx	0	0	1	1	1	0	0	0	38h

Command Function	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Idle Mode On	0	1	↑	xx	0	0	1	1	1	0	0	1	39h

Command Function	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Interface Pixel Format	0	1	↑	xx	0	0	1	1	1	0	1	0	3Ah
	1	1	↑	xx	0	DPI [2:0]			0	DBI [2:0]			xx

Command Function	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Memory Write Continue	0	1	↑	xx	0	0	1	1	1	1	0	0	3Ch
	1	1	↑	Image Data 1 [D23:D0]									xx
	1	1	↑	Image Data x [D23:D0]									xx
	1	1	↑	Image Data n [D23:D0]									xx

Command Function	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Memory Read Continue	0	1	↑	xx	0	0	1	1	1	1	1	0	3Eh
	1	↑	1	xx	x	x	x	x	x	x	x	x	xx
	1	↑	1	Image Data 1 [D23:D0]									xx
	1	↑	1	Image Data x [D23:D0]									xx
	1	↑	1	Image Data n [D23:D0]									xx

Command Function	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Write Tear Scan line	0	1	↑	xx	0	1	0	0	0	1	0	0	44h
	1	1	↑	xx	N [15:8]								xx
	1	1	↑	xx	N [7:0]								xx

Command Function	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Read Tear Line	0	1	↑	xx	0	1	0	0	0	1	0	1	45h
	1	↑	1	xx	x	x	x	x	x	x	x	x	xx
	1	↑	1	xx	N [15:8]								xx
	1	↑	1	xx	N [7:0]								xx

Command Function	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Write Display Brightness	0	1	↑	xx	0	1	0	1	0	0	0	1	51h
	1	1	↑	xx	DBV [7:0]								xx

Command Function	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Read Display Brightness Value	0	1	↑	xx	0	1	0	1	0	0	1	0	52h
	1	↑	1	xx	x	x	x	x	x	x	x	x	xx
	1	↑	1	xx	DBV [7:0]								xx

Command Function	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Write CTRL Display	0	1	↑	xx	0	1	0	1	0	0	1	1	53h
	1	1	↑	xx	0	0	BCTRL	0	DD	BL	0	0	xx

Command Function	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Read CTRL Display	0	1	↑	xx	0	1	0	1	0	1	0	0	54h
	1	↑	1	xx	x	x	x	x	x	x	x	x	xx
	1	↑	1	xx	0	0	BCTRL	0	DD	BL	0	0	xx

Command Function	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Write Content Adaptive Brightness Control	0	1	↑	xx	0	1	0	1	0	1	0	1	55h
	1	1	↑	xx	C [7:4]				C [3:0]				xx

Command Function	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Read Content Adaptive Brightness Control	0	1	↑	xx	0	1	0	1	0	1	1	0	56h
	1	↑	1	xx	x	x	x	x	x	x	x	x	xx
	1	↑	1	xx	C [7:4]				C [3:0]				xx

Command Function	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Write CABC Minimum Brightness	0	1	↑	xx	0	1	0	1	1	1	1	0	5Eh
	1	1	↑	xx	CMB [7:0]								xx

Command Function	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Read CABC Minimum Brightness	0	1	↑	xx	0	1	0	1	1	1	1	1	5Fh
	1	↑	1	xx	x	x	x	x	x	x	x	x	xx
	1	↑	1	xx	CMB [7:0]								xx

Command Function	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Read Automatic Brightness Control Self-Diagnostic Result	0	1	↑	xx	0	1	1	0	1	0	0	0	68h
	1	↑	1	xx	x	x	x	x	x	x	x	x	xx
	1	↑	1	xx	D [7:6]			0	0	0	0	0	xx

Command Function	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Read Black/White Low Bits	0	1	↑	xx	0	1	1	1	0	0	0	0	70h
	1	↑	1	xx	x	x	x	x	x	x	x	x	xx
	1	↑	1	xx	BKx [1:0]		BKy [1:0]		Wx [1:0]		Wy [1:0]		xx

Command Function	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Read Bkx	0	1	↑	xx	0	1	1	1	0	0	0	1	71h
	1	↑	1	xx	x	x	x	x	x	x	x	x	xx
	1	↑	1	xx	BKx [9:2]								xx

Command Function	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Read Bky	0	1	↑	xx	0	1	1	1	0	0	1	0	72h
	1	↑	1	xx	x	x	x	x	x	x	x	x	xx
	1	↑	1	xx	BKv [9:2]								xx

Command Function	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Read Wx	0	1	↑	xx	0	1	1	1	0	0	1	1	73h
	1	↑	1	xx	x	x	x	x	x	x	x	x	xx
	1	↑	1	xx	Wx [9:2]								xx

Command Function	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Read Wy	0	1	↑	xx	0	1	1	1	0	1	0	0	74h
	1	↑	1	xx	x	x	x	x	x	x	x	x	xx
	1	↑	1	xx	Wy [9:2]								xx

Command Function	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Read Red/Green Low bits	0	1	↑	xx	0	1	1	1	0	1	0	1	75h
	1	↑	1	xx	x	x	x	x	x	x	x	x	xx
	1	↑	1	xx	Rx [1:0]		Ry [1:0]		Gx [1:0]		Gy [1:0]		xx

Command Function	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Read Rx	0	1	↑	xx	0	1	1	1	0	1	1	0	76h
	1	↑	1	xx	x	x	x	x	x	x	x	x	xx
	1	↑	1	xx	Rx [9:2]								xx

Command Function	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Read Ry	0	1	↑	xx	0	1	1	1	0	1	1	1	77h
	1	↑	1	xx	x	x	x	x	x	x	x	x	xx
	1	↑	1	xx	Ry [9:2]								xx

Command Function	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Read Gx	0	1	↑	xx	0	1	1	1	1	0	0	0	78h
	1	↑	1	xx	x	x	x	x	x	x	x	x	xx
	1	↑	1	xx	Gx [9:2]								xx

Command Function	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Read Gy	0	1	↑	xx	0	1	1	1	1	0	0	1	79h
	1	↑	1	xx	x	x	x	x	x	x	x	x	xx
	1	↑	1	xx	Gy [9:2]								xx

Command Function	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Blue/AColour Low Bits	0	1	↑	xx	0	1	1	1	1	0	1	0	7Ah
	1	↑	1	xx	x	x	x	x	x	x	x	x	xx
	1	↑	1	xx	Bx [1:0]		By [1:0]		Ax [1:0]		Ay [1:0]		xx

Command Function	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Read Bx	0	1	↑	xx	0	1	1	1	1	0	1	1	7Bh
	1	↑	1	xx	x	x	x	x	x	x	x	x	xx
	1	↑	1	xx	Bx [9:2]								xx

Command Function	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Read By	0	1	↑	xx	0	1	1	1	1	1	0	0	7Ch
	1	↑	1	xx	x	x	x	x	x	x	x	x	xx
	1	↑	1	xx	By [9:2]								xx

Command Function	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Read Ax	0	1	↑	xx	0	1	1	1	1	1	0	1	7Dh
	1	↑	1	xx	x	x	x	x	x	x	x	x	xx
	1	↑	1	xx	Ax [9:2]								xx

Command Function	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Read Ay	0	1	↑	xx	0	1	1	1	1	1	1	0	7Eh
	1	↑	1	xx	x	x	x	x	x	x	x	x	xx
	1	↑	1	xx	Ay [9:2]								xx

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Command Function	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Read DDB Start	0	1	↑	xx	1	0	1	0	0	0	0	1	A1h
	1	↑	1	xx	x	x	x	x	x	x	x	x	xx
	1	↑	1	xx	SID [7:0]								xx
	1	↑	1	xx	SID [15:8]								xx
	1	↑	1	xx	MRID [7:0]								xx
	1	↑	1	xx	MRID [15:8]								xx
	1	↑	1	xx	1	1	1	1	1	1	1	1	FFh

Command Function	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Read DDB Continue	0	1	↑	xx	1	0	1	0	1	0	0	0	A8h
	1	↑	1	xx	x	x	x	x	x	x	x	x	xx
	1	↑	1	xx	D1 [7:0]								xx
	1	↑	1	xx	Dx [7:0]								xx
	1	↑	1	xx	Dn [7:0]								xx

Command Function	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Read First Checksum	0	1	↑	xx	1	0	1	0	1	0	1	0	AAh
	1	↑	1	xx	FCS [7:0]								xx

Command Function	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Read Continue Checksum	0	1	↑	xx	1	0	1	0	1	1	1	1	AFh
	1	↑	1	xx	CCS [7:0]								xx

Command Function	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Read Device Code	0	1	↑	xx	1	1	0	1	1	0	1	0	D3h
	1	↑	1	xx	x	x	x	x	x	x	x	x	xx
	1	↑	1	xx	0	0	0	0	0	0	0	0	00h
	1	↑	1	xx	1	0	0	1	1	0	0	0	98h
	1	↑	1	xx	0	0	0	0	0	1	1	0	06h

Command Function	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Read ID1	0	1	↑	xx	1	1	0	1	1	0	1	0	DAh
	1	↑	1	xx	x	x	x	x	x	x	x	x	xx
	1	↑	1	xx	ID1 [7:0]								xx

Command Function	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Read ID2	0	1	↑	xx	1	1	0	1	1	0	1	1	DBh
	1	↑	1	xx	x	x	x	x	x	x	x	x	xx
	1	↑	1	xx	ID2 [7:0]								xx

Command Function	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Read ID3	0	1	↑	xx	1	1	0	1	1	1	0	0	DCh
	1	↑	1	xx	x	x	x	x	x	x	x	x	xx
	1	↑	1	xx	ID3 [7:0]								xx

4.1.2. Extended Command List

Extended Command Set												
Command Function	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Interface Mode Control	0	1	↑	1	0	1	1	0	0	0	0	B0h
	1	1	↑	0	0	0	0	VSPL	HSPL	DPL	EPL	XX

Command Function	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Frame Rate Control 1	0	1	↑	1	0	1	1	0	0	0	1	B1h
	1	1	↑	0	0	0	0	0	0	DIVA [1:0]		XX
	1	1	↑	0	0	0	RTNA [4:0]					XX
	1	1	↑	0	0	FRSA [5:0]						XX

Command Function	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Frame Rate Control 2	0	1	↑	1	0	1	1	0	0	1	0	B2h
	1	1	↑	0	0	0	0	0	0	DIVB [1:0]		XX
	1	1	↑	0	0	0	RTNB [4:0]					XX
	1	1	↑	0	0	FRSB [5:0]					XX	

Command Function	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Frame Rate Control 3	0	1	↑	1	0	1	1	0	0	1	1	B3h
	1	1	↑	0	0	0	0	0	0	DIVC[1:0]		XX
	1	1	↑	0	0	0	RTNC [4:0]					XX
	1	1	↑	0	0	FRSC [5:0]					XX	

Command Function	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Display Inversion Control	0	1	↑	1	0	1	1	0	1	0	0	B4h
	1	1	↑	0	0	0	0	NLA [3:0]				XX
	1	1	↑	0	0	0	0	NLB [3:0]				XX
	1	1	↑	0	0	0	0	NLC [3:0]				XX

Command Function	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Blanking Porch Control	0	1	↑	1	0	1	1	0	1	0	1	B5h
	1	1	↑	0	VFP [6:0]							XX
	1	1	↑	0	VBP [6:0]							XX
	1	1	↑	HBP [7:0]								XX
	1	1	↑	0	0	0	0	0	0	HBP [9:8]		XX

Command Function	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Display Function Control	0	1	↑	1	0	1	1	0	1	1	0	B6h
	1	1	↑	SYNC mode	0	RM	0	0	0	1	PT	XX

Command Function	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Entry Mode Set	0	1	↑	1	0	1	1	0	1	1	1	B7h
	1	1	↑	0	0	0	0	DSTB	1	1	0	XX

Command Function	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Interface Setting	0	1	↑	1	0	1	1	1	0	0	0	B8h
	1	1	↑	0	WEMODE	EPF [1:0]		0	0	0	0	XX

Command Function	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Panel Control	0	1	↑	1	0	1	1	1	0	0	1	B9h
	1	1	↑	MY_ Panel	MX_ Panel	MV_ Panel	ML_ Panel	BGR_ Panel	MH_ Panel	SS_ Panel	GS_ Panel	XX
	1	1	↑	0	0	0	0	0	0	REV_ Panel	0	XX

Command Function	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	Hex
SPI Interface Setting	0	1	↑	1	0	1	1	1	0	1	0	BAh
	1	1	↑	Spitype	1	1	0	0	0r	0	0	XX

Command Function	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Power Control 1	0	1	↑	1	1	0	0	0	0	0	0	C0h
	1	1	↑	VD[2:0]			VE[2:0]			1	1	03
	1	1	↑	0	0	0	0	1	0	1	1	0B
	1	1	↑	0	0	0	0	BL [1:0]		1	0	0A

Command Function	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Power Control 2	0	1	↑	1	1	0	0	0	0	0	1	C1h
	1	1	↑	0	0	BG_ISC [1:0]		0	1	1	1	17
	1	1	↑	VRH1 [7:0]								90
	1	1	↑	VRH2 [7:0]								90
	1	1	↑	0	0	EXT_CPCK_SEL[5:4]		0	0	0	0	20

Command Function	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Power Control 3	0	1	↑	1	1	0	0	0	0	1	0	C2h
	1	1	↑	0	1	0	0	0	0	0	1	41
	1	1	↑	0	1	0	0	0	1	0	0	44
	1	1	↑	0	0	0	0	0	1	0	0	04
	1	1	↑	VGSP [7:0]								00
	1	1	↑	VGSN [7:0]								00

Command Function	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	Hex
VCOM Control 1	0	1	↑	1	1	0	0	0	1	1	1	C7h
	1	1	↑	VCM [7:0]								8F
	1	1	↑	nVM	0	0	0	0	0	0	0	80

Command Function	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Backlight Control 1	0	1	↑	1	1	0	0	1	0	0	0	C8h
	1	1	↑	PWM_DIV [7:0]								XX

Command Function	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Backlight Control 2	0	1	↑	1	1	0	0	1	0	0	1	C9h
	1	1	↑	THRES_MOV [3:0]			THRES_STILL [3:0]					XX

Command Function	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Backlight Control 3	0	1	↑	1	1	0	0	1	0	1	0	CAh
	1	1	↑	0	0	0	0	THRES_UI [3:0]				XX

Command Function	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Backlight Control 4	0	1	↑	1	1	0	0	1	0	1	1	CBh
	1	1	↑	DTH_MOV [3:0]				DTH_STILL [3:0]				XX

Command Function	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Backlight Control 5	0	1	↑	1	1	0	0	1	1	0	0	CCh
	1	1	↑	0	0	0	0	DTH_UI [3:0]				XX

Command Function	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Backlight Control 6	0	1	↑	1	1	0	0	1	1	0	1	CDh
	1	1	↑	0	DIM_MOV [2:0]			0	DIM_STILL [2:0]			XX

Command Function	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Backlight Control 7	0	1	↑	1	1	0	0	1	1	1	0	CEh
	1	1	↑	DIM_MIN [3:0]				0	DIM_UI [2:0]			XX

Command Function	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Backlight Control 8	0	1	↑	1	1	0	0	1	1	1	1	CFh
	1	1	↑	0	0	0	0	0	LEDONR	LEDON POL	PWM POL	XX

Command Function	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	Hex
NV Memory Write	0	1	↑	1	1	0	1	0	0	0	0	D0h
	1	1	↑	PGM_DATA [7:0]								XX
	1	1	↑	PGM_ADR [7:0]								XX

Command Function	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	Hex
NV Memory Protection Key	0	1	↑	1	1	0	1	0	0	0	1	D1h
	1	1	↑	KEY [23:16]								XX
	1	1	↑	KEY [15:8]								XX
	1	1	↑	KEY [7:0]								XX

Command Function	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	Hex
NV Memory Status Read	0	1	↑	1	1	0	1	0	0	1	0	D2h
	1	↑	1	Dummy read								XX
	1	↑	1	0	ID2_Mk [2:0]			0	ID1_Mk [2:0]			XX
	1	↑	1	OTP Busy	VCM_Mk [2:0]			0	ID3_Mk [2:0]			XX
	1	↑	1	0	0	0	0	RB9_P2_Mk		RB9_P1_Mk		XX

Command Function	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Engineering Setting	0	1	↑	1	1	0	1	1	1	1	1	DFh
	1	1	↑	0	0	0	0	0	0	0	0	00
	1	1	↑	0	0	0	0	0	0	0	0	00
	1	1	↑	0	0	0	0	0	0	0	0	00
	1	1	↑	0	0	0	0	0	0	0	0	00
	1	1	↑	0	0	0	0	0	0	0	0	00
	1	1	↑	0	0	dsi_pclk_div	0	0	0	0	0	00

Command Function	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Positive Gamma Control	0	1	↑	1	1	1	0	0	0	0	0	E0h
	1	1	↑	0	0	VP0 [5:0]						XX
	1	1	↑	0	0	VP4 [5:0]						XX
	1	1	↑	0	0	VP8 [5:0]						XX
	1	1	↑	0	0	0	VP16 [4:0]					XX
	1	1	↑	0	0	0	VP32 [4:0]					XX
	1	1	↑	0	0	0	VP52 [4:0]					XX
	1	1	↑	0	0	0	0	VP80 [3:0]				XX
	1	1	↑	0	0	0	0	VP108 [3:0]				XX
	1	1	↑	0	0	0	0	VP147 [3:0]				XX
	1	1	↑	0	0	0	0	VP175 [3:0]				XX
	1	1	↑	0	0	0	VP203 [4:0]					XX
	1	1	↑	0	0	0	VP223 [4:0]					XX
	1	1	↑	0	0	0	VP239 [4:0]					XX
	1	1	↑	0	0	VP247 [5:0]						XX
	1	1	↑	0	0	VP251 [5:0]						XX
	1	1	↑	0	0	VP255 [5:0]						XX

Command Function	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Negative Gamma Control	0	1	↑	1	1	1	0	0	0	0	1	E1h
	1	1	↑	0	0	VN0 [5:0]						XX
	1	1	↑	0	0	VN4 [5:0]						XX
	1	1	↑	0	0	VN8 [5:0]						XX
	1	1	↑	0	0	0	VN16 [4:0]					XX
	1	1	↑	0	0	0	VN32 [4:0]					XX
	1	1	↑	0	0	0	VN52 [4:0]					XX
	1	1	↑	0	0	0	0	VN80 [3:0]				XX
	1	1	↑	0	0	0	0	VN108 [3:0]				XX
	1	1	↑	0	0	0	0	VN147 [3:0]				XX
	1	1	↑	0	0	0	0	VN175 [3:0]				XX
	1	1	↑	0	0	0	VN203 [4:0]					XX
	1	1	↑	0	0	0	VN223 [4:0]					XX
	1	1	↑	0	0	0	VN239 [4:0]					XX
	1	1	↑	0	0	VN247 [5:0]						XX
	1	1	↑	0	0	VN251 [5:0]						XX
	1	1	↑	0	0	VN255 [5:0]						XX

Command Function	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Digital Gamma Control 1	0	1	↑	1	1	1	0	0	0	1	0	E2h
	1	1	↑	RCA0 [3:0]				BCA0 [3:0]				XX
	1	1	↑	RCA1 [3:0]				BCA1 [3:0]				XX
	1	1	↑	:				:				XX
	1	1	↑	RCAx [3:0]				BCAx [3:0]				XX
	1	1	↑	:				:				XX
	1	1	↑	RCA62 [3:0]				BCA62 [3:0]				XX
	1	1	↑	RCA63 [3:0]				BCA63 [3:0]				XX

Command Function	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Digital Gamma Control 2	0	1	↑	1	1	1	0	0	0	1	1	E3h
	1	1	↑	RFA0 [3:0]				BFA0 [3:0]				XX
				:				:				XX
	1	1	↑	RFAx [3:0]				BFAx [3:0]				XX
				:				:				XX
	1	1	↑	RFA256 [3:0]				BFA256 [3:0]				XX
	1	1	↑	0	0	0	0	0	0	0	0	00

Command Function	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	Hex
D3GE	0	1	↑	1	1	1	0	1	0	1	0	EAh
	1	1	↑	0	0	0	0	0	0	En_3G	Dith_en	XX

Command Function	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	Hex
VGMP / VGMN / VGSP / VGSN Voltage Measurement Set	0	1	↑	1	1	1	0	1	1	0	1	EDh
	1	1	↑	0	1	1	1	1	1	1	1	7F
	1	1	↑	0	0	0	0	0	1	1	1	07

Command Function	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	Hex
PTCTRL1	0	1	↑	1	1	1	1	0	0	0	1	F1h
	1	1	↑	0	0	1	0	1	0	0	1	29
	1	1	↑	Chopper_opt	Chopper_sel[1:0]		0	1	0	1	0	CA
	1	1	↑	0	0	Outsre	0	0	1	1	1	07

Command Function	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	Hex
PTCTRL2	0	1	↑	1	1	1	1	0	0	1	0	F2h
	1	1	↑	SDTI [1:0]		0	0	0	CRTI [2:0]			40
	1	1	↑	1	1	0	1	0	EQTl [2:0]			D2
	1	1	↑	0	creqpc	0	1	0	PCTl [2:0]			52
	1	1	↑	0	0	1	0	1	0	SDTI[2]	0	2A

Command Function	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	Hex
DVDD Voltage Setting	0	1	↑	1	1	1	1	0	0	1	1	F3h
	1	1	↑	0	1	1	1	0	0	0	0	70

Command Function	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	Hex
PWCTRL 5	0	1	↑	1	1	1	1	0	1	0	1	F5h
	1	1	↑	0	1	0	0	0	0	1	0	42
	1	1	↑	0	0	0	0	0	1	0	0	04
	1	1	↑	1	0	VRGH[5:0]						80

Command Function	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Panel Resolution Selection Set	0	1	↑	1	1	1	1	0	1	1	1	F7h
	1	1	↑	1	0	0	0	0	rso_in_test_mode[2:0]			80

Command Function	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RDEXTCSPI	0	1	↑	1	1	1	1	1	0	1	1	FBh
	1	1	↑	ext_spi_read_en	ext_spi_cnt[6:0]							XX
	1	1	↑	0	0	0	0	0	0	ext_spi_cnt[8:7]		XX

Command Function	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	Hex
LVGL Voltage Setting	0	1	↑	1	1	1	1	1	1	0	0	FCh
	1	1	↑	0	0	0	EXB1T_IN	LVGL_SEL[3:0]				04

Command Function	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	Hex
External Power Selection Set	0	1	↑	1	1	1	1	1	1	0	1	FDh
	1	1	↑	0	0	0	0	1	0	1	0	0A
	1	1	↑	0	0	pccs_reg[1:0]		0	0	0	0	00

Command Function	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	Hex
EXTC Command Set enable register	0	1	↑	1	1	1	1	1	1	1	1	FFh
	1	1	↑	1	1	1	1	1	1	1	1	FF
	1	1	↑	1	0	0	1	1	0	0	0	98
	1	1	↑	0	0	0	0	0	1	1	0	06

Notes:

- Undefined commands are treated as NOP (00h) command.
- B0 to D9 and DE to FF are for factory use of display supplier. Users can decide if these commands are available or they are treated as NOP (00h) commands before shipping to Users. The default value is NOP (00h).
- Commands 10h, 12h, 13h, 26h, 28h, 29h, 30h, 36h (Bit D4 only), 38h and 39h are updated during V-SYNC. When the module is in the Sleep Out mode to avoid abnormal visual effects. During the Sleep In mode, these commands are updated immediately. Read status (09h), Read display power mode (0Ah), Read display MADCTL (0Bh), Read display pixel format (0Ch), Read display image mode (0Dh), Read display signal mode (0Eh) and Read display self-diagnostic result (0Fh) are updated immediately in both Sleep In mode and Sleep Out mode.

4.2. Command Description

4.2.1. NOP (00h)

00h	NOP (No Operation)																								
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	0	0	0	0	0	0	0	0	00h												
Parameter	No parameter																								
Description	This command is an empty command. It does not have any effect on the ILI9806G. However, it can be used to terminate the Frame Memory Write or Read as described in RAMWR (Memory Write) and RAMRD (Memory Read) Commands. X = void																								
Restriction	None																								
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>N/A</td></tr><tr><td>S/W Reset</td><td>N/A</td></tr><tr><td>H/W Reset</td><td>N/A</td></tr></table>													Status	Default Value	Power On Sequence	N/A	S/W Reset	N/A	H/W Reset	N/A				
Status	Default Value																								
Power On Sequence	N/A																								
S/W Reset	N/A																								
H/W Reset	N/A																								
Flow Chart	None																								

4.2.2. Software Reset (01h)

01h	SWRESET (Software Reset)																								
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	0	0	0	0	0	0	0	1	01h												
Parameter	No parameter																								
Description	<p>When the Software Reset command is written, it causes software reset. It resets the commands and parameters to their S/W Reset default values. (See default tables in each command description.)</p> <p>Note: The Frame Memory contents are not affected by this command.</p> <p>X = void</p>																								
Restriction	<p>It is necessary to wait 5msec before sending a new command after software reset. The display module loads all factory default values of the display supplier to the registers during this 5msec. If Software Reset is applied during the Sleep Out mode, it will be necessary to wait 120msec before sending the Sleep Out command.</p> <p>The Software Reset Command cannot be sent during the Sleep Out sequence.</p>																								
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>N/A</td></tr><tr><td>S/W Reset</td><td>N/A</td></tr><tr><td>H/W Reset</td><td>N/A</td></tr></table>													Status	Default Value	Power On Sequence	N/A	S/W Reset	N/A	H/W Reset	N/A				
Status	Default Value																								
Power On Sequence	N/A																								
S/W Reset	N/A																								
H/W Reset	N/A																								
Flow Chart	<div><div><div>SWRESET(01h)</div><div>Display whole blank screen</div><div>Set Commands to S/W Default Values</div><div>Sleep In Mode</div></div><div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div></div>																								

4.2.3. Read display identification information (04h)

04h	RDDIDIF (Read Display Identification Information)																								
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	0	0	0	0	0	1	0	0	04h												
1 st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	XX												
2 nd Parameter	1	↑	1	XX	ID1 [7:0]								XX												
3 rd Parameter	1	↑	1	XX	ID2 [7:0]								XX												
4 th Parameter	1	↑	1	XX	ID3 [7:0]								XX												
Description	This read byte returns 24 bits of display identification information.																								
	The 1 st parameter is a dummy data.																								
	The 2 nd parameter (ID1 [7:0]): LCD module's manufacturer ID.																								
	The 3 rd parameter (ID2 [7:0]): LCD module/driver version ID.																								
	The 4 th parameter (ID3 [7:0]): LCD module/driver ID.																								
X = void																									
Restriction																									
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
	Status	Availability																							
	Normal Mode On, Idle Mode Off, Sleep Out	Yes																							
	Normal Mode On, Idle Mode On, Sleep Out	Yes																							
	Partial Mode On, Idle Mode Off, Sleep Out	Yes																							
	Partial Mode On, Idle Mode On, Sleep Out	Yes																							
Sleep In	Yes																								
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>See description</td></tr><tr><td>S/W Reset</td><td>See description</td></tr><tr><td>H/W Reset</td><td>See description</td></tr></table>													Status	Default Value	Power On Sequence	See description	S/W Reset	See description	H/W Reset	See description				
	Status	Default Value																							
	Power On Sequence	See description																							
	S/W Reset	See description																							
H/W Reset	See description																								
Flow Chart	<div><div><div>RDDIDIF(04h)</div><div></div></div><div></div><div>1st Parameter: Dummy Read 2nd Parameter: Send LCD module's manufacturer information 3rd Parameter: Send panel type and LCM/driver version information 4th Parameter: Send module/driver information</div></div> <div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>																								

4.2.4. Read Number of the Errors on DSI (05h)

05h	RDNUMED (Read Number of the Errors on DSI)																								
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	0	0	0	0	0	1	0	1	05h												
1 st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	XX												
2 nd Parameter	1	↑	1	XX	P [7:0]								XX												
Description	<p>The 1st parameter is a dummy data.</p> <p>The 2nd parameter indicates the amount of errors on the DSI. The more detailed description of the bits is below.</p> <p>P [6..0] bits indicate the amount of the error. P [7] is set to 1 if there is overflow with P [6..0] bits.</p> <p>P [7...0] bits are set to 0 (and RDDSM (0Eh)'s D0 is set 0 at the same time) after the second parameter information is sent (= the read function is completed). This function always returns P [7...0] = 00h if the parallel MPU interface is selected.</p> <p>X = void</p>																								
Restriction	<p>The ILI9806G sends the 2nd parameter value to the data lines if the MPU wants to read more than one parameter (= more than 2 RDX cycle) on the parallel MPU interface.</p> <p>Only the 2nd parameter is sent on DSI; the 1st parameter is not sent.</p>																								
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>00_{HEX}</td></tr><tr><td>S/W Reset</td><td>00_{HEX}</td></tr><tr><td>H/W Reset</td><td>00_{HEX}</td></tr></table>													Status	Default Value	Power On Sequence	00 _{HEX}	S/W Reset	00 _{HEX}	H/W Reset	00 _{HEX}				
Status	Default Value																								
Power On Sequence	00 _{HEX}																								
S/W Reset	00 _{HEX}																								
H/W Reset	00 _{HEX}																								
Flow Chart	<div><div><div>RDNUMPE (05h)</div><div>↓</div><div>1st Parameter: Dummy Read 2nd Parameter: Read</div><div>↓</div><div>P [7:0] = 00h RDDSM (0Eh)'s D0 = 0</div></div><div>Host ----- Driver</div><div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div></div>																								

4.2.5. Get Red Channel (06h)

06h	RDRED (Read Red Color)																								
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	0	0	0	0	0	1	1	0	06h												
1 st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	XX												
2 nd Parameter	1	↑	1	XX	R [7:0]								XX												
Description	<p>This command returns the red component value of the first pixel in the active frame.</p> <p>Only the relevant bits are used according to the pixel format. Unused bits are set to 0.</p> <p>16-bit format R5 is MSB and R1 is LSB; R7, R6 and R0 are set to 0.</p> <p>18-bit format R5 is MSB and R0 is LSB; R7, R6 are set to 0.</p> <p>24-bit format R7 is MSB and R0 is LSB.</p> <p>X = void</p>																								
Restriction																									
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>N/A</td></tr><tr><td>S/W Reset</td><td>N/A</td></tr><tr><td>H/W Reset</td><td>N/A</td></tr></table>													Status	Default Value	Power On Sequence	N/A	S/W Reset	N/A	H/W Reset	N/A				
Status	Default Value																								
Power On Sequence	N/A																								
S/W Reset	N/A																								
H/W Reset	N/A																								
Flow Chart	<div><div><div>Serial I/F Mode</div><div>Read R Color</div><div>↓</div><div>Send D[7:0]</div></div><div>Host Driver</div></div> <div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>																								

4.2.6. Get Green Channel (07h)

07h	RDGREEN (Read Green Color)																								
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	0	0	0	0	0	1	1	1	07h												
1 st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	XX												
2 nd Parameter	1	↑	1	XX	G [7:0]								XX												
Description	<p>This command returns the green component value of the first pixel in the active frame.</p> <p>Only the relevant bits are used according to the pixel format. Unused bits are set to 0.</p> <p>16-bit format G5 is MSB and G0 is LSB; G7, G6 are set to 0.</p> <p>18-bit format G5 is MSB and G0 is LSB; G7, G6 are set to 0.</p> <p>24-bit format G7 is MSB and G0 is LSB.</p> <p>X = void</p>																								
Restriction																									
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>N/A</td></tr><tr><td>S/W Reset</td><td>N/A</td></tr><tr><td>H/W Reset</td><td>N/A</td></tr></table>													Status	Default Value	Power On Sequence	N/A	S/W Reset	N/A	H/W Reset	N/A				
Status	Default Value																								
Power On Sequence	N/A																								
S/W Reset	N/A																								
H/W Reset	N/A																								
Flow Chart	<div><div><div><div><div>Serial I/F Mode</div><div>Read Green Color</div></div><div><div>Send D[7:0]</div></div></div><div><div>Host Driver</div></div></div><div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div></div>																								

4.2.7. Get Blue Channel (08h)

08h	RDBLUE (Read Blue Color)																								
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	0	0	0	0	1	0	0	0	08h												
1 st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	XX												
2 nd Parameter	1	↑	1	XX	B [7:0]								XX												
Description	<p>This command returns the blue component value of the first pixel in the active frame.</p> <p>Only the relevant bits are used according to the pixel format. Unused bits are set to 0.</p> <p>16-bit format B5 is MSB and B1 is LSB; B7, B6 and B0 are set to 0.</p> <p>18-bit format B5 is MSB and B0 is LSB; B7, B6 are set to 0.</p> <p>24-bit format B7 is MSB and B0 is LSB.</p> <p>X = void</p>																								
Restriction																									
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>N/A</td></tr><tr><td>S/W Reset</td><td>N/A</td></tr><tr><td>H/W Reset</td><td>N/A</td></tr></table>													Status	Default Value	Power On Sequence	N/A	S/W Reset	N/A	H/W Reset	N/A				
Status	Default Value																								
Power On Sequence	N/A																								
S/W Reset	N/A																								
H/W Reset	N/A																								
Flow Chart	<div><div><div>Serial I/F Mode</div><div><div>Read Blue Color</div><div>↓</div><div>Send D[7:0]</div></div></div><div>Host Driver</div></div> <div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>																								

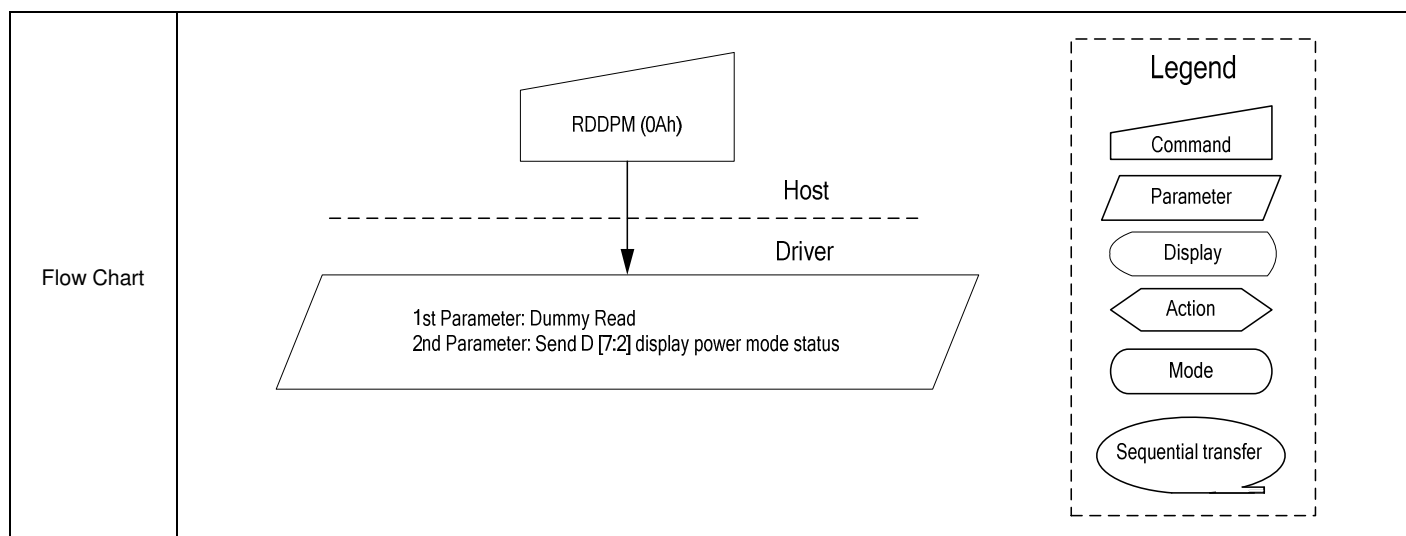
4.2.8. Read Display Status (09h)

09h	RDDST (Read Display Status)												
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	0	1	0	0	1	09h
1 st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
2 nd Parameter	1	↑	1	XX	D [31:24]							XX	
3 rd Parameter	1	↑	1	XX	D [23:16]							XX	
4 th Parameter	1	↑	1	XX	D [15:8]							XX	
5 th Parameter	1	↑	1	XX	D [7:0]							XX	
Description	This command indicates the current status of the display, as described in the table below:												
	Bit	Description			Value	Status							
	D31	Booster voltage status			0	Booster Off							
					1	Booster On							
	D30	Row address order			0	Top to Bottom (When MADCTL D7 = 0)							
					1	Bottom to Top (When MADCTL D7 = 1)							
	D29	Column address order			0	Left to Right (When MADCTL D6 = 0)							
					1	Right to Left (When MADCTL D6 = 1)							
	D28	Row/column exchange			0	Normal Mode (When MADCTL D5 = 0)							
					1	Reverse Mode (When MADCTL D5 = 1)							
	D27	Vertical refresh			0	LCD Refresh Top to Bottom (When MADCTL D4 = 0)							
					1	LCD Refresh Bottom to Top (When MADCTL D4 = 1)							
	D26	RGB/BGR order			0	RGB (When MADCTL D3 = 0)							
					1	BGR (When MADCTL D3= 1)							
	D25	Horizontal refresh order			0	LCD Refresh Left to Right (When MADCTL D2 = 0)							
					1	LCD Refresh Right to Left (When MADCTL D2 = 1)							
	D24	Source scan sequence			0	Source output Left to Right (When MADCTL D1 = 0)							
					1	Source output Right to Left (When MADCTL D1 = 1)							
	D23	Gate scan sequence			0	Gate output Top to Bottom (When MADCTL D0 = 0)							
					1	Gate output Bottom to Top (When MADCTL D0 = 1)							
	D [22:20]	Interface color pixel format definition			101	16-bit/pixel							
					110	18-bit/pixel							
					111	24-bit/pixel							
					others	Not defined							
	D19	Idle Mode On/Off			0	Idle Mode Off							
					1	Idle Mode On							
	D18	Partial Mode On/Off			0	Partial Mode Off							
					1	Partial Mode On							
	D17	Sleep In/Out			0	Sleep In Mode							
					1	Sleep Out Mode							
	D16	Display Normal Mode On/Off			0	Display Normal Mode Off (Partial or Scrolling Mode)							
					1	Display Normal Mode On							
	D15	Vertical scrolling status			0	Vertical Scroll Off							
					1	Vertical Scroll On							
	D14	Horizontal Scrolling Status			0	This bit is not applicable for this project, so it is set to 0							
	D13	Inversion status			0	Inversion Off							
					1	Inversion On							

	D12	All Pixel On	0	Normal mode												
			1	All Pixels On												
	D11	All Pixel Off	0	Normal mode												
			1	All Pixels Off												
	D10	Display ON/OFF	0	Display is OFF												
			1	Display is ON												
	D9	Tearing effect line ON/OFF	0	Tearing Effect Line OFF												
			1	Tearing Effect ON												
	D [8:6]	Gamma curve selection	000	Gamma Curve 1												
			001	Gamma Curve 2												
			010	Gamma Curve 3												
			011	Gamma Curve 4												
			others	Not defined												
	D5	Tearing Effect Line mode	0	Mode 1, V-Blanking only												
			1	Mode 2, both H-Blanking and V-Blanking.												
	D4	Horizontal Sync. (HSYNC, DPI I/F) (Note)	0	Horizontal Sync. line is Off (Low)												
			1	Horizontal Sync. line is On (High)												
	D3	Vertical Sync. (VSYNC, DPI I/F) (Note)	0	Vertical Sync. line is Off (Low)												
			1	Vertical Sync. line is On (High)												
	D2	DOT Clock (DCK, DPI I/F) (Note)	0	DCK line is Off (Low)												
			1	DCK line is On (High)												
	D1	Data Enable (ENABLE, DPI I/F) (Note)	0	DE line is Off (Low)												
			1	DE line is On (High)												
	D0	Parity Error on DSI	0	No Parity Error												
			1	Parity Error												
Note: This bit indicates the current status of the line when this command is sent.																
X = void																
Restriction																
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>				Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability															
Normal Mode On, Idle Mode Off, Sleep Out	Yes															
Normal Mode On, Idle Mode On, Sleep Out	Yes															
Partial Mode On, Idle Mode Off, Sleep Out	Yes															
Partial Mode On, Idle Mode On, Sleep Out	Yes															
Sleep In	Yes															
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>32'h00710000h</td></tr><tr><td>S/W Reset</td><td>D20~D30 no change, keep the current status before S/W Reset</td></tr><tr><td>H/W Reset</td><td>32'h00710000h</td></tr></table>				Status	Default Value	Power On Sequence	32'h00710000h	S/W Reset	D20~D30 no change, keep the current status before S/W Reset	H/W Reset	32'h00710000h				
Status	Default Value															
Power On Sequence	32'h00710000h															
S/W Reset	D20~D30 no change, keep the current status before S/W Reset															
H/W Reset	32'h00710000h															
Flow Chart	<div><div>RDDST (09h)</div><div><div>Host</div><div>Driver</div></div><div>1st Parameter: Dummy Read 2nd Parameter: Send D [31:25] display status 3rd Parameter: Send D [22:16] display status 4th Parameter: Send D [10:8] display status 5th Parameter: Send D [7:0] display status</div></div> <div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>															

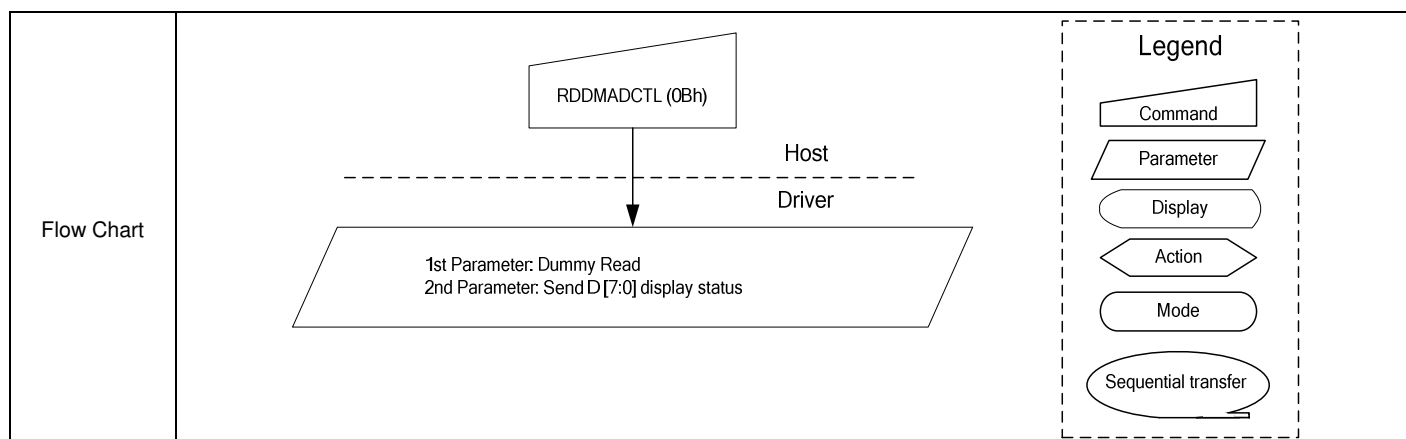
4.2.9. Read Display Power Mode (0Ah)

0Ah	RDDPM (Read Display Power Mode)																								
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	0	0	0	0	1	0	1	0	0Ah												
1 st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	XX												
2 nd Parameter	1	↑	1	XX	D [7:2]						0	0	XX												
Description	This command indicates the current status of the display, as described in the table below.																								
	Bit	Description				Value		Status																	
	D7	Booster Voltage Status				0		Booster Off or has a fault																	
						1		Booster On and working OK																	
	D6	Idle Mode On/Off				0		Idle Mode Off																	
						1		Idle Mode On																	
	D5	Partial Mode On/Off				0		Partial Mode Off																	
						1		Partial Mode On																	
	D4	Sleep In/Out				0		Sleep In Mode																	
						1		Sleep Out Mode																	
	D3	Display Normal Mode On/Off				0		Display Normal Mode Off																	
						1		Display Normal Mode On																	
	D2	Display On/Off				0		Display is Off																	
						1		Display is On																	
	D1	Not Defined				--		Set to 0																	
D0	Not Defined				--		Set to 0																		
X = void																									
Restriction	The ILI9806G sends the 2 nd parameter value to the data lines if the MPU wants to read more than one parameter (= more than 2 RDX cycle) on the parallel MPU interface. Only the 2 nd parameter is sent on the DSI; the 1 st parameter is not sent.																								
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>08_{HEX}</td></tr><tr><td>S/W Reset</td><td>08_{HEX}</td></tr><tr><td>H/W Reset</td><td>08_{HEX}</td></tr></table>													Status	Default Value	Power On Sequence	08 _{HEX}	S/W Reset	08 _{HEX}	H/W Reset	08 _{HEX}				
Status	Default Value																								
Power On Sequence	08 _{HEX}																								
S/W Reset	08 _{HEX}																								
H/W Reset	08 _{HEX}																								



4.2.10. Read Display MADCTL (0Bh)

0Bh	RDDMADCTL (Read Display MADCTL)																								
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	0	0	0	0	1	0	1	1	0Bh												
1 st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	XX												
2 nd Parameter	1	↑	1	XX	D [7:0]							XX													
Description	This command indicates the current status of the display, as described in the table below.																								
	Bit	Description			Value	Status																			
	D7	Page Address Order			0	Top to Bottom (When MADCTL D7= 0)																			
					1	Bottom to Top (When MADCTL D7= 1)																			
	D6	Column Address Order			0	Left to Right (When MADCTL D6= 0)																			
					1	Right to Left (When MADCTL D6= 1)																			
	D5	Page/Column Order			0	Normal Mode (When MADCTL D5= 0)																			
					1	Reverse Mode (When MADCTL D5= 1)																			
	D4	Line Address Order			0	LCD Refresh Top to Bottom (When MADCTL D4= 0)																			
					1	LCD Refresh Bottom to Top (When MADCTL D4= 1)																			
	D3	RGB/BGR Order			0	RGB (When MADCTL D3= 0)																			
					1	BGR (When MADCTL D3= 1)																			
	D2	Display Data Latch Data Order			0	LCD Refresh Left to Right (When MADCTL D2= 0)																			
					1	LCD Refresh Right to Left (When MADCTL D2= 1)																			
	D1	Source scan sequence			0	Source output Left to Right																			
					1	Source output Right to Left																			
D0	Gate scan sequence			0	Gate output Top to Bottom																				
				1	Gate output Bottom to Top																				
X = void																									
Restriction	The ILI9806G sends the 2 nd parameter value to the data lines if the MPU wants to read more than one parameter (= more than 2 RDX cycle) on the parallel MPU interface. Only the 2 nd parameter is sent on the DSI; the 1 st parameter is not sent.																								
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>00_{HEX}</td></tr><tr><td>S/W Reset</td><td>No Change</td></tr><tr><td>H/W Reset</td><td>00_{HEX}</td></tr></table>													Status	Default Value	Power On Sequence	00 _{HEX}	S/W Reset	No Change	H/W Reset	00 _{HEX}				
Status	Default Value																								
Power On Sequence	00 _{HEX}																								
S/W Reset	No Change																								
H/W Reset	00 _{HEX}																								

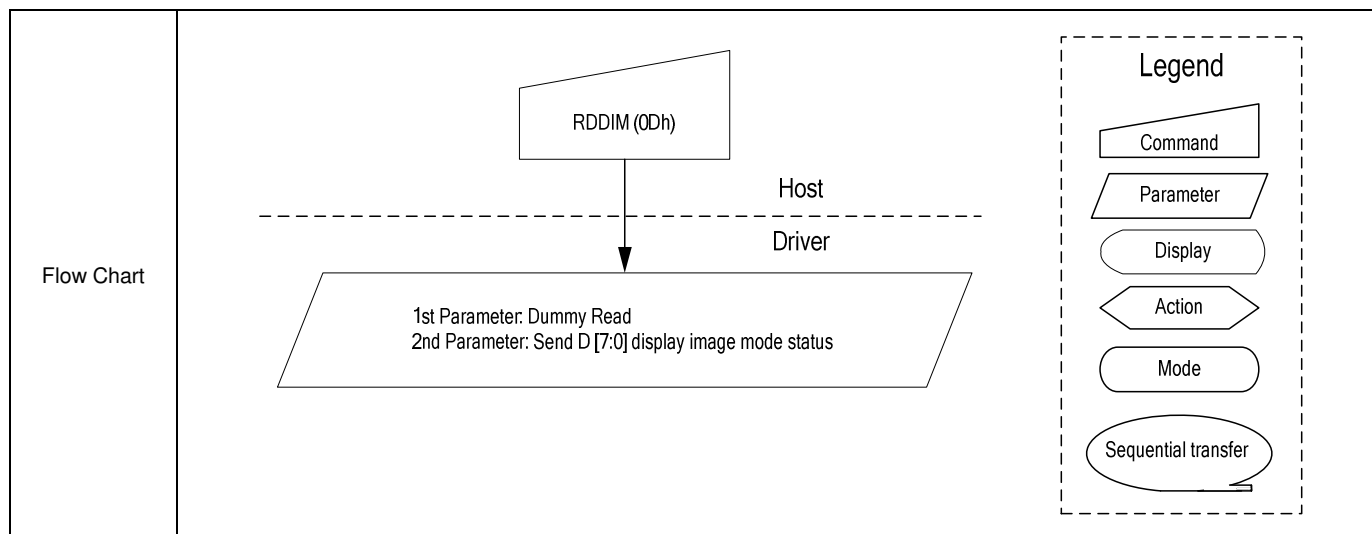


4.2.11. Read Display Pixel Format (0Ch)

0Ch	RDDCOLMOD (Read Display COLMOD)																																															
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																			
Command	0	1	↑	XX	0	0	0	0	1	1	0	0	0Ch																																			
1 st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	XX																																			
2 nd Parameter	1	↑	1	XX	0	DPI [2:0]			0	DBI [2:0]			XX																																			
Description	This command indicates the current status of the display, as described in the table below:																																															
	<table><tr><th colspan="3">DPI [2:0]</th><th>RGB Interface Format</th></tr><tr><td>1</td><td>0</td><td>1</td><td>16-bit/pixel</td></tr><tr><td>1</td><td>1</td><td>0</td><td>18-bit/pixel</td></tr><tr><td>1</td><td>1</td><td>1</td><td>24-bit/pixel</td></tr><tr><td colspan="3">Others</td><td>Reserved</td></tr></table>				DPI [2:0]			RGB Interface Format	1	0	1	16-bit/pixel	1	1	0	18-bit/pixel	1	1	1	24-bit/pixel	Others			Reserved	<table><tr><th colspan="3">DBI [2:0]</th><th>CPU Interface Format</th></tr><tr><td>1</td><td>0</td><td>1</td><td>16-bit/pixel</td></tr><tr><td>1</td><td>1</td><td>0</td><td>18-bit/pixel</td></tr><tr><td>1</td><td>1</td><td>1</td><td>24-bit/pixel</td></tr><tr><td colspan="3">Others</td><td>Reserved</td></tr></table>				DBI [2:0]			CPU Interface Format	1	0	1	16-bit/pixel	1	1	0	18-bit/pixel	1	1	1	24-bit/pixel	Others			Reserved
	DPI [2:0]			RGB Interface Format																																												
	1	0	1	16-bit/pixel																																												
	1	1	0	18-bit/pixel																																												
1	1	1	24-bit/pixel																																													
Others			Reserved																																													
DBI [2:0]			CPU Interface Format																																													
1	0	1	16-bit/pixel																																													
1	1	0	18-bit/pixel																																													
1	1	1	24-bit/pixel																																													
Others			Reserved																																													
X = void																																																
Restriction	The ILI9806G sends the 2 nd parameter value to the data lines if the MPU wants to read more than one parameter (= more than 2 RDX cycle) on the parallel MPU interface. Only the 2 nd parameter is sent on the DSI; the 1 st parameter is not sent.																																															
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes																							
Status	Availability																																															
Normal Mode On, Idle Mode Off, Sleep Out	Yes																																															
Normal Mode On, Idle Mode On, Sleep Out	Yes																																															
Partial Mode On, Idle Mode Off, Sleep Out	Yes																																															
Partial Mode On, Idle Mode On, Sleep Out	Yes																																															
Sleep In	Yes																																															
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>07_{HEX}</td></tr><tr><td>S/W Reset</td><td>07_{HEX}</td></tr><tr><td>H/W Reset</td><td>07_{HEX}</td></tr></table>													Status	Default Value	Power On Sequence	07 _{HEX}	S/W Reset	07 _{HEX}	H/W Reset	07 _{HEX}																											
Status	Default Value																																															
Power On Sequence	07 _{HEX}																																															
S/W Reset	07 _{HEX}																																															
H/W Reset	07 _{HEX}																																															
Flow Chart	<div><div><div>RDDCOLMOD (0Ch)</div><div>↓</div><div>1st Parameter: Dummy Read 2nd Parameter: Send D [7:0] display pixel format status</div></div><div>Host ----- Driver</div></div> <div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>																																															

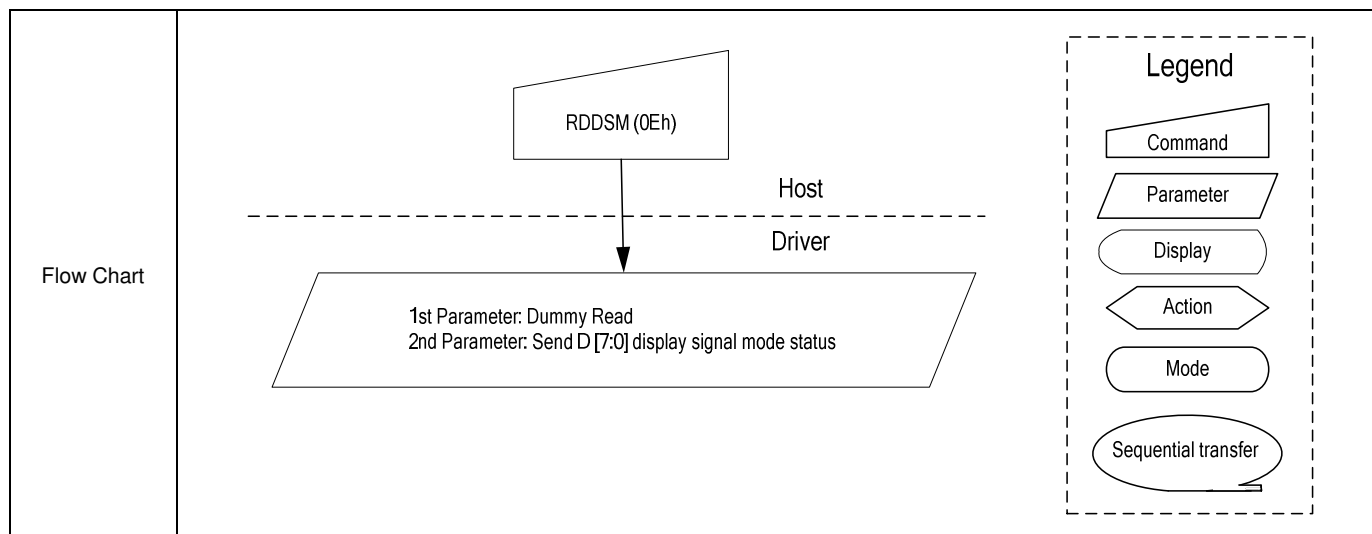
4.2.12. Read Display Image Mode (0Dh)

0Dh	RDDIM (Read Display Image Mode)																													
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX																	
Command	0	1	↑	XX	0	0	0	0	1	1	0	1	0Dh																	
1 st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	XX																	
2 nd Parameter	1	↑	1	XX	D [7:0]								XX																	
Description	This command indicates the Image Mode status of the display, as described in the Tables below:																													
	Bit	Description				Value	Status																							
	D7	Vertical Scrolling Status				0	Vertical Scrolling is Off																							
						1	Vertical Scrolling is On																							
	D6	Horizontal Scrolling Status (Reserved)				0	It is not applicable for this project, so set to 0																							
	D5	Inversion On/Off				0	Inversion is Off																							
						1	Inversion is On																							
	D4	All Pixels On				0	Normal Display																							
						1	White Display																							
	D3	All Pixels Off				0	Normal Display																							
1						Black Display																								
<table><tr><th>Bit D [2:0]</th><th>Gamma Cure Selection</th><th>Gamma Set (26h) Parameter</th></tr><tr><td>000</td><td>Gamma curve 1</td><td>GC0</td></tr><tr><td>001</td><td>Gamma curve 2</td><td>GC1</td></tr><tr><td>010</td><td>Gamma curve 3</td><td>GC2</td></tr><tr><td>011</td><td>Gamma curve 4</td><td>GC3</td></tr><tr><td>Others</td><td>Not defined</td><td>Not defined</td></tr></table>													Bit D [2:0]	Gamma Cure Selection	Gamma Set (26h) Parameter	000	Gamma curve 1	GC0	001	Gamma curve 2	GC1	010	Gamma curve 3	GC2	011	Gamma curve 4	GC3	Others	Not defined	Not defined
Bit D [2:0]	Gamma Cure Selection	Gamma Set (26h) Parameter																												
000	Gamma curve 1	GC0																												
001	Gamma curve 2	GC1																												
010	Gamma curve 3	GC2																												
011	Gamma curve 4	GC3																												
Others	Not defined	Not defined																												
X = void																														
Restriction	The ILI9806G sends the 2 nd parameter value to the data lines if the MPU wants to read more than one parameter (= more than 2 RDX cycle) on the parallel MPU interface. Only the 2 nd parameter is sent on the DSI; the 1 st parameter is not sent.																													
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes					
Status	Availability																													
Normal Mode On, Idle Mode Off, Sleep Out	Yes																													
Normal Mode On, Idle Mode On, Sleep Out	Yes																													
Partial Mode On, Idle Mode Off, Sleep Out	Yes																													
Partial Mode On, Idle Mode On, Sleep Out	Yes																													
Sleep In	Yes																													
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>00_{HEX}</td></tr><tr><td>S/W Reset</td><td>00_{HEX}</td></tr><tr><td>H/W Reset</td><td>00_{HEX}</td></tr></table>													Status	Default Value	Power On Sequence	00 _{HEX}	S/W Reset	00 _{HEX}	H/W Reset	00 _{HEX}									
Status	Default Value																													
Power On Sequence	00 _{HEX}																													
S/W Reset	00 _{HEX}																													
H/W Reset	00 _{HEX}																													



4.2.13. Read Display Signal Mode (0Eh)

0Eh	RDDSM (Read Display Signal Mode)																								
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	0	0	0	0	1	1	1	0	0Eh												
1 st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	XX												
2 nd Parameter	1	↑	1	XX	D7	D6	D5	D4	D3	D2	D1	D0	XX												
Description	This command indicates the current status of the display, as described in the table below:																								
	Bit	Description				Value		Status																	
	D7	Tearing Effect Line On/Off				0		Tearing Effect Line OFF																	
						1		Tearing Effect Line ON																	
	D6	Tearing Effect Line Output Mode,				0		Tearing Effect Line Mode 1																	
						1		Tearing Effect Line Mode 2																	
	D5	Horizontal Sync. (RGB I/F) On/Off				0		HSYNC line is OFF (low)																	
						1		HSYNC line is ON (high)																	
	D4	Vertical Sync. (RGB I/F) On/Off				0		VSYNC line is OFF (low)																	
						1		VSYNC line is ON (high)																	
	D3	Pixel Clock (DCK, RGB I/F) On/Off				0		DCK line is OFF (low)																	
						1		DCK line is ON (high)																	
	D2	Data Enable (DE, RGB I/F) On/Off				0		Enable Line is OFF (low)																	
						1		Enable Line is ON (high)																	
	D1	Reserved				0		Reserved, so it is set to 0																	
	D0	Error on DSI,				0		No Error on DSI																	
1						Error on DSI																			
X = void																									
Restriction	The ILI9487 sends the 2 nd parameter value to the data lines if the MPU wants to read more than one parameter (= more than 2 RDX cycle) on the parallel MPU interface. Only the 2 nd parameter is sent on the DSI; the 1 st parameter is not sent.																								
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>00_{HEX}</td></tr><tr><td>S/W Reset</td><td>00_{HEX}</td></tr><tr><td>H/W Reset</td><td>00_{HEX}</td></tr></table>													Status	Default Value	Power On Sequence	00 _{HEX}	S/W Reset	00 _{HEX}	H/W Reset	00 _{HEX}				
Status	Default Value																								
Power On Sequence	00 _{HEX}																								
S/W Reset	00 _{HEX}																								
H/W Reset	00 _{HEX}																								



Legend

Command

Parameter

Display

Action

Mode

Sequential transfer

4.2.14. Read Display Self-Diagnostic Result (0Fh)

0Fh	RDDSDR (Read Display Self-Diagnostic Result)																								
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	0	0	0	0	1	1	1	1	0Fh												
1 st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	XX												
2 nd Parameter	1	↑	1	XX	D7	D6	D5	D4	0	0	0	D0	XX												
Description	This command indicates the status of the display self-diagnostic results after the Sleep Out command, as described in the table below:																								
	Bit	Description				Action																			
	D7	Register Loading Detection				Invert the D7 bit when the EEPROM and register values are the same.																			
	D6	Functionality Detection				Invert the D6 bit when the chip meets user's functionality requirements																			
	D5	Chip Attachment Detection				Set bit D5 to 0, if this function is not implemented.																			
	D4	Display Glass Break Detection				Set bit D4 to 0, if this function is not implemented.																			
	D3	Not Used				Set to 0																			
	D2	Not Used				Set to 0																			
	D1	Not Used				Set to 0																			
	D0	Checksums Comparison				0 = Checksums are the same 1 = Checksums are not the same																			
X = void																									
Restriction	It is necessary to wait 300ms after the last write access to registers on the User area before the Bit D0 value can be read.																								
	The ILI9487 sends the 2 nd parameter value to the data lines if the MPU wants to read more than one parameter (= more than 2 RDX cycle) on the parallel MPU interface.																								
	Only the 2 nd parameter is sent on the DSI; the 1 st parameter is not sent.																								
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
	Status	Availability																							
	Normal Mode On, Idle Mode Off, Sleep Out	Yes																							
	Normal Mode On, Idle Mode On, Sleep Out	Yes																							
	Partial Mode On, Idle Mode Off, Sleep Out	Yes																							
	Partial Mode On, Idle Mode On, Sleep Out	Yes																							
Sleep In	Yes																								
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>00_{HEX}</td></tr><tr><td>S/W Reset</td><td>00_{HEX}</td></tr><tr><td>H/W Reset</td><td>00_{HEX}</td></tr></table>													Status	Default Value	Power On Sequence	00 _{HEX}	S/W Reset	00 _{HEX}	H/W Reset	00 _{HEX}				
	Status	Default Value																							
	Power On Sequence	00 _{HEX}																							
	S/W Reset	00 _{HEX}																							
	H/W Reset	00 _{HEX}																							
Flow Chart	<div><div><div>RDDSDR (0Fh)</div><div>↓</div><div>1st Parameter: Dummy Read 2nd Parameter: Send D [7:0] display self-diagnostic status</div></div><div>Host ----- Driver</div></div> <div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>																								

4.2.15. Sleep In (10h)

10h	SLPIN (Sleep In)																								
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	0	0	0	1	0	0	0	0	10h												
Parameter	No parameter																								
Description	<p>This command causes the ILI9806G to enter the minimum power consumption mode.</p> <p>In this mode, the DC/DC converter, Internal oscillator, and panel scanning are all stopped.</p> <div><div>OUT</div><div>Blank</div><div>STOP</div></div> <p>The MPU interface and memory are still working, and the memory keeps its contents.</p> <p>X = Void</p>																								
Restriction	<p>This command has no effect when the module is already in the Sleep In mode. To exit the Sleep In mode, only the Sleep Out Command (11h) is workable. It is necessary to wait 5msec before sending the next command; this is to allow time for the supply voltages and clock circuits to become stable. It is necessary to wait 120msec after sending the Sleep Out command (when in the Sleep In Mode) before the Sleep In command can be sent.</p>																								
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Sleep In Mode</td></tr><tr><td>S/W Reset</td><td>Sleep In Mode</td></tr><tr><td>H/W Reset</td><td>Sleep In Mode</td></tr></table>													Status	Default Value	Power On Sequence	Sleep In Mode	S/W Reset	Sleep In Mode	H/W Reset	Sleep In Mode				
Status	Default Value																								
Power On Sequence	Sleep In Mode																								
S/W Reset	Sleep In Mode																								
H/W Reset	Sleep In Mode																								
Flow Chart	<div><div><div>SPLIN (10h)</div><div>Display whole blank screen (Automatic No effect to DISP ON/OFF commands)</div><div>Drain charge from LCD panel</div></div><div><div>Stop DC/DC Converter</div><div>Stop Internal Oscillator</div><div>Sleep In Mode</div></div></div> <div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>																								

4.2.16. Sleep Out (11h)

11h	SLPOUT (Sleep Out)																								
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	0	0	0	1	0	0	0	1	11h												
Parameter	No parameter																								
Description	<p>This command turns off the sleep mode.</p> <p>In this mode, the DC/DC converter is enabled, the Internal oscillator is started, and the panel scanning is started.</p> <div><div>OUT</div><div>STOP</div><div>Blank</div><div>Memory Contents (DISPON 29h is set)</div></div> <p>X = Void</p>																								
Restriction	<p>This command has no effect when the module is already in the Sleep Out mode. To exit the Sleep Out Mode, Sleep In command (10h), S/W reset command (01h), and H/W reset are workable. It is necessary to wait 5msec before sending the next command; this is to allow time for the supply voltages and clock circuits to become stable.</p> <p>The ILI9806G loads all factory default values of the display supplier to the registers during this 5msec. There cannot be any abnormal visual effect on the display image if factory defaults and register values are the same when this load is done and when the ILI9806G is already in the Sleep Out mode.</p> <p>The ILI9806G performs self-diagnostic functions during this 5msec. It is necessary to wait 120msec after sending the Sleep In command (when in the Sleep Out mode) before the Sleep Out command can be sent.</p>																								
Register Availability	<table><thead><tr><th>Status</th><th>Availability</th></tr></thead><tbody><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></tbody></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><thead><tr><th>Status</th><th>Default Value</th></tr></thead><tbody><tr><td>Power On Sequence</td><td>Sleep In Mode</td></tr><tr><td>S/W Reset</td><td>Sleep In Mode</td></tr><tr><td>H/W Reset</td><td>Sleep In Mode</td></tr></tbody></table>													Status	Default Value	Power On Sequence	Sleep In Mode	S/W Reset	Sleep In Mode	H/W Reset	Sleep In Mode				
Status	Default Value																								
Power On Sequence	Sleep In Mode																								
S/W Reset	Sleep In Mode																								
H/W Reset	Sleep In Mode																								
Flow Chart	<div><div><div>SPLPOUT (11h)</div><div>Start Internal Oscillator</div><div>Start up DC-DC Converter</div><div>Charge Offset voltage for LCD Panel</div></div><div><div>Display whole blank screen for 2 frames (Automatic No effect to DISP ON/OFF Commands)</div><div>Display Memory contents in accordance with the current command table settings</div><div>Sleep Out Mode</div></div><div><div>Legend</div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>																								

4.2.17. Partial Mode On (12h)

12h	PTLON (Partial Mode On)																								
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	0	0	0	1	0	0	1	0	12h												
Parameter	No parameter																								
Description	This command turns on the Partial Mode. The Partial Mode window is described in the Partial Area command (30H). To leave the Partial Mode, the Normal Display Mode On command (13H) should be written.																								
Restriction	This command has no effect when the Partial Display Mode is already active.																								
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Normal Display Mode</td></tr><tr><td>S/W Reset</td><td>Normal Display Mode</td></tr><tr><td>H/W Reset</td><td>Normal Display Mode</td></tr></table>													Status	Default Value	Power On Sequence	Normal Display Mode	S/W Reset	Normal Display Mode	H/W Reset	Normal Display Mode				
Status	Default Value																								
Power On Sequence	Normal Display Mode																								
S/W Reset	Normal Display Mode																								
H/W Reset	Normal Display Mode																								
Flow Chart	See Partial Area (30h)																								

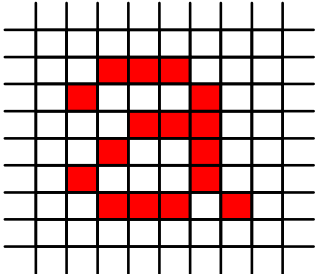
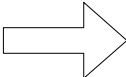
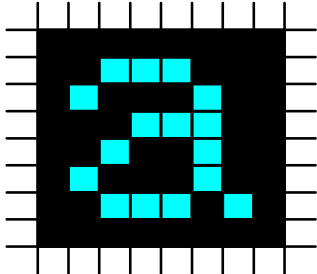
4.2.18. Normal Display Mode On (13h)

13h	NORON (Normal Display Mode On)																								
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	0	0	0	1	0	0	1	1	13h												
Parameter	No parameter																								
Description	This command returns the display to the Normal Display Mode. Normal Display Mode On means Partial Mode Off and Scroll mode off. X = Void																								
Restriction	This command has no effect when the Normal Display Mode is active.																								
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Normal Display Mode On</td></tr><tr><td>S/W Reset</td><td>Normal Display Mode On</td></tr><tr><td>H/W Reset</td><td>Normal Display Mode On</td></tr></table>													Status	Default Value	Power On Sequence	Normal Display Mode On	S/W Reset	Normal Display Mode On	H/W Reset	Normal Display Mode On				
Status	Default Value																								
Power On Sequence	Normal Display Mode On																								
S/W Reset	Normal Display Mode On																								
H/W Reset	Normal Display Mode On																								
Flow Chart	See Partial Area Descriptions for details of when to use this command.																								

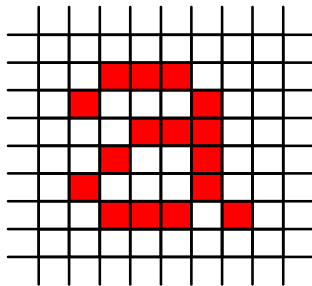
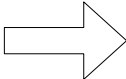
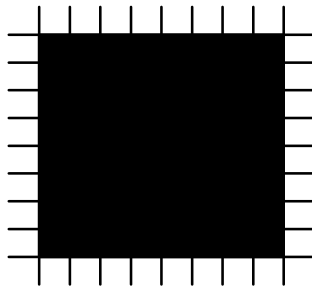
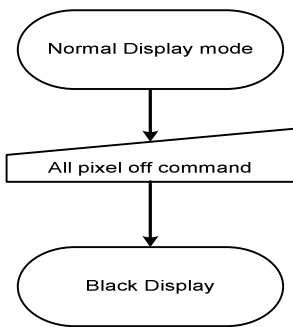
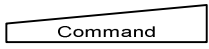
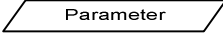

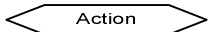

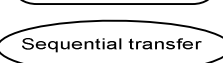
4.2.19. Display Inversion Off (20h)

20h	INVOFF (Display Inversion Off)																								
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	0	0	1	0	0	0	0	0	20h												
Parameter	No parameter																								
Description	<p>This command is used to recover from the Display Inversion On mode.</p> <p>This command makes no change of the content of Frame Memory.</p> <p>This command does not change any other status.</p> <div><div><p>Memory</p><p>X = Void</p></div><div><p>Display Panel</p></div></div> <p>X = Void</p>																								
Restriction	This command has no effect when the module is already in the Display Inversion Off mode.																								
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Display Inversion Off</td></tr><tr><td>S/W Reset</td><td>Display Inversion Off</td></tr><tr><td>H/W Reset</td><td>Display Inversion Off</td></tr></table>													Status	Default Value	Power On Sequence	Display Inversion Off	S/W Reset	Display Inversion Off	H/W Reset	Display Inversion Off				
Status	Default Value																								
Power On Sequence	Display Inversion Off																								
S/W Reset	Display Inversion Off																								
H/W Reset	Display Inversion Off																								
Flow Chart	<div><div><p>Display Inversion On Mode</p><p>↓</p><p>INVOFF(20h)</p><p>↓</p><p>Display Inversion Off Mode</p></div><div><p>Legend</p><ul style="list-style-type: none">CommandParameterDisplayActionModeSequential transfer</div></div>																								

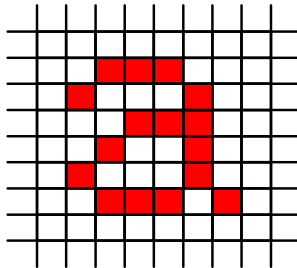
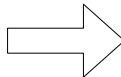
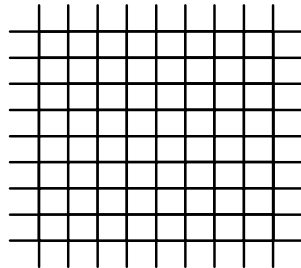
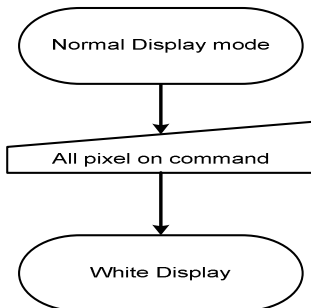
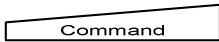





4.2.20. fDisplay Inversion On (21h)

21h	INVON (Display Inversion ON)																								
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	0	0	1	0	0	0	0	1	21h												
Parameter	No parameter																								
Description	<p>This command is used to enter the Display Inversion On mode.</p> <p>This command makes no change of the content of the Frame Memory. Every bit is inverted from the Frame Memory to the display.</p> <p>This command does not change any other status.</p> <p>To exit the Display Inversion On mode, the Display Inversion Off command (20h) should be written.</p> <div><div><p>Memory</p></div><div></div><div><p>Display Panel</p></div></div> <p>X = Void</p>																								
	Restriction	This command has no effect when the ILI9806G is already in the Inversion On mode.																							
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Display Inversion Off</td></tr><tr><td>S/W Reset</td><td>Display Inversion Off</td></tr><tr><td>H/W Reset</td><td>Display Inversion Off</td></tr></table>													Status	Default Value	Power On Sequence	Display Inversion Off	S/W Reset	Display Inversion Off	H/W Reset	Display Inversion Off				
Status	Default Value																								
Power On Sequence	Display Inversion Off																								
S/W Reset	Display Inversion Off																								
H/W Reset	Display Inversion Off																								
Flow Chart	<div><div><p>Display Inversion Off Mode</p><p>↓</p><p>INVON(21h)</p><p>↓</p><p>Display Inversion On Mode</p></div><div><p>Legend</p><ul style="list-style-type: none">CommandParameterDisplayActionModeSequential transfer</div></div>																								

4.2.21. All Pixel Off (22h)

22h	INVON (Display Inversion ON)																								
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	0	0	1	0	0	0	1	0	22h												
Parameter	No parameter																								
Description	<p>This command turns the display panel black in the Sleep Out mode and the status of the Display On/Off register can be ON or OFF. This command makes no change to the contents of the Frame Memory. This command does not change any other status.</p> <div><div><p>Memory</p></div><div></div><div><p>Display Panel</p></div></div> <p>To exit this mode, All Pixels On, Normal Display Mode On, or Partial Mode On commands can be used. The display panel shows the content of the Frame Memory after Normal Display Mode On and Partial Mode On commands.</p>																								
Restriction	This command has no effect when the ILI9806G is already in the Display Inversion On mode.																								
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>OFF</td></tr><tr><td>S/W Reset</td><td>OFF</td></tr><tr><td>H/W Reset</td><td>OFF</td></tr></table>													Status	Default Value	Power On Sequence	OFF	S/W Reset	OFF	H/W Reset	OFF				
Status	Default Value																								
Power On Sequence	OFF																								
S/W Reset	OFF																								
H/W Reset	OFF																								
Flow Chart	<div><div><pre>graph TD; A([Normal Display mode]) --> B[/All pixel off command/]; B --> C([Black Display]);</pre></div><div><p>Legend</p><ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer</div></div>																								

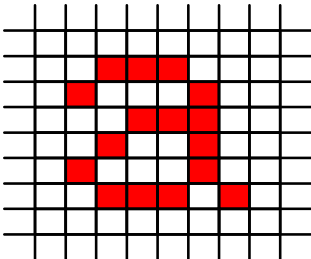
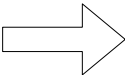
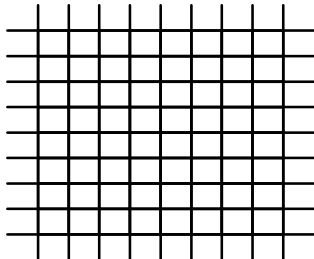
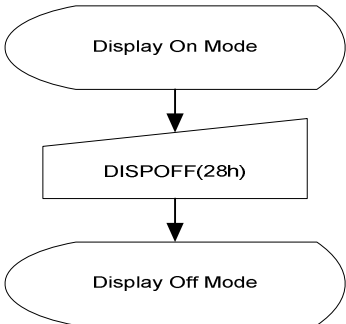
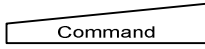
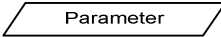

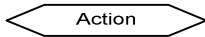
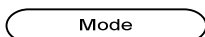

4.2.22. All Pixel On (23h)

23h	INVON (Display Inversion ON)																								
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	0	0	1	0	0	0	1	1	23h												
Parameter	No parameter																								
Description	<p>This command turns the display panel white in the Sleep Out mode and the status of the Display On/Off register can be ON or OFF. This command makes no change of contents of the Frame Memory. This command does not change any other status.</p> <div><div><p>Memory</p></div><div></div><div><p>Display Panel</p></div></div> <p>To exit this mode, All Pixels Off, Normal Display Mode On or Partial Mode On commands can be used. The display shows the content of the Frame Memory after Normal Display Mode On and Partial Mode On commands.</p>																								
Restriction	This command has no effect when the ILI9806G is already in the Inversion on mode.																								
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>OFF</td></tr><tr><td>S/W Reset</td><td>OFF</td></tr><tr><td>H/W Reset</td><td>OFF</td></tr></table>													Status	Default Value	Power On Sequence	OFF	S/W Reset	OFF	H/W Reset	OFF				
Status	Default Value																								
Power On Sequence	OFF																								
S/W Reset	OFF																								
H/W Reset	OFF																								
Flow Chart	<div><div><pre>graph TD A([Normal Display mode]) --> B[/All pixel on command/] B --> C([White Display])</pre></div><div><p>Legend</p><ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer</div></div>																								

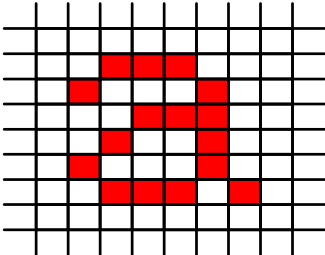
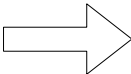
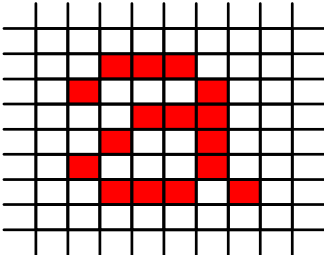
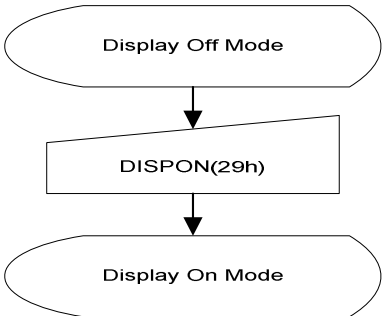
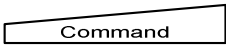
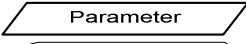
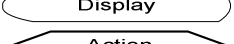
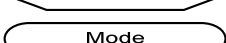
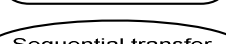
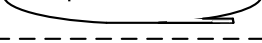
4.2.23. Gamma Set (26h)

26h	GAMSET (Gamma Set)																								
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	0	0	1	0	0	1	1	0	26h												
Parameter	1	1	↑	XX	GC [7:0]								01												
Description	This command is used to select the desired Gamma curve for the current display. A maximum of 4 fixed Gamma curves can be selected. The curve is selected by setting the appropriate bit in the parameter as described in the Table below:																								
	GC [7:0]		Parameter				Curve Selected																		
	01h		GC0				Gamma curve 1 (G2.2)																		
	02h		GC1				Gamma curve 2 (G1.8)																		
	04h		GC2				Gamma curve 3 (G2.5)																		
	08h		GC3				Gamma curve 4 (G1)																		
	Note: All others value are undefined.																								
	X = Void																								
Restriction	Values of GC [7:0] not shown in the table above are invalid and will not change the current selected Gamma curve until a valid value is received.																								
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>8'h01h</td></tr><tr><td>S/W Reset</td><td>8'h01h</td></tr><tr><td>H/W Reset</td><td>8'h01h</td></tr></table>													Status	Default Value	Power On Sequence	8'h01h	S/W Reset	8'h01h	H/W Reset	8'h01h				
Status	Default Value																								
Power On Sequence	8'h01h																								
S/W Reset	8'h01h																								
H/W Reset	8'h01h																								
Flow Chart	<div><div><div>GAMSET (26h)</div><div>↓</div><div>1st Parameter: GC [7:0]</div><div>↓</div><div>New Gamma Curve Loaded</div></div><div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div></div>																								

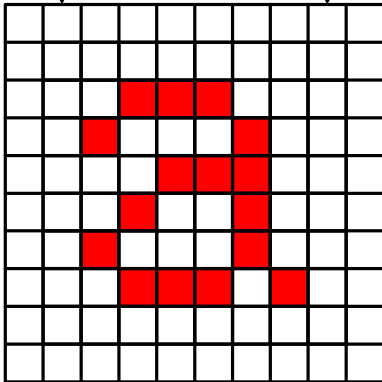
4.2.24. Display Off (28h)

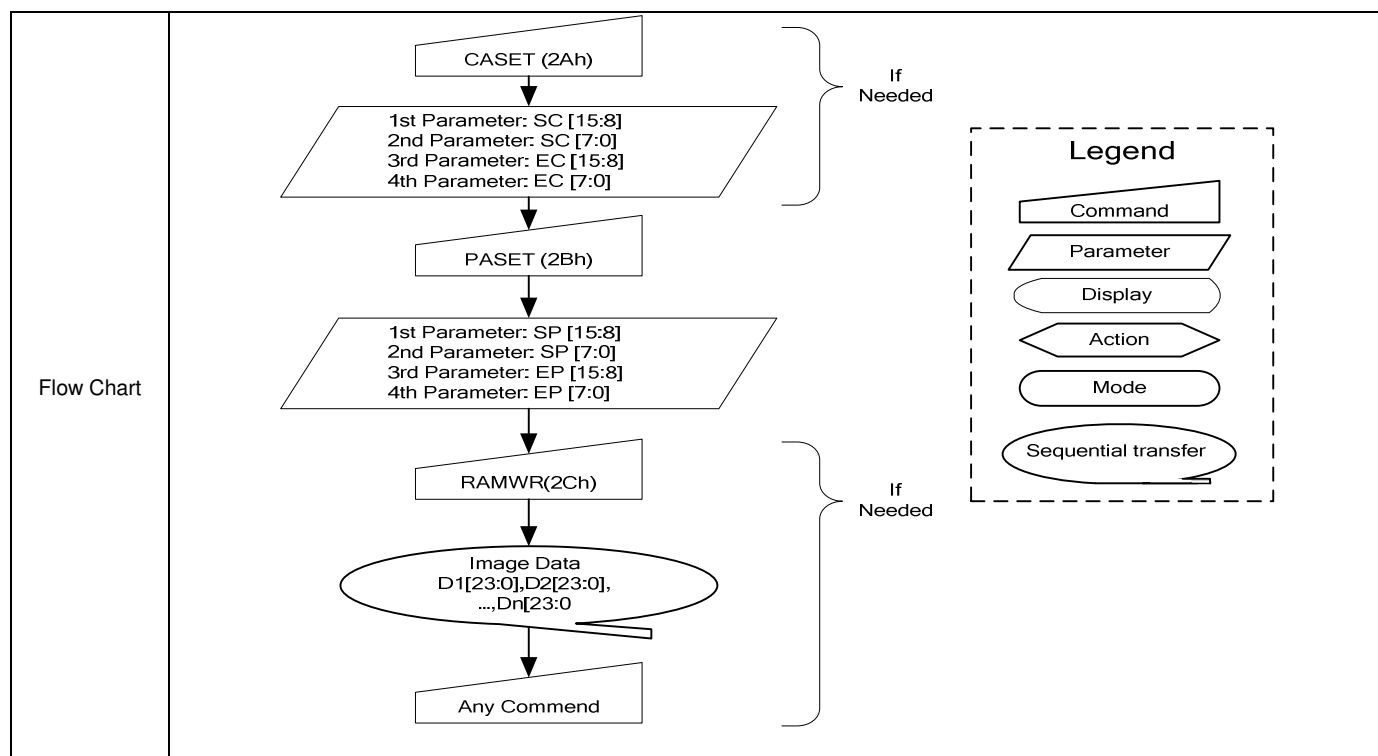
28h	DISOFF (Display Off)																								
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	0	0	1	0	1	0	0	0	28h												
Parameter	No parameter																								
Description	<p>This command is used to enter the Display Off mode. In this mode, the output from the Frame Memory is disabled and a blank page inserted.</p> <p>This command makes no change of contents of the Frame Memory and does not change any other status.</p> <p>There will be no abnormal visible effect on the display.</p> <div><div><p>Memory</p></div><div></div><div><p>Display Panel</p></div></div> <p>X = Void</p>																								
Restriction	This command has no effect when the module is already in the Display Off mode.																								
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Display Off</td></tr><tr><td>S/W Reset</td><td>Display Off</td></tr><tr><td>H/W Reset</td><td>Display Off</td></tr></table>													Status	Default Value	Power On Sequence	Display Off	S/W Reset	Display Off	H/W Reset	Display Off				
Status	Default Value																								
Power On Sequence	Display Off																								
S/W Reset	Display Off																								
H/W Reset	Display Off																								
Flow Chart	<div><div><pre>graph TD; A([Display On Mode]) --> B[/DISPOFF(28h)/]; B --> C([Display Off Mode]);</pre></div><div><p>Legend</p><ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer</div></div>																								

4.2.25. Display ON (29h)

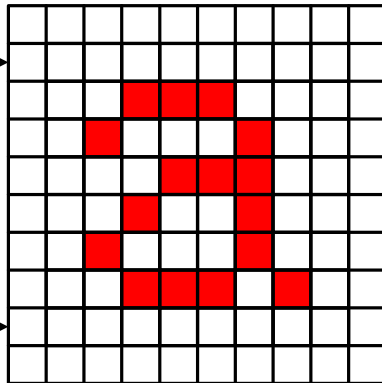
29h	DISON (Display ON)																								
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	0	0	1	0	1	0	0	1	29h												
Parameter	No parameter																								
Description	<p>This command is used to recover from the Display Off mode. Output from the Frame Memory is enabled.</p> <p>This command makes no change to the contents of the Frame Memory.</p> <p>This command does not change any other status.</p> <div><div><p>Memory</p></div><div></div><div><p>Display Panel</p></div></div> <p>X = Void</p>																								
Restriction	This command has no effect when the ILI9806G is already in the Display On mode.																								
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Display Off</td></tr><tr><td>S/W Reset</td><td>Display Off</td></tr><tr><td>H/W Reset</td><td>Display Off</td></tr></table>													Status	Default Value	Power On Sequence	Display Off	S/W Reset	Display Off	H/W Reset	Display Off				
Status	Default Value																								
Power On Sequence	Display Off																								
S/W Reset	Display Off																								
H/W Reset	Display Off																								
Flow Chart	<div><div></div><div><p>Legend</p><div><p>Command</p></div><div><p>Parameter</p></div><div><p>Display</p></div><div><p>Action</p></div><div><p>Mode</p></div><div><p>Sequential transfer</p></div></div></div>																								

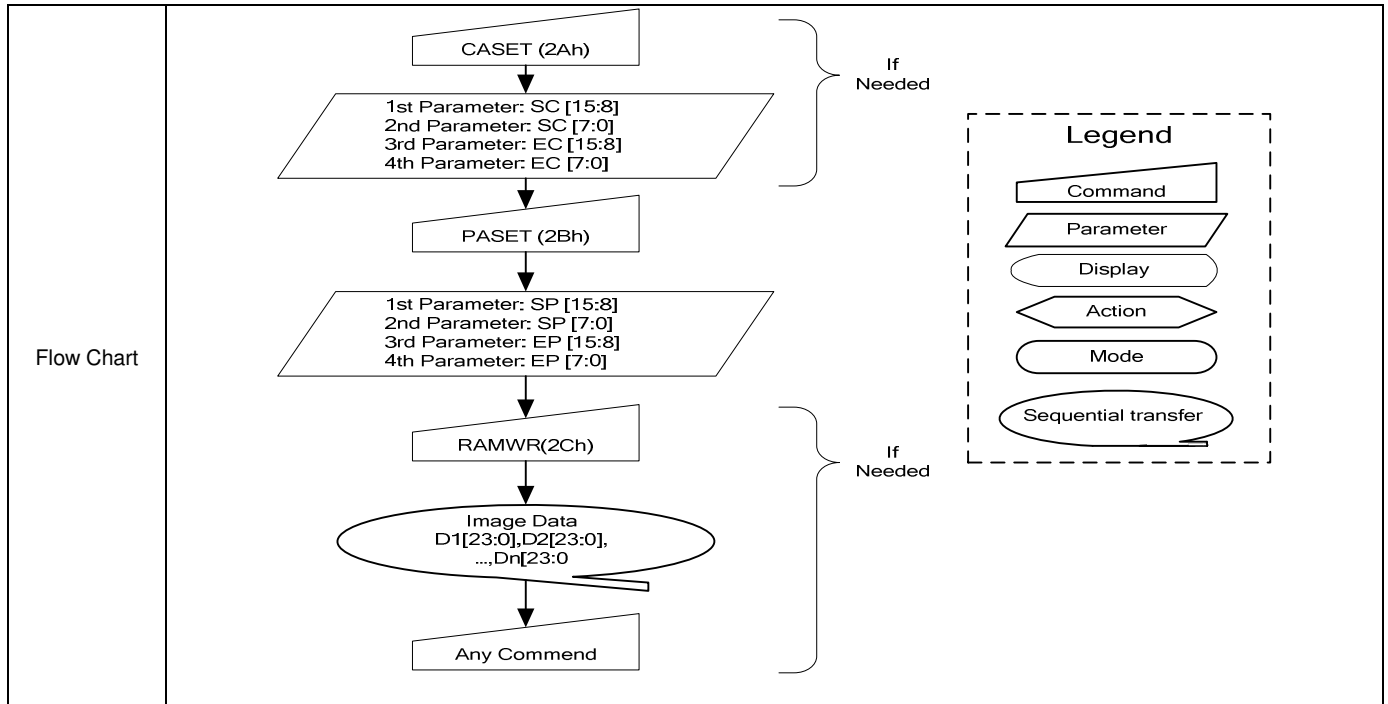
4.2.26. Column Address Set (2Ah)

2Ah	CASET (Column Address Set)																																
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX																				
Command	0	1	↑	XX	0	0	1	0	1	0	1	0	2Ah																				
1 st Parameter	1	1	↑	XX	SC [15:8]								XX																				
2 nd Parameter	1	1	↑	XX	SC [7:0]								XX																				
3 rd Parameter	1	1	↑	XX	EC [15:8]								XX																				
4 th Parameter	1	1	↑	XX	EC [7:0]								XX																				
Description	This command is used to define the area of the frame memory the MPU can access. This command makes no change on the other status of the driver. When the RAMWR command is applied, the values of SC [15:0] and EC [15:0] are referred. Each value represents one column line in the Frame Memory.																																
	<div><div>SC[15:0]</div><div>EC[15:0]</div></div>																																
Restriction	SC [15:0] must always be equal to or less than EC [15:0]. For example (480 (RGB) x 864 Resolution): When SC [15:0] or EC [15:0] is greater than 01DFh (when MADCTL's D5 = 0) or 035Fh (when MADCTL's D5 = 1), data out of range will be ignored.																																
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes								
Status	Availability																																
Normal Mode On, Idle Mode Off, Sleep Out	Yes																																
Normal Mode On, Idle Mode On, Sleep Out	Yes																																
Partial Mode On, Idle Mode Off, Sleep Out	Yes																																
Partial Mode On, Idle Mode On, Sleep Out	Yes																																
Sleep In	Yes																																
Default	<table><tr><th>RSO [2:0]</th><th>Resolution</th><th>SC [15:0]</th><th>EC [15:0]</th></tr><tr><td>000</td><td>480 (RGB) x 864</td><td>0 x 0000h</td><td>0 x 01DFh</td></tr><tr><td>001</td><td>480 (RGB) x 854</td><td>0 x 0000h</td><td>0 x 01DFh</td></tr><tr><td>010</td><td>480 (RGB) x 800</td><td>0 x 0000h</td><td>0 x 01DFh</td></tr><tr><td>011</td><td>480 (RGB) x 640</td><td>0 x 0000h</td><td>0 x 01DFh</td></tr></table>													RSO [2:0]	Resolution	SC [15:0]	EC [15:0]	000	480 (RGB) x 864	0 x 0000h	0 x 01DFh	001	480 (RGB) x 854	0 x 0000h	0 x 01DFh	010	480 (RGB) x 800	0 x 0000h	0 x 01DFh	011	480 (RGB) x 640	0 x 0000h	0 x 01DFh
RSO [2:0]	Resolution	SC [15:0]	EC [15:0]																														
000	480 (RGB) x 864	0 x 0000h	0 x 01DFh																														
001	480 (RGB) x 854	0 x 0000h	0 x 01DFh																														
010	480 (RGB) x 800	0 x 0000h	0 x 01DFh																														
011	480 (RGB) x 640	0 x 0000h	0 x 01DFh																														



4.2.27. Page Address Set (2Bh)

2Bh	PASET (Page Address Set)																																
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX																				
Command	0	1	↑	XX	0	0	1	0	1	0	1	1	2Bh																				
1 st Parameter	1	1	↑	XX	SP [15:8]								XX																				
2 nd Parameter	1	1	↑	XX	SP [7:0]								XX																				
3 rd Parameter	1	1	↑	XX	EP [15:8]								XX																				
4 th Parameter	1	1	↑	XX	EP [7:0]								XX																				
Description	<p>This command is used to define the area of the frame memory the MPU can access. This command makes no change on the other status of the driver. The values of SP [15:0] and EP [15:0] are referred when RAMWR command is applied. Each value represents one Page line in the Frame Memory.</p> <div><div>SP[15:0] →</div><div>EP[15:0] →</div></div> <p>X = void</p>																																
Restriction	<p>SP [15:0] must always be equal to or less than EP [15:0]. For example (480 (RGB) x 864 Resolution):</p> <p>When SP [15:0] or EP [15:0] is greater than 035Fh (when MADCTL's D5 = 0) or 01DFh (when MADCTL's D5 = 1), data out of range will be ignored.</p>																																
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes								
Status	Availability																																
Normal Mode On, Idle Mode Off, Sleep Out	Yes																																
Normal Mode On, Idle Mode On, Sleep Out	Yes																																
Partial Mode On, Idle Mode Off, Sleep Out	Yes																																
Partial Mode On, Idle Mode On, Sleep Out	Yes																																
Sleep In	Yes																																
Default	<table><tr><th>RSO [2:0]</th><th>Resolution</th><th>SP [15:0]</th><th>EP [15:0]</th></tr><tr><td>000</td><td>480 (RGB) x 864</td><td>0 x 0000h</td><td>0 x 035Fh</td></tr><tr><td>001</td><td>480 (RGB) x 854</td><td>0 x 0000h</td><td>0 x 0355h</td></tr><tr><td>010</td><td>480 (RGB) x 800</td><td>0 x 0000h</td><td>0 x 031Fh</td></tr><tr><td>011</td><td>480 (RGB) x 640</td><td>0 x 0000h</td><td>0 x 027Fh</td></tr></table>													RSO [2:0]	Resolution	SP [15:0]	EP [15:0]	000	480 (RGB) x 864	0 x 0000h	0 x 035Fh	001	480 (RGB) x 854	0 x 0000h	0 x 0355h	010	480 (RGB) x 800	0 x 0000h	0 x 031Fh	011	480 (RGB) x 640	0 x 0000h	0 x 027Fh
RSO [2:0]	Resolution	SP [15:0]	EP [15:0]																														
000	480 (RGB) x 864	0 x 0000h	0 x 035Fh																														
001	480 (RGB) x 854	0 x 0000h	0 x 0355h																														
010	480 (RGB) x 800	0 x 0000h	0 x 031Fh																														
011	480 (RGB) x 640	0 x 0000h	0 x 027Fh																														



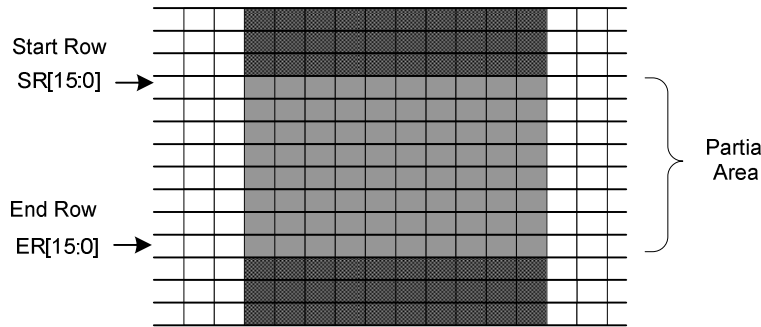
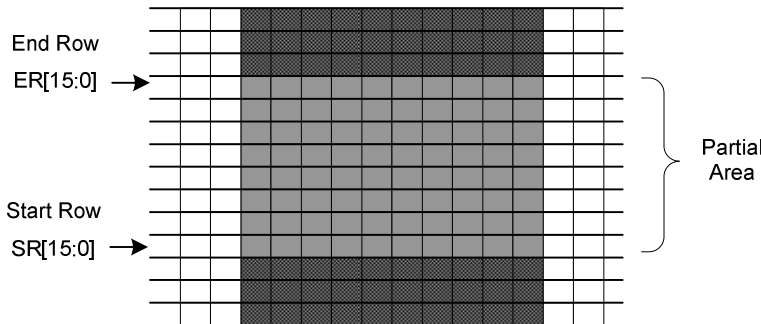
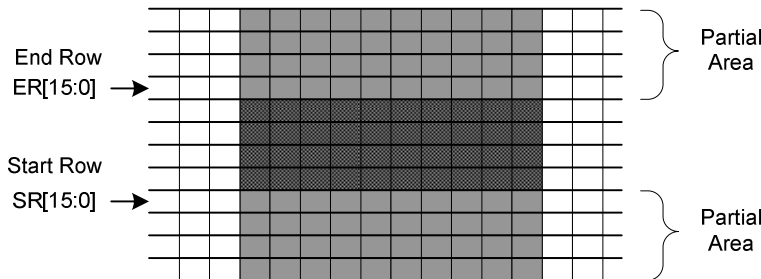
4.2.28. Memory Write (2Ch)

2Ch	RAMWR (Memory Write)																								
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	0	0	1	0	1	1	0	0	2Ch												
1 st Parameter	1	1	↑	D1 [23:0]									XX												
:	1	1	↑	Dx [23:0]									XX												
N th Parameter	1	1	↑	Dn [23:0]									XX												
Description	<p>This command transfers data from the MPU to the Frame Memory. This command makes no change to the other status of the driver. When this command is accepted, the column register and the page register are reset to the Start Column (SC) and the Start Page (SP) positions. The Start Column and Start Page positions are different in accordance with the MADCTL setting. Then D [23:0] is stored in the Frame Memory, and the column register and the page register are incremented at the same time. Sending any other commands can stop the frame Write.</p> <p>X = void.</p>																								
Restriction	There is no restriction on the length of parameters.																								
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Contents of memory is set randomly</td></tr><tr><td>S/W Reset</td><td>Contents of memory is set randomly</td></tr><tr><td>H/W Reset</td><td>Contents of memory is set randomly</td></tr></table>													Status	Default Value	Power On Sequence	Contents of memory is set randomly	S/W Reset	Contents of memory is set randomly	H/W Reset	Contents of memory is set randomly				
Status	Default Value																								
Power On Sequence	Contents of memory is set randomly																								
S/W Reset	Contents of memory is set randomly																								
H/W Reset	Contents of memory is set randomly																								
Flow Chart	<div><div><div>RAMWR(2Ch)</div><div>↓</div><div>Image Data D1[23:0],D2[23:0], ...,Dn[23:0]</div><div>↓</div><div>Any Command</div></div><div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div></div>																								

4.2.29. Memory Read (2Eh)

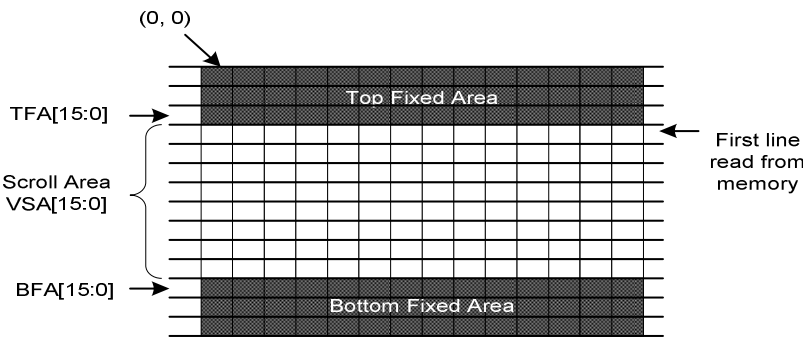

2Eh	RAMRD (Memory Read)																								
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	0	0	1	0	1	1	1	0	2Eh												
1 st Parameter	1	1	↑	XX	X	X	X	X	X	X	X	X	XX												
2 nd Parameter	1	1	↑	D1 [23:0]									XX												
:	1	1	↑	Dx [23:0]									XX												
(N+1) th Parameter	1	1	↑	Dn [23:0]									XX												
Description	<p>The command transfers image data from the Frame Memory to the MPU. This command makes no change to the other status of the driver. When this command is accepted, the column register and the page register are reset to the Start Column (SC) and the Start Page (SP) positions.</p> <p>The Start Column and Start Page positions are different in accordance with the MADCTL setting.</p> <p>Then D [23:0] is read back from the Frame Memory, and the column register and the page register are incremented at the same time. Sending any other command can stop the frame read.</p> <p>X = void</p>																								
Restriction	There is no restriction on the length of parameters.																								
Register Availability	<table><thead><tr><th>Status</th><th>Availability</th></tr></thead><tbody><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></tbody></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><thead><tr><th>Status</th><th>Default Value</th></tr></thead><tbody><tr><td>Power On Sequence</td><td>Contents of memory is set randomly</td></tr><tr><td>S/W Reset</td><td>Contents of memory is set randomly</td></tr><tr><td>H/W Reset</td><td>Contents of memory is set randomly</td></tr></tbody></table>													Status	Default Value	Power On Sequence	Contents of memory is set randomly	S/W Reset	Contents of memory is set randomly	H/W Reset	Contents of memory is set randomly				
Status	Default Value																								
Power On Sequence	Contents of memory is set randomly																								
S/W Reset	Contents of memory is set randomly																								
H/W Reset	Contents of memory is set randomly																								
Flow Chart	<div><div><div>RAMRD(2Eh)</div><div>Dummy</div><div>Image Data D1[23:0],D2[23:0], ...,Dn[23:0]</div><div>Any Commend</div></div><div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div></div>																								

4.2.30. Partial Area (30h)

30h	PLTAR (Partial Area)												
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	0	0	0	0	30h
1 st Parameter	1	1	↑	XX	SR [15:8]								XX
2 nd Parameter	1	1	↑	XX	SR [7:0]								XX
3 rd Parameter	1	1	↑	XX	ER [15:8]								XX
4 th Parameter	1	1	↑	XX	ER [7:0]								XX
Description	<p>This command defines the module's partial display area. There are two parameters associated with this command. The first defines the Start Row (SR) and the second the End Row (ER), as illustrated in the following figure. SR and ER refer to the Frame Memory line pointer.</p> <p>If End Row > Start Row when MADCTL D4 = 0.</p> 												
	<p>If End Row > Start Row when MADCTL D4 = 1.</p> 												
	<p>If End Row < Start Row when MADCTL D4 = 0.</p> 												
	<p>If End Row = Start Row, then the Partial Area will be one row deep.</p> <p>X = void</p>												
Restriction	SR [15..0] and ER [15..0] cannot be greater than the horizontal line number.												

<p>Register Availability</p>	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
<p>Default</p>													
<p>Flow Chart</p>	<p>1. To Enter the Partial Mode</p> <p>2. To Leave the Partial Mode</p> <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 												

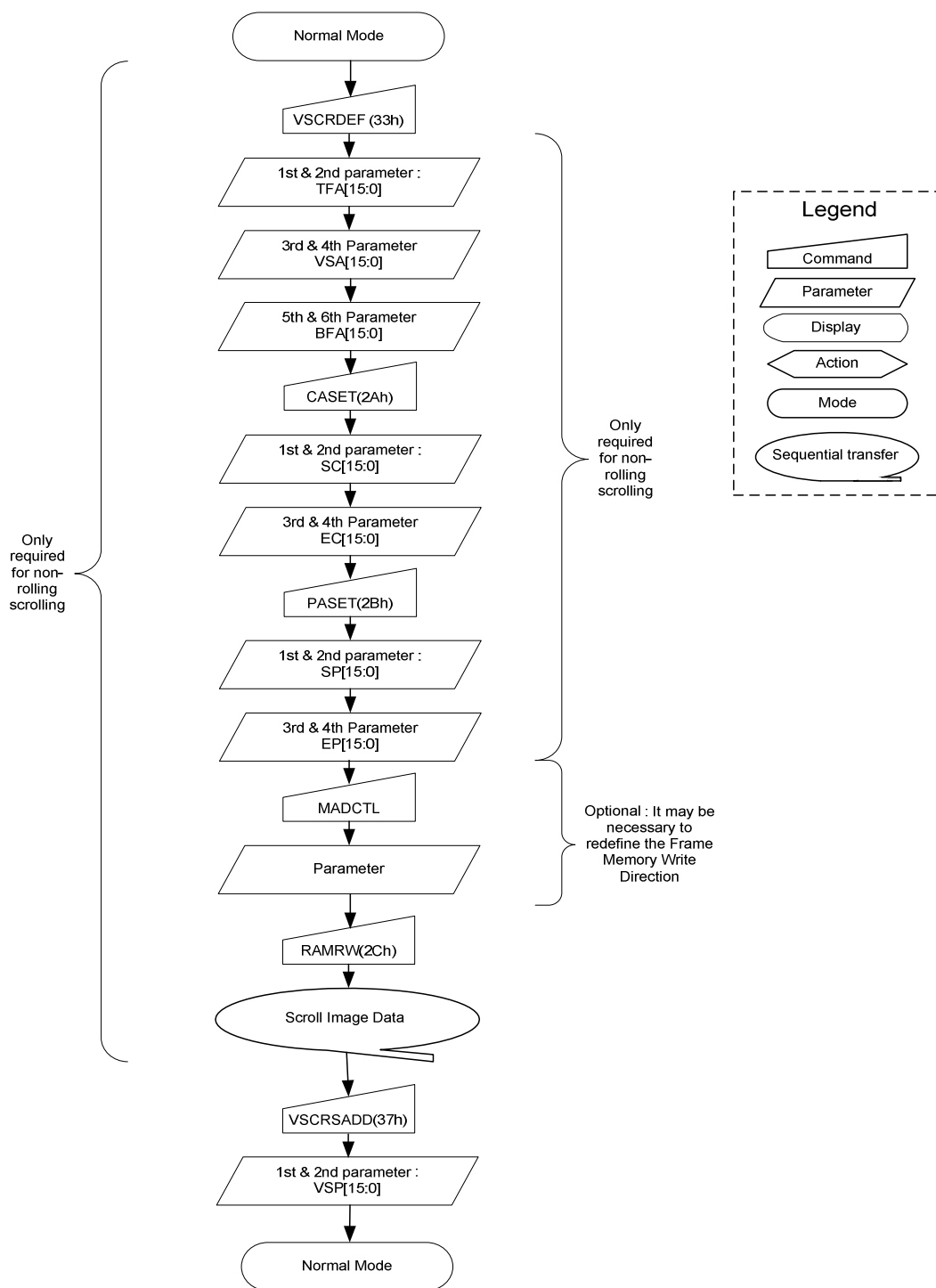
4.2.31. Vertical Scrolling Definition (33h)

33h	VSCRDEF (Vertical Scrolling Definition)												
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	0	0	1	1	33h
1 st Parameter	1	1	↑	XX	TFA [15:8]								XX
2 nd Parameter	1	1	↑	XX	TFA [7:0]								XX
3 rd Parameter	1	1	↑	XX	VSA [15:8]								XX
4 th Parameter	1	1	↑	XX	VSA [7:0]								XX
5 th Parameter	1	1	↑	XX	BFA [15:8]								XX
6 th Parameter	1	1	↑	XX	BFA [7:0]								XX
Description	This command defines the display vertical scrolling area.												
	<p>Memory Access Control (36h) D4 = 0:</p> <p>The 1st & 2nd parameters, TFA [15:0], describe the Top Fixed Area in number of lines from the top of the Frame Memory. The top of the Frame Memory and top of the display device are aligned.</p> <p>The 3rd & 4th parameters, VSA [15:0], describe the height of the Vertical Scrolling Area in number of lines of the Frame Memory from the Vertical Scrolling Start Address. The first line of the Vertical Scrolling Area starts immediately after the bottom most line of the Top Fixed Area. The last line of the Vertical Scrolling Area ends immediately before the top most line of the Bottom Fixed Area.</p> <p>The 5th & 6th parameters, BFA [15:0], describe the Bottom Fixed Area in number of lines from the bottom of the Frame Memory. The bottom of the Frame Memory and bottom of the display device are aligned.</p> <p>TFA, VSA, and BFA refer to the Frame Memory Line Pointer.</p> 												
	<p>Memory Access Control (36h) D4 = 1:</p> <p>The 1st & 2nd parameters, TFA [15:0], describe the Top Fixed Area in number of lines from the bottom of the Frame Memory. The bottom of the Frame Memory and bottom of the display device are aligned.</p> <p>The 3rd & 4th parameters, VSA [15:0], describe the height of the Vertical Scrolling Area in number of lines of the Frame Memory from the Vertical Scrolling Start Address. The first line of the Vertical Scrolling Area starts immediately after the top most line of the Top Fixed Area. The last line of the Vertical Scrolling Area ends immediately before the bottom most line of the Bottom Fixed Area.</p> <p>The 5th & 6th parameters, BFA [15:0], describe the Bottom Fixed Area in number of lines from the top of the Frame Memory. The top of the Frame Memory and top of the display device are aligned.</p> <p>TFA, VSA and BFA refer to the Frame Memory Line Pointer.</p> 												

Restriction	The sum of TFA, VSA and BFA must equal the number of the display device's horizontal lines; otherwise, the Scrolling mode is undefined. In the Vertical Scroll mode, Memory Access Control (36h) D5 should be set to 0 – this only affects the Frame Memory write.																							
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>				Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes								
Status	Availability																							
Normal Mode On, Idle Mode Off, Sleep Out	Yes																							
Normal Mode On, Idle Mode On, Sleep Out	Yes																							
Partial Mode On, Idle Mode Off, Sleep Out	Yes																							
Partial Mode On, Idle Mode On, Sleep Out	Yes																							
Sleep In	Yes																							
Default	<table><tr><th>Resolution</th><th>TFA [15..0]</th><th>VSA [15..0]</th><th>BFA [15..0]</th></tr><tr><td>480 (RGB) x 864</td><td>0 x 0000h</td><td>0 x 0360h</td><td>0 x 0000h</td></tr><tr><td>480 (RGB) x 854</td><td>0 x 0000h</td><td>0 x 0356h</td><td>0 x 0000h</td></tr><tr><td>480 (RGB) x 800</td><td>0 x 0000h</td><td>0 x 0320h</td><td>0 x 0000h</td></tr><tr><td>480 (RGB) x 640</td><td>0 x 0000h</td><td>0 x 0280h</td><td>0 x 0000h</td></tr></table>				Resolution	TFA [15..0]	VSA [15..0]	BFA [15..0]	480 (RGB) x 864	0 x 0000h	0 x 0360h	0 x 0000h	480 (RGB) x 854	0 x 0000h	0 x 0356h	0 x 0000h	480 (RGB) x 800	0 x 0000h	0 x 0320h	0 x 0000h	480 (RGB) x 640	0 x 0000h	0 x 0280h	0 x 0000h
Resolution	TFA [15..0]	VSA [15..0]	BFA [15..0]																					
480 (RGB) x 864	0 x 0000h	0 x 0360h	0 x 0000h																					
480 (RGB) x 854	0 x 0000h	0 x 0356h	0 x 0000h																					
480 (RGB) x 800	0 x 0000h	0 x 0320h	0 x 0000h																					
480 (RGB) x 640	0 x 0000h	0 x 0280h	0 x 0000h																					

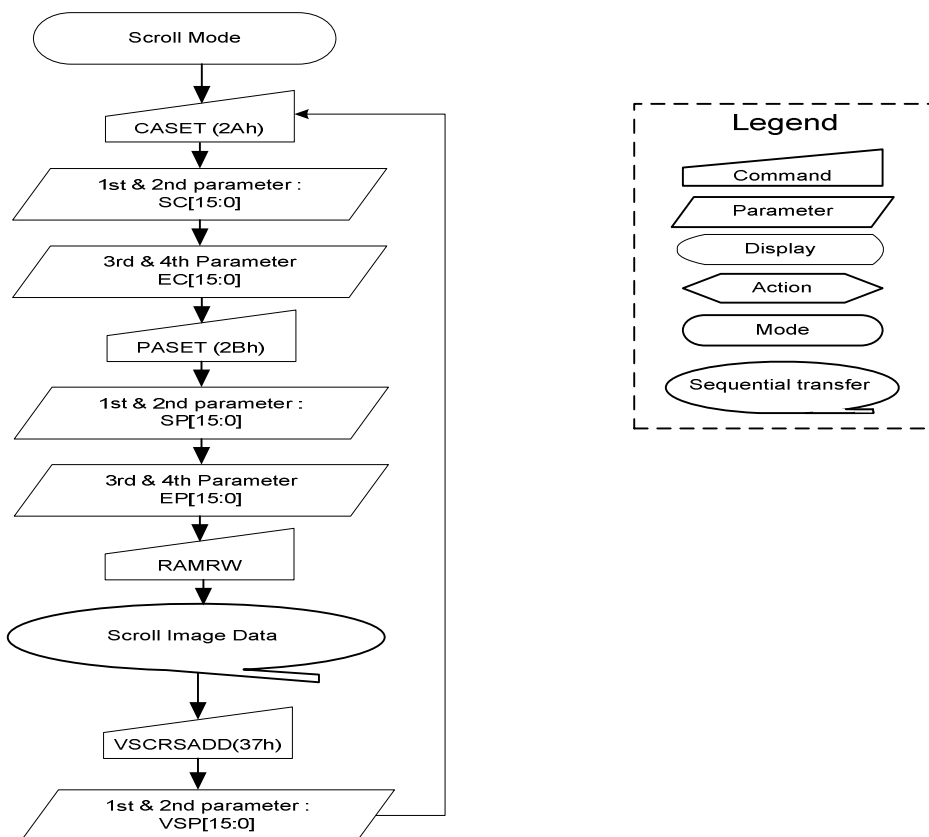
1. To enter the Vertical Scroll Mode:

Flow Chart

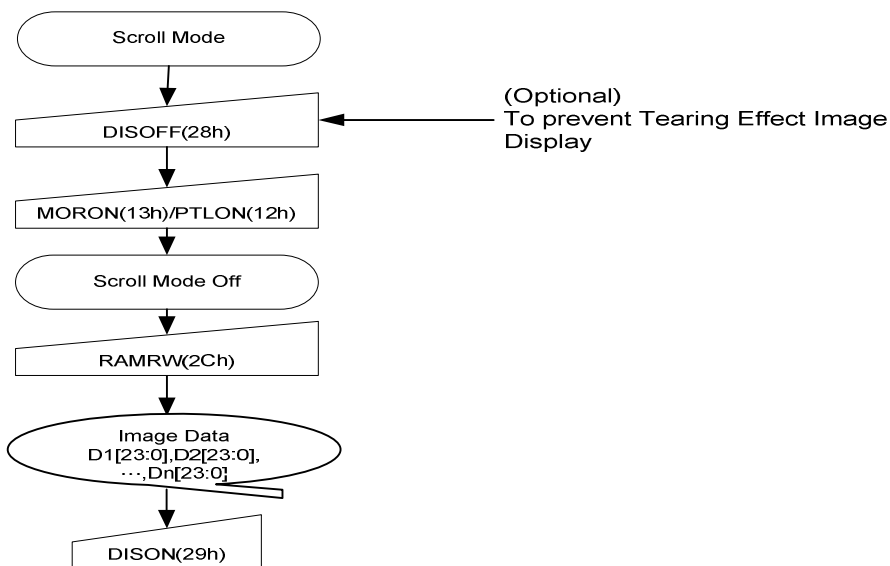


Since the value of the Vertical Scrolling Start Address is absolute with reference to the Frame Memory, it must not enter the fixed area; otherwise, an undesirable image may appear on the Display Panel.

2. Continuous Scroll :



3. To Leave Vertical Scroll Mode:

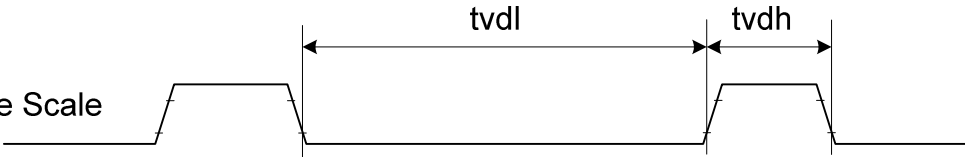
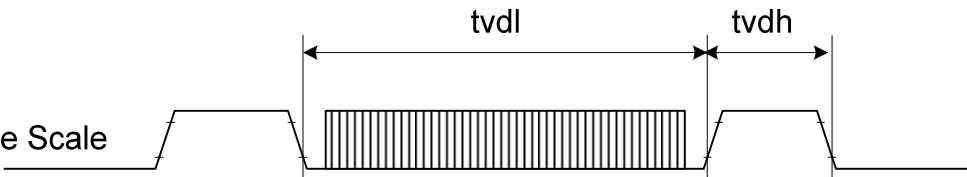


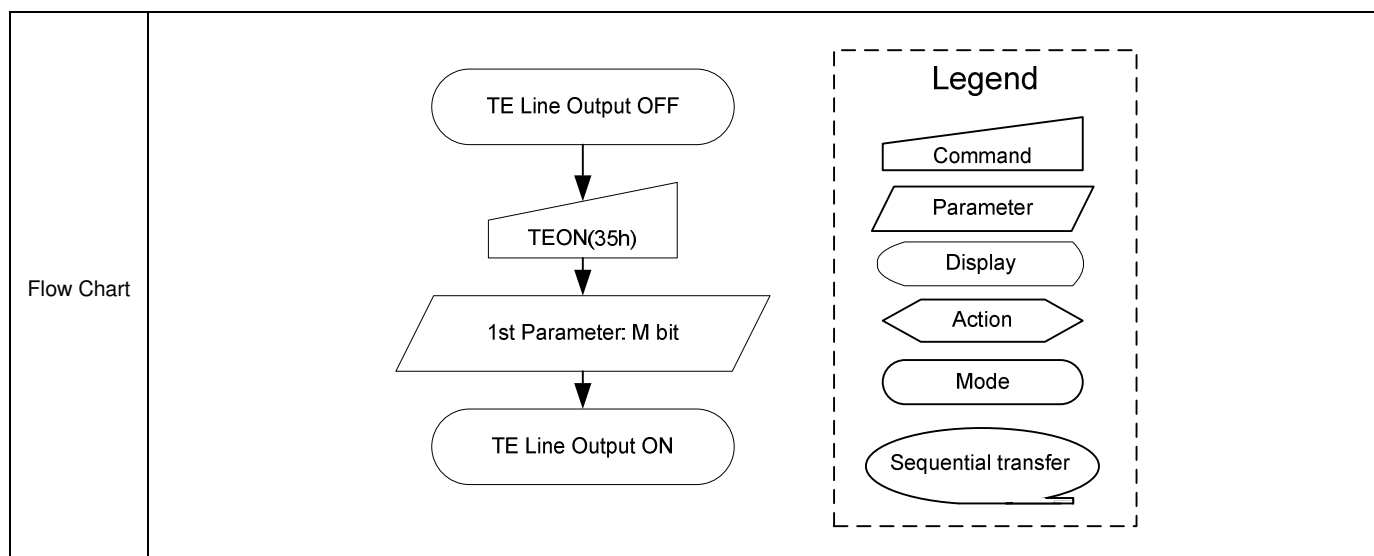
Note: To exit the Scroll Mode, both Normal Display Mode On (13h) and Partial Mode On (12h) commands can be used.

4.2.32. Tearing Effect Line OFF (34h)

34h	TEOFF (Tearing Effect Line OFF)																								
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	0	0	1	1	0	1	0	0	34h												
Parameter	No parameter																								
Description	This command is used to turn off the Display module's Tearing Effect output signal (Active Low) on the TE signal line.																								
Restriction	This command has no effect when the Tearing Effect output is already OFF.																								
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Off</td></tr><tr><td>S/W Reset</td><td>Off</td></tr><tr><td>H/W Reset</td><td>Off</td></tr></table>													Status	Default Value	Power On Sequence	Off	S/W Reset	Off	H/W Reset	Off				
Status	Default Value																								
Power On Sequence	Off																								
S/W Reset	Off																								
H/W Reset	Off																								
Flow Chart	<div><div><div>TE Line Output ON</div><div>↓</div><div>TEOFF(34h)</div><div>↓</div><div>TE Line Output OFF</div></div><div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div></div>																								

4.2.33. Tearing Effect Line ON (35h)

35h	TEON (Tearing Effect Line ON)																								
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	0	0	1	1	0	1	0	1	35h												
Parameter	1	1	↑	XX	X	X	X	X	X	X	X	M	XX												
Parameter	No parameter																								
Description	<p>This command is used to turn ON the Tearing Effect output signal on the TE signal line. Changing the MADCTL bit B4 will not affect this output. The Tearing Effect Line On has one parameter, which describes the mode of the Tearing Effect Output Line.</p> <p>When M = 0: The Tearing Effect Output line consists of V-Blanking information only:</p> <div><p>Vertical Time Scale</p></div> <p>When M = 1: The Tearing Effect Output Line consists of both V-Blanking and H-Blanking information:</p> <div><p>Vertical Time Scale</p></div> <p>Note: During the Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.</p> <p>X = void</p>																								
	Restriction	This command has no effect when the Tearing Effect output is already OFF.																							
	Register Availability	<table><thead><tr><th>Status</th><th>Availability</th></tr></thead><tbody><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></tbody></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In
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Normal Mode On, Idle Mode On, Sleep Out	Yes																								
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Default	<table><thead><tr><th>Status</th><th>Default Value</th></tr></thead><tbody><tr><td>Power On Sequence</td><td>Off</td></tr><tr><td>S/W Reset</td><td>Off</td></tr><tr><td>H/W Reset</td><td>Off</td></tr></tbody></table>													Status	Default Value	Power On Sequence	Off	S/W Reset	Off	H/W Reset	Off				
Status	Default Value																								
Power On Sequence	Off																								
S/W Reset	Off																								
H/W Reset	Off																								



4.2.34. Memory Access Control (36h)

36h	MADCTL (Memory Access Control)												
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	0	1	1	0	36h
Parameter	1	1	↑	XX	MY	MX	MV	ML	BGR	MH	SS	GS	XX

This command defines read/write scanning direction of the Frame Memory.

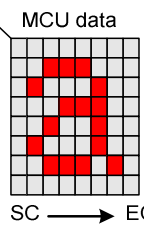
This command makes no change on the other status of the driver.

Bit	Symbol	Name	Description
D7	MY	Row Address Order	These 3 bits control the write/read direction from the MPU to memory
D6	MX	Column Address Order	
D5	MV	Row/Column Exchange	
D4	ML	Vertical Refresh Order	LCD vertical refresh direction control
D3	BGR	RGB-BGR Order	Color selector switch control (0 = RGB color filter panel, 1 = BGR color filter panel)
D2	MH	Horizontal Refresh Order	LCD horizontal refreshing direction control
D1	SS	Flip Horizontal(SS)	Select the Source driver scan direction on the panel module
D0	GS	Flip Vertical (GS)	Select the Gate driver scan direction on the panel module

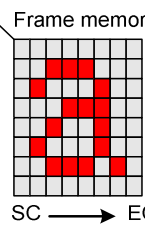
Top-Left (0,0) means the physical memory location

MY (Page Address Order)="0"

Top Left MCU data

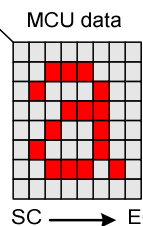


Top Left Frame memory

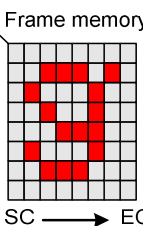


MY (Page Address Order)="1"

Top Left MCU data

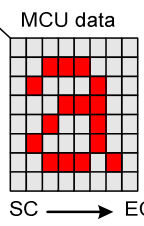


Top Left Frame memory

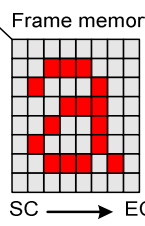


MX (Column Address Order)="0"

Top Left MCU data

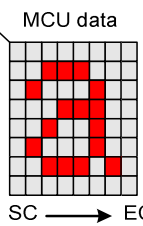


Top Left Frame memory

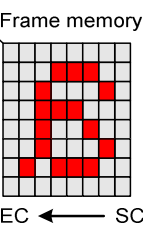


MX (Column Address Order)="1"

Top Left MCU data

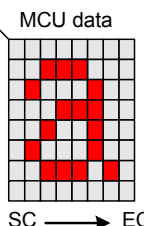


Top Left Frame memory

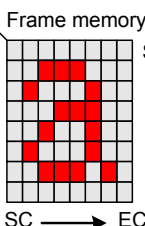


MV (Vertical Refresh Order bit)="0"

Top Left MCU data

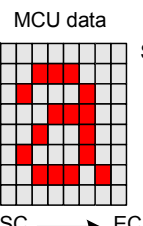


Top Left Frame memory

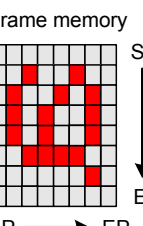


MV (Vertical Refresh Order bit)="1"

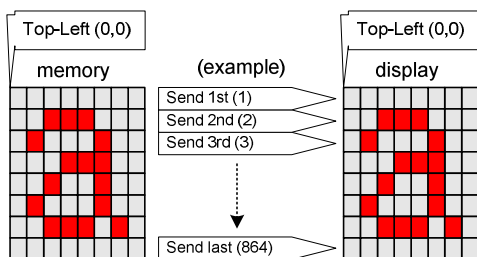
Top Left MCU data



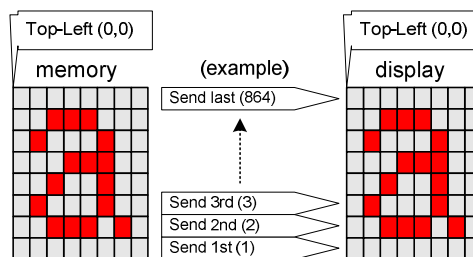
Top Left Frame memory



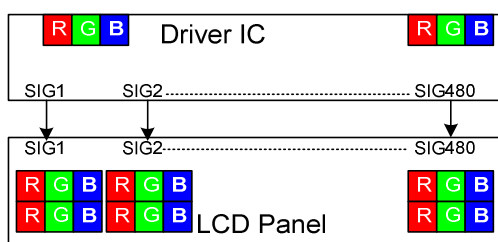
ML (Vertical refresh order bit)="0"



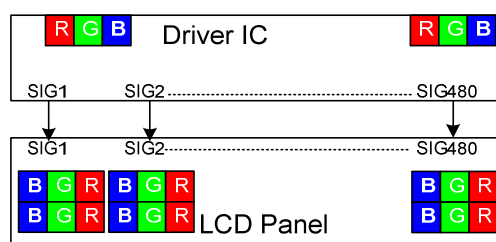
ML (Vertical refresh order bit)="1"



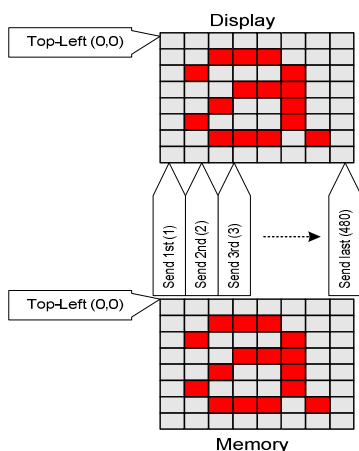
BGR (RGB-BGR Order control bit)="0"



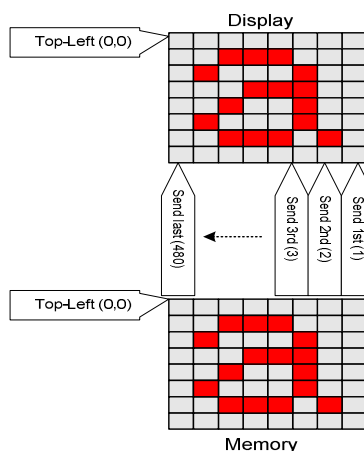
BGR (RGB-BGR Order control bit)="1"



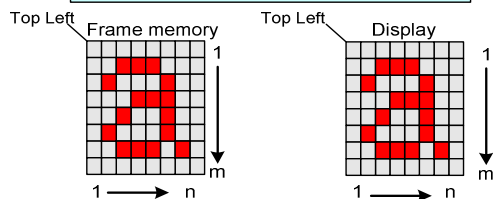
MH (Horizontal refresh order control bit)="0"



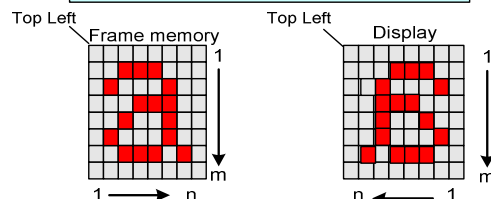
MH (Horizontal refresh order control bit)="1"



SS (Source Scan sequence)="0"



SS (Source Scan sequence)="1"



	<div style="display: flex; justify-content: space-around;"> <div style="text-align: center;"> <p>GS (Gate Scan sequence)="0"</p> </div> <div style="text-align: center;"> <p>GS (Gate Scan sequence)="1"</p> </div> </div>												
Restriction													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Sleep In	Yes												
Default	<table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>00h</td></tr> <tr> <td>S/W Reset</td><td>No change</td></tr> <tr> <td>H/W Reset</td><td>00h</td></tr> </tbody> </table>	Status	Default Value	Power On Sequence	00h	S/W Reset	No change	H/W Reset	00h				
Status	Default Value												
Power On Sequence	00h												
S/W Reset	No change												
H/W Reset	00h												
Flow Chart	<div style="display: flex; align-items: center; justify-content: center;"> <div style="text-align: center;"> <p>MADCTR(36h)</p> <p>↓</p> <p>1st Parameter D [7:0]</p> </div> <div style="margin-left: 20px;"> <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer </div> </div>												

4.2.35. Vertical Scrolling Start Address (37h)

37h	VSCRSADD (Vertical Scrolling Start Address)																																
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX																				
Command	0	1	↑	XX	0	0	1	1	0	1	1	1	37h																				
1 st Parameter	1	1	↑	XX	VSP [15:8]								XX																				
2 nd Parameter	1	1	↑	XX	VSP [7:0]								XX																				
Description	<p>This command is used together with the Vertical Scrolling Definition (33h). These two commands describe the scrolling area and the scrolling mode. The Vertical Scrolling Start Address command has one parameter which describes the address of the line in the Frame Memory that will be written as the first line after the last line of the Top Fixed Area on the display, as illustrated below.</p> <p>When MADCTL D4 = 0</p> <p>Example: When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 864 and VSP= 3</p> <div><div><p>(0, 0) →</p><p>Line Pointer VSP[15:0] →</p><p>(0, 863) →</p><p>Frame Memory</p></div><div><p>Pointer B4=0</p><table><tr><td>0</td></tr><tr><td>1</td></tr><tr><td>2</td></tr><tr><td>3</td></tr><tr><td>4</td></tr><tr><td>..</td></tr><tr><td>..</td></tr><tr><td>861</td></tr><tr><td>862</td></tr><tr><td>863</td></tr></table></div><div><p>Display</p></div></div> <p>When MADCTL D4=1</p> <p>Example: When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 864 and VSP= 3</p> <div><div><p>(0, 0) →</p><p>Line Pointer VSP[15:0] →</p><p>(0, 863) →</p><p>Frame Memory</p></div><div><p>Pointer B4=1</p><table><tr><td>863</td></tr><tr><td>862</td></tr><tr><td>861</td></tr><tr><td>..</td></tr><tr><td>..</td></tr><tr><td>4</td></tr><tr><td>3</td></tr><tr><td>2</td></tr><tr><td>1</td></tr><tr><td>0</td></tr></table></div><div><p>Display</p></div></div> <p>Note: When the new Pointer position and Picture Data are sent, the result on the display will appear at the next Panel Scan to avoid tearing effect.</p> <p>VSP refers to the Frame Memory line Pointer.</p> <p>X = void</p>													0	1	2	3	4	861	862	863	863	862	861	4	3	2	1	0
	0																																
	1																																
	2																																
3																																	
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3																																	
2																																	
1																																	
0																																	
Restriction	Since the value of the Vertical Scrolling Start Address is absolute (with reference to the Frame Memory), it must not enter the fixed area (defined by Vertical Scrolling Definition (33h). Otherwise, undesirable image will occur on the Panel.																																

Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default	<table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>00h</td></tr> <tr> <td>S/W Reset</td><td>00h</td></tr> <tr> <td>H/W Reset</td><td>00h</td></tr> </tbody> </table>	Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h				
Status	Default Value												
Power On Sequence	00h												
S/W Reset	00h												
H/W Reset	00h												
Flow Chart	See Vertical Scrolling Definition (33h) description.												

4.2.36. Idle Mode Off (38h)

38h	IDMOFF (Idle Mode Off)																								
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	0	0	1	1	1	0	0	0	38h												
Parameter	No parameter																								
Description	This command causes the Display module to exit the Idle mode. In the Idle Mode Off, the display panel can display a maximum of 16.7M colors.																								
Restriction	This command has no effect when the module is already in the Idle Mode Off.																								
Register Availability	<table><thead><tr><th>Status</th><th>Availability</th></tr></thead><tbody><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></tbody></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><thead><tr><th>Status</th><th>Default Value</th></tr></thead><tbody><tr><td>Power On Sequence</td><td>Idle Mode Off</td></tr><tr><td>S/W Reset</td><td>Idle Mode Off</td></tr><tr><td>H/W Reset</td><td>Idle Mode Off</td></tr></tbody></table>													Status	Default Value	Power On Sequence	Idle Mode Off	S/W Reset	Idle Mode Off	H/W Reset	Idle Mode Off				
Status	Default Value																								
Power On Sequence	Idle Mode Off																								
S/W Reset	Idle Mode Off																								
H/W Reset	Idle Mode Off																								
Flow Chart	<div><div><div>Idle mode on</div><div>↓</div><div>IDMOFF(38h)</div><div>↓</div><div>Idle mode off</div></div><div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div></div>																								

4.2.37. Idle Mode On (39h)

39h	IDMON (Idle Mode On)																																																				
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																								
Command	0	1	↑	XX	0	0	1	1	1	0	0	1	39h																																								
Parameter	No parameter																																																				
Description	<p>This command is used to enter the Idle Mode On. In the Idle Mode On, color expression is reduced. The first bits of R, G, and B in the Frame Memory will determine the display color, as shown in the table below.</p> <div><div><p>Memory</p></div><div><p>Panel Display</p></div></div> <table><tr><th colspan="4">Memory Contents vs. Display Color</th></tr><tr><th></th><th>R₇ - R₀</th><th>G₇ - G₀</th><th>B₇ - B₀</th></tr><tr><td>Black</td><td>0XXXXXXX</td><td>0XXXXXXX</td><td>0XXXXXXX</td></tr><tr><td>Blue</td><td>0XXXXXXX</td><td>0XXXXXXX</td><td>1XXXXXXX</td></tr><tr><td>Red</td><td>1XXXXXXX</td><td>0XXXXXXX</td><td>0XXXXXXX</td></tr><tr><td>Magenta</td><td>1XXXXXXX</td><td>0XXXXXXX</td><td>1XXXXXXX</td></tr><tr><td>Green</td><td>0XXXXXXX</td><td>1XXXXXXX</td><td>0XXXXXXX</td></tr><tr><td>Cyan</td><td>0XXXXXXX</td><td>1XXXXXXX</td><td>1XXXXXXX</td></tr><tr><td>Yellow</td><td>1XXXXXXX</td><td>1XXXXXXX</td><td>0XXXXXXX</td></tr><tr><td>White</td><td>1XXXXXXX</td><td>1XXXXXXX</td><td>1XXXXXXX</td></tr></table> <p>X = void</p>													Memory Contents vs. Display Color					R ₇ - R ₀	G ₇ - G ₀	B ₇ - B ₀	Black	0XXXXXXX	0XXXXXXX	0XXXXXXX	Blue	0XXXXXXX	0XXXXXXX	1XXXXXXX	Red	1XXXXXXX	0XXXXXXX	0XXXXXXX	Magenta	1XXXXXXX	0XXXXXXX	1XXXXXXX	Green	0XXXXXXX	1XXXXXXX	0XXXXXXX	Cyan	0XXXXXXX	1XXXXXXX	1XXXXXXX	Yellow	1XXXXXXX	1XXXXXXX	0XXXXXXX	White	1XXXXXXX	1XXXXXXX	1XXXXXXX
	Memory Contents vs. Display Color																																																				
		R ₇ - R ₀	G ₇ - G ₀	B ₇ - B ₀																																																	
	Black	0XXXXXXX	0XXXXXXX	0XXXXXXX																																																	
Blue	0XXXXXXX	0XXXXXXX	1XXXXXXX																																																		
Red	1XXXXXXX	0XXXXXXX	0XXXXXXX																																																		
Magenta	1XXXXXXX	0XXXXXXX	1XXXXXXX																																																		
Green	0XXXXXXX	1XXXXXXX	0XXXXXXX																																																		
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Yellow	1XXXXXXX	1XXXXXXX	0XXXXXXX																																																		
White	1XXXXXXX	1XXXXXXX	1XXXXXXX																																																		
Restriction	This command has no effect when the module is already in the Idle Mode Off.																																																				
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes																												
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Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Idle Mode Off</td></tr><tr><td>S/W Reset</td><td>Idle Mode Off</td></tr><tr><td>H/W Reset</td><td>Idle Mode Off</td></tr></table>													Status	Default Value	Power On Sequence	Idle Mode Off	S/W Reset	Idle Mode Off	H/W Reset	Idle Mode Off																																
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Power On Sequence	Idle Mode Off																																																				
S/W Reset	Idle Mode Off																																																				
H/W Reset	Idle Mode Off																																																				
Flow Chart	<div><div></div><div><p>Legend</p><ul style="list-style-type: none">CommandParameterDisplayActionModeSequential transfer</div></div>																																																				

4.2.38. Interface Pixel Format (3Ah)

3Ah	COLMOD (Interface Pixel Format)																																							
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX																											
Command	0	1	↑	XX	0	0	1	1	1	0	1	0	3Ah																											
Parameter	1	1	↑	XX	0	DPI [2:0]			X	DBI [2:0]			XX																											
Description	This command sets the pixel format. DPI [3:0] selects the pixel format of the RGB interface, and DBI [2:0] select the pixel format of the MPU interface.																																							
	<table><tr><th colspan="3">DPI [2:0]</th><th>RGB Interface Format</th></tr><tr><td>1</td><td>0</td><td>1</td><td>16-bit/pixel</td></tr><tr><td>1</td><td>1</td><td>0</td><td>18-bit/pixel</td></tr><tr><td>1</td><td>1</td><td>1</td><td>24-bit/pixel</td></tr></table>				DPI [2:0]			RGB Interface Format	1	0	1	16-bit/pixel	1	1	0	18-bit/pixel	1	1	1	24-bit/pixel	<table><tr><th colspan="3">DBI [2:0]</th><th>MPU Interface Format</th></tr><tr><td>1</td><td>0</td><td>1</td><td>16-bit/pixel</td></tr><tr><td>1</td><td>1</td><td>0</td><td>18-bit/pixel</td></tr><tr><td>1</td><td>1</td><td>1</td><td>24-bit/pixel</td></tr></table>				DBI [2:0]			MPU Interface Format	1	0	1	16-bit/pixel	1	1	0	18-bit/pixel	1	1	1	24-bit/pixel
	DPI [2:0]			RGB Interface Format																																				
	1	0	1	16-bit/pixel																																				
	1	1	0	18-bit/pixel																																				
1	1	1	24-bit/pixel																																					
DBI [2:0]			MPU Interface Format																																					
1	0	1	16-bit/pixel																																					
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X = void																																								
Restriction																																								
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes															
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Partial Mode On, Idle Mode Off, Sleep Out	Yes																																							
Partial Mode On, Idle Mode On, Sleep Out	Yes																																							
Sleep In	Yes																																							
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>07h</td></tr><tr><td>S/W Reset</td><td>07h</td></tr><tr><td>H/W Reset</td><td>07h</td></tr></table>													Status	Default Value	Power On Sequence	07h	S/W Reset	07h	H/W Reset	07h																			
Status	Default Value																																							
Power On Sequence	07h																																							
S/W Reset	07h																																							
H/W Reset	07h																																							
Flow Chart	<div>Example :</div> <div><div>18 bit/pixel Mode</div><div>↓</div><div>COLMOD(3Ah) DBI: 111</div><div>↓</div><div>24 bit/pixel Mode</div></div> <div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>																																							


4.2.39. Memory Write Continue (3Ch)

3Ch	RAMWRC (Memory Write Continue)																											
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX															
Command	0	1	↑	XX	0	0	1	1	1	1	0	0	3Ch															
1 st Parameter	1	1	↑	D1 [23:0]									XX															
:	1	1	↑	Dx [23:0]									XX															
N th Parameter	1	1	↑	Dn [23:0]									XX															
Description	<p>This command is used to transfer data from the MPU to the frame memory if the frame memory wants to continue memory write after the “Memory Write (2Ch)” command. This command makes no change to the other status of the driver.</p> <p>When this command is accepted, the column register and the page register will not reset to the Start Column/Start Page positions after it is done on the “Memory Write (2Ch)” command.</p> <p>Then D [23:0] is stored in the frame memory and the column register and the page register are incremented, as the table below:</p> <p>Column and Page Counter Control.</p> <table><tr><th>Condition</th><th>Column counter</th><th>Page Counter</th></tr><tr><td>When RAMWR/RAMRD command is accepted</td><td>Return to “Start Column”</td><td>Return to “Start Page”</td></tr><tr><td>Complete Pixel Read/Write action</td><td>Increment by 1</td><td>No change</td></tr><tr><td>The Column counter value is large than “End Column”</td><td>Return to “Start Column”</td><td>Increment by 1</td></tr><tr><td>The Page counter value is large than “End Page”</td><td>Return to “Start Column”</td><td>Return to “Start Page”</td></tr></table> <p>Sending any other command can stop the Memory Write Continue command.</p> <p>X = void</p>													Condition	Column counter	Page Counter	When RAMWR/RAMRD command is accepted	Return to “Start Column”	Return to “Start Page”	Complete Pixel Read/Write action	Increment by 1	No change	The Column counter value is large than “End Column”	Return to “Start Column”	Increment by 1	The Page counter value is large than “End Page”	Return to “Start Column”	Return to “Start Page”
Condition	Column counter	Page Counter																										
When RAMWR/RAMRD command is accepted	Return to “Start Column”	Return to “Start Page”																										
Complete Pixel Read/Write action	Increment by 1	No change																										
The Column counter value is large than “End Column”	Return to “Start Column”	Increment by 1																										
The Page counter value is large than “End Page”	Return to “Start Column”	Return to “Start Page”																										
Restriction	There is no restriction on the length of parameters. No access to the frame memory in the Sleep In mode.																											
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes			
Status	Availability																											
Normal Mode On, Idle Mode Off, Sleep Out	Yes																											
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Partial Mode On, Idle Mode Off, Sleep Out	Yes																											
Partial Mode On, Idle Mode On, Sleep Out	Yes																											
Sleep In	Yes																											
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Contents of memory is set randomly</td></tr><tr><td>S/W Reset</td><td>Contents of memory is set randomly</td></tr><tr><td>H/W Reset</td><td>Contents of memory is set randomly</td></tr></table>													Status	Default Value	Power On Sequence	Contents of memory is set randomly	S/W Reset	Contents of memory is set randomly	H/W Reset	Contents of memory is set randomly							
Status	Default Value																											
Power On Sequence	Contents of memory is set randomly																											
S/W Reset	Contents of memory is set randomly																											
H/W Reset	Contents of memory is set randomly																											
Flow Chart	<div><div><div>RAMWRC(3Ch)</div><div>Image Data D1[23:0],D2[23:0], ...,Dn[23:0]</div><div>Next Command</div></div><div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div></div>																											

4.2.40. Memory Read Continue (3Eh)

3Eh	RAMRDC (Memory Read Continue)																											
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX															
Command	0	1	↑	XX	0	0	1	1	1	1	1	0	3Eh															
1 st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	XX															
2 nd Parameter	1	↑	1	D1 [15:0]									XX															
:	1	↑	1	Dx [15:0]									XX															
N th Parameter	1	↑	1	Dn [15:0]									XX															
Description	This command is used to transfer data from the Frame Memory to the MPU, if the MPU wants to continue memory read after “Memory Read (2Eh)” command. This command makes no change to the other status of the driver.																											
	When this command is accepted, the column register and the page register will not reset to the Start Column/Start Page positions since it is done on the “Memory Read (2Eh)” command.																											
	Then D [15:0] is read back from the frame memory, and the column register and the page register are incremented, as the table below: Column and Page Counter Control.																											
	<table><tr><th>Condition</th><th>Column counter</th><th>Page Counter</th></tr><tr><td>When RAMWR/RAMRD command is accepted</td><td>Return to “Start Column”</td><td>Return to “Start Page”</td></tr><tr><td>Complete Pixel Read/Write action</td><td>Increment by 1</td><td>No change</td></tr><tr><td>The Column counter value is large than “End Column”</td><td>Return to “Start Column”</td><td>Increment by 1</td></tr><tr><td>The Page counter value is large than “End Page”</td><td>Return to “Start Column”</td><td>Return to “Start Page”</td></tr></table>						Condition	Column counter	Page Counter	When RAMWR/RAMRD command is accepted	Return to “Start Column”	Return to “Start Page”	Complete Pixel Read/Write action	Increment by 1	No change	The Column counter value is large than “End Column”	Return to “Start Column”	Increment by 1	The Page counter value is large than “End Page”	Return to “Start Column”	Return to “Start Page”							
	Condition	Column counter	Page Counter																									
	When RAMWR/RAMRD command is accepted	Return to “Start Column”	Return to “Start Page”																									
	Complete Pixel Read/Write action	Increment by 1	No change																									
The Column counter value is large than “End Column”	Return to “Start Column”	Increment by 1																										
The Page counter value is large than “End Page”	Return to “Start Column”	Return to “Start Page”																										
Sending any other command can stop the Memory Read Continue command.																												
X = void.																												
Restriction	There is no restriction on the length of parameters. No access to the frame memory in the Sleep In mode.																											
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes			
Status	Availability																											
Normal Mode On, Idle Mode Off, Sleep Out	Yes																											
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Status	Default Value																											
Power On Sequence	Contents of memory is set randomly																											
S/W Reset	Contents of memory is set randomly																											
H/W Reset	Contents of memory is set randomly																											
Flow Chart	<div><div><div>RAMRDC(3Eh)</div><div>Dummy read</div><div>Image Data D1[23:0],D2[23:0], ...,Dn[23:0]</div><div>Next Command</div></div><div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div></div>																											

4.2.41. Write Tear Scan Line (44h)

44h	TESLWR (Write Tear Scan Line)																								
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	0	1	0	0	0	1	0	0	44h												
1 st Parameter	1	1	↑	XX	N [15:8]								XX												
2 nd Parameter	1	1	↑	XX	N [7:0]								XX												
Description	<p>This command turns on the display Tearing Effect output signal on the TE signal line when the display reaches line N. Changing Memory Access Control (36h) D4 will not affect the TE signal. The Tearing Effect Line On has one parameter that describes the Tearing Effect Output Line mode. The Tearing Effect Output line consists of V-Blanking information only.</p> <div><p>Vertical Time Scale</p></div> <p>Note that set Tear Scan Line with N = 0 is equivalent to Tearing Effect Line ON with M = 0.</p> <p>The Tearing Effect Output line shall be active low when the ILI9806G is in the Sleep mode.</p>																								
Restriction	This command has no effect when the Tearing Effect output is already ON.																								
Register Availability	<table><thead><tr><th>Status</th><th>Availability</th></tr></thead><tbody><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></tbody></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><thead><tr><th>Status</th><th>Default Value</th></tr></thead><tbody><tr><td>Power On Sequence</td><td>00h</td></tr><tr><td>S/W Reset</td><td>00h</td></tr><tr><td>H/W Reset</td><td>00h</td></tr></tbody></table>													Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h				
Status	Default Value																								
Power On Sequence	00h																								
S/W Reset	00h																								
H/W Reset	00h																								
Flow Chart	<div><div><p>TE Output ON or OFF</p><p>TESLWR (44h)</p><p>1st Parameter : N[15:8]</p><p>2nd Parameter : N[7:0]</p><p>TE Line Output ON</p></div><div><p>Legend</p><ul style="list-style-type: none">CommandParameterDisplayActionModeSequential transfer</div></div>																								

4.2.42. Read Scan Line (45h)

45h	TESLRD (Read Tear Scan Line)																								
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	0	1	0	0	0	1	0	1	45h												
1 st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	XX												
2 nd Parameter	1	↑	1	XX	N [15:8]								XX												
3 rd Parameter	1	↑	1	XX	N [7:0]								XX												
Description	The display reads the current scan line N, used to update the display device. The total number of scan lines on a display device is defined as VSYNC + VBP + VACT + VFP. The first scan line is defined as the first line of V-Sync and is denoted as Line 0. When in the Sleep Mode, the value returned by the Read Scan Line command is undefined.																								
Restriction																									
Register Availability	<table><thead><tr><th>Status</th><th>Availability</th></tr></thead><tbody><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></tbody></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><thead><tr><th>Status</th><th>Default Value</th></tr></thead><tbody><tr><td>Power On Sequence</td><td>00h</td></tr><tr><td>S/W Reset</td><td>00h</td></tr><tr><td>H/W Reset</td><td>00h</td></tr></tbody></table>													Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h				
Status	Default Value																								
Power On Sequence	00h																								
S/W Reset	00h																								
H/W Reset	00h																								
Flow Chart	<div><div><div>TESLRD(45h)</div><div>Dummy Read</div><div>2nd Parameter : N [15:8]</div><div>3rd Parameter : N [7:0]</div></div><div>Host Driver</div><div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div></div>																								

4.2.43. Write Display Brightness Value (51h)

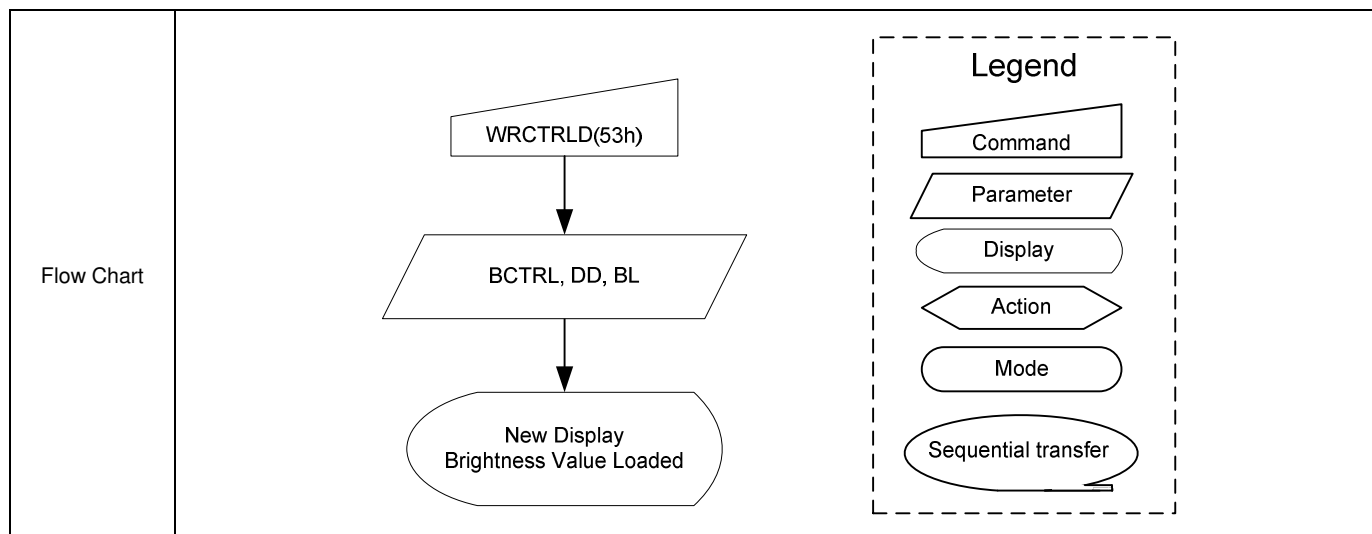
51h	WRDISBV (Write Display Brightness)																								
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	0	1	0	1	0	0	0	1	51h												
1 st Parameter	1	1	↑	XX	DBV [7:0]								XX												
Description	This command is used to adjust the brightness value of the display. DBV [7:0]: 8 bit, for display brightness of manual brightness setting and the CABC in the ILI9806G. PWM output signal and LEDPWM pin will control the LED driver IC in order to control the display brightness.																								
Restriction																									
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>00h</td></tr><tr><td>S/W Reset</td><td>00h</td></tr><tr><td>H/W Reset</td><td>00h</td></tr></table>													Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h				
Status	Default Value																								
Power On Sequence	00h																								
S/W Reset	00h																								
H/W Reset	00h																								
Flow Chart	<div><div><div>WRDISBV(51h)</div><div>↓</div><div>DBV [7:0]</div><div>↓</div><div>New Display Brightness Value Loaded</div></div><div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div></div>																								

4.2.44. Read Display Brightness Value (52h)

52h	RDISBV (Read Display Brightness Value)																								
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	0	1	0	1	0	0	1	0	52h												
1 st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	XX												
2 nd Parameter	1	↑	1	XX	DBV [7:0]								XX												
Description	<p>This command is used to return the brightness value of the display.</p> <p>DBV [7:0] is reset when display is in the Sleep In mode.</p> <p>DBV [7:0] is 0 when the bit BCTRL of “Write CTRL Display (53h)” command is 0.</p> <p>DBV [7:0] is the manual set brightness specified by the Write CTRL Display (53h) command when BCTRL bit is 1.</p> <p>When the bit BCTRL of the Write CTRL Display (53h) command is 1 and C1/C0 bit of the Write Content Adaptive Brightness Control (55h) command are 0, DBV [7:0] output is the brightness value specified by the Write Display Brightness (51h) command.</p>																								
Restriction	<p>The ILI9806G sends the 2nd parameter value to the data lines if the MPU wants to read more than one parameter (= more than 2 RDX cycle) on the parallel MPU interface.</p> <p>Only the 2nd parameter is sent on the DSI; the 1st parameter is not sent.</p>																								
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>00h</td></tr><tr><td>S/W Reset</td><td>00h</td></tr><tr><td>H/W Reset</td><td>00h</td></tr></table>													Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h				
Status	Default Value																								
Power On Sequence	00h																								
S/W Reset	00h																								
H/W Reset	00h																								
	<div><div><div>RDISBV(52h)</div><div>Host</div><div>Driver</div><div>1st Parameter: Dummy Read 2nd Parameter: Display Brightness Value Read</div></div><div><div>Legend</div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>																								

4.2.45. Write CTRL Display Value (53h)

53h	WRCTRLD (Write Control Display)																								
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	0	1	0	1	0	0	1	1	53h												
1 st Parameter	1	1	↑	XX	X	X	BCTRL	X	DD	BL	X	X	XX												
Description	This command is used to control the display brightness.																								
	BCTRL : Brightness Control Block On/Off. This bit is always used to switch brightness for display.																								
	<table><tr><th>BCTRL</th><th>Description</th></tr><tr><td>0</td><td>Brightness Control Block Off (DBV [7:0] = 00h)</td></tr><tr><td>1</td><td>Brightness Control Block On (DBV [7:0] is active)</td></tr></table>													BCTRL	Description	0	Brightness Control Block Off (DBV [7:0] = 00h)	1	Brightness Control Block On (DBV [7:0] is active)						
	BCTRL	Description																							
	0	Brightness Control Block Off (DBV [7:0] = 00h)																							
	1	Brightness Control Block On (DBV [7:0] is active)																							
	DD : Display Dimming Control. This function is only for manual brightness setting.																								
	<table><tr><th>DD</th><th>Description</th></tr><tr><td>0</td><td>Display Dimming Off</td></tr><tr><td>1</td><td>Display Dimming On</td></tr></table>													DD	Description	0	Display Dimming Off	1	Display Dimming On						
	DD	Description																							
	0	Display Dimming Off																							
1	Display Dimming On																								
BL : Backlight Control On/Off																									
<table><tr><th>BL</th><th>Description</th></tr><tr><td>0</td><td>Backlight Control Off</td></tr><tr><td>1</td><td>Backlight Control On</td></tr></table>													BL	Description	0	Backlight Control Off	1	Backlight Control On							
BL	Description																								
0	Backlight Control Off																								
1	Backlight Control On																								
Dimming function is adapted to the brightness registers for display when the bit BCTRL is changed at DD = 1, e.g. BCTRL: 0->1 or 1-> 0.																									
When the BL bit changes from ON to OFF, backlight is turned off without gradual dimming, even if Display Dimming On (DD = 1) are selected.																									
X = void																									
Restriction																									
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>00h</td></tr><tr><td>S/W Reset</td><td>No Change</td></tr><tr><td>H/W Reset</td><td>00h</td></tr></table>													Status	Default Value	Power On Sequence	00h	S/W Reset	No Change	H/W Reset	00h				
Status	Default Value																								
Power On Sequence	00h																								
S/W Reset	No Change																								
H/W Reset	00h																								

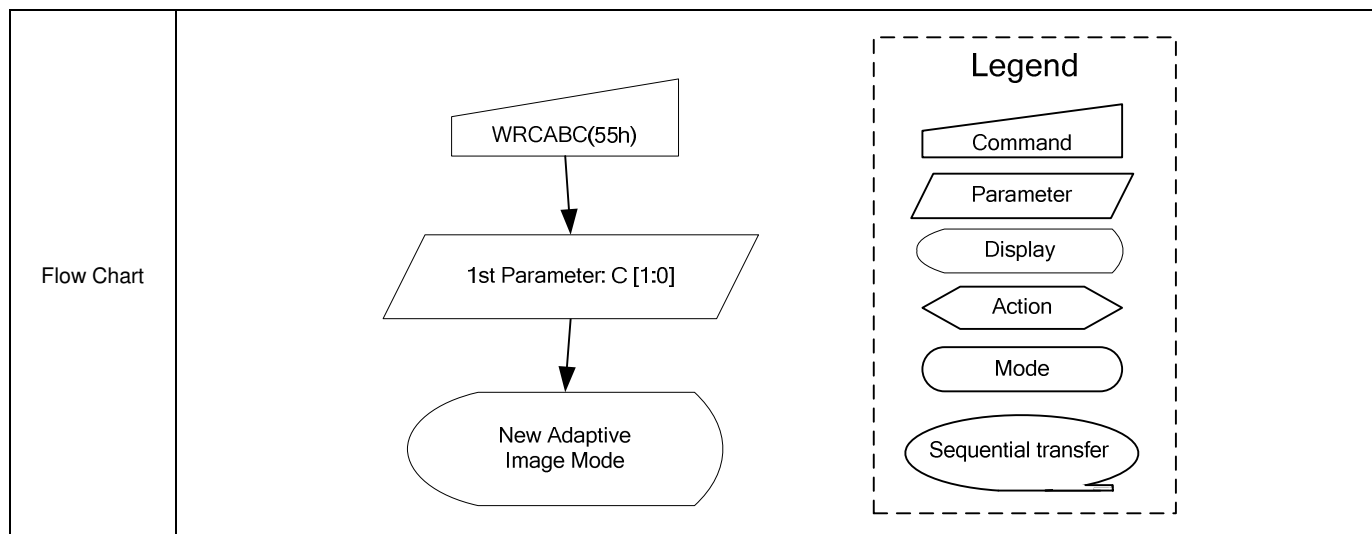


4.2.46. Read CTRL Display Value (54h)

54h	RDCTRLD (Read Control Display Value)																								
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	0	1	0	1	0	1	0	0	54h												
1 st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	XX												
2 nd Parameter	1	↑	1	XX	X	X	BCTRL	X	DD	BL	X	X	XX												
Description	This command is used to control the display brightness.																								
	BCTRL: Brightness Control Block On/Off. This bit is always used to switch brightness for display.																								
	<table><tr><th>BCTRL</th><th>Description</th></tr><tr><td>0</td><td>Brightness Control Block Off (DBV [7:0] = 00h)</td></tr><tr><td>1</td><td>Brightness Control Block On (DBV [7:0] is active)</td></tr></table>													BCTRL	Description	0	Brightness Control Block Off (DBV [7:0] = 00h)	1	Brightness Control Block On (DBV [7:0] is active)						
	BCTRL	Description																							
	0	Brightness Control Block Off (DBV [7:0] = 00h)																							
	1	Brightness Control Block On (DBV [7:0] is active)																							
	DD: Display Dimming Control. This function is only for manual brightness setting.																								
	<table><tr><th>DD</th><th>Description</th></tr><tr><td>0</td><td>Display Dimming Off</td></tr><tr><td>1</td><td>Display Dimming On</td></tr></table>													DD	Description	0	Display Dimming Off	1	Display Dimming On						
	DD	Description																							
	0	Display Dimming Off																							
1	Display Dimming On																								
BL: Backlight Control On/Off																									
<table><tr><th>BL</th><th>Description</th></tr><tr><td>0</td><td>Backlight Control Off</td></tr><tr><td>1</td><td>Backlight Control On</td></tr></table>													BL	Description	0	Backlight Control Off	1	Backlight Control On							
BL	Description																								
0	Backlight Control Off																								
1	Backlight Control On																								
X = Void																									
Restriction																									
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
	Status	Availability																							
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>00h</td></tr><tr><td>S/W Reset</td><td>No Change</td></tr><tr><td>H/W Reset</td><td>00h</td></tr></table>													Status	Default Value	Power On Sequence	00h	S/W Reset	No Change	H/W Reset	00h				
Status	Default Value																								
Power On Sequence	00h																								
S/W Reset	No Change																								
H/W Reset	00h																								
Flow Chart	<div><div><div>RDCTRLD(54h)</div><div>↓</div><div>1st Parameter: Dummy Read 2nd Parameter: Control Display Value Read</div></div><div>Host ----- Driver</div></div> <div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>																								

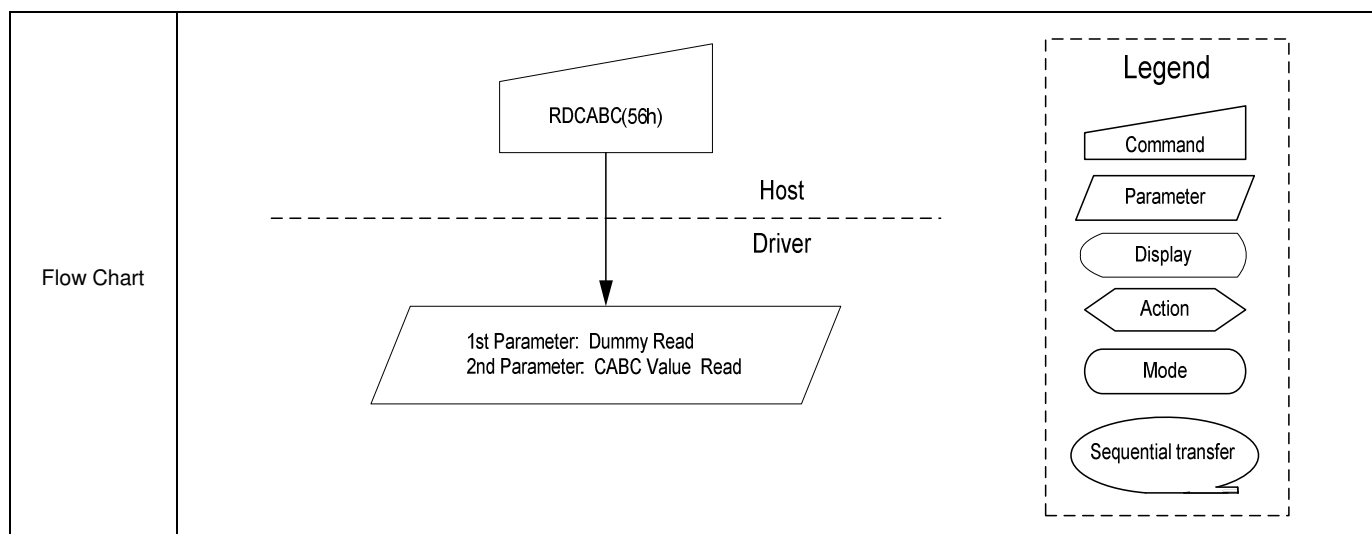
4.2.47. Write Content Adaptive Brightness Control Value (55h)

55h	WRCABC (Write Content Adaptive Brightness Control)																																																														
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																		
Command	0	1	↑	XX	0	1	0	1	0	1	0	1	55h																																																		
1 st Parameter	1	1	↑	XX	C[7:4]				C [3:0]				XX																																																		
Description	<p>This command is used to set parameters for image content based on the adaptive brightness control functionality.</p> <p>There are 4 different modes for content adaptive image functionality, which are defined in the table below.</p> <table><tr><th colspan="4">C [3:0]</th><th>Description</th></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>CABC Off</td></tr><tr><td>0</td><td>0</td><td>0</td><td>1</td><td>User Interface Image mode</td></tr><tr><td>0</td><td>0</td><td>1</td><td>0</td><td>Still Picture mode</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1</td><td>Moving Image mode</td></tr></table> <p>Color enhancement level selection.</p> <table><tr><th colspan="4">C [7:4]</th><th>Description</th></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>Enhancement Disable</td></tr><tr><td>1</td><td>0</td><td>0</td><td>0</td><td>Low Enhancement</td></tr><tr><td>1</td><td>0</td><td>0</td><td>1</td><td>Medium Enhancement</td></tr><tr><td>1</td><td>0</td><td>1</td><td>1</td><td>High Enhancement</td></tr></table> <p>X = Void</p>													C [3:0]				Description	0	0	0	0	CABC Off	0	0	0	1	User Interface Image mode	0	0	1	0	Still Picture mode	0	0	1	1	Moving Image mode	C [7:4]				Description	0	0	0	0	Enhancement Disable	1	0	0	0	Low Enhancement	1	0	0	1	Medium Enhancement	1	0	1	1	High Enhancement
	C [3:0]				Description																																																										
	0	0	0	0	CABC Off																																																										
	0	0	0	1	User Interface Image mode																																																										
	0	0	1	0	Still Picture mode																																																										
0	0	1	1	Moving Image mode																																																											
C [7:4]				Description																																																											
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1	0	0	0	Low Enhancement																																																											
1	0	0	1	Medium Enhancement																																																											
1	0	1	1	High Enhancement																																																											
Restriction																																																															
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes																																						
Status	Availability																																																														
Normal Mode On, Idle Mode Off, Sleep Out	Yes																																																														
Normal Mode On, Idle Mode On, Sleep Out	Yes																																																														
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Partial Mode On, Idle Mode On, Sleep Out	Yes																																																														
Sleep In	Yes																																																														
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>00h</td></tr><tr><td>S/W Reset</td><td>00h</td></tr><tr><td>H/W Reset</td><td>00h</td></tr></table>													Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h																																										
Status	Default Value																																																														
Power On Sequence	00h																																																														
S/W Reset	00h																																																														
H/W Reset	00h																																																														



4.2.48. Read Content Adaptive Brightness Control Value (56h)

56h	RDCABC (Read Content Adaptive Brightness Control)																																					
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX																									
Command	0	1	↑	XX	0	1	0	1	0	1	1	0	56h																									
1 st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	XX																									
2 nd Parameter	1	↑	1	XX	C[7:4]				C [3:0]				XX																									
Description	This command is used to read the settings for image content based on the adaptive brightness control functionality. There are 4 different modes for content adaptive image functionality, which are defined in the table below.																																					
	<table><tr><th colspan="4">C [3:0]</th><th>Description</th></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>CABC Off</td></tr><tr><td>0</td><td>0</td><td>0</td><td>1</td><td>User Interface Image mode</td></tr><tr><td>0</td><td>0</td><td>1</td><td>0</td><td>Still Picture mode</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1</td><td>Moving Image mode</td></tr></table>													C [3:0]				Description	0	0	0	0	CABC Off	0	0	0	1	User Interface Image mode	0	0	1	0	Still Picture mode	0	0	1	1	Moving Image mode
	C [3:0]				Description																																	
	0	0	0	0	CABC Off																																	
	0	0	0	1	User Interface Image mode																																	
	0	0	1	0	Still Picture mode																																	
	0	0	1	1	Moving Image mode																																	
	Color enhancement level selection.																																					
	<table><tr><th colspan="4">C [7:4]</th><th>Description</th></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>Enhancement Disable</td></tr><tr><td>1</td><td>0</td><td>0</td><td>0</td><td>Low Enhancement</td></tr><tr><td>1</td><td>0</td><td>0</td><td>1</td><td>Medium Enhancement</td></tr><tr><td>1</td><td>0</td><td>1</td><td>1</td><td>High Enhancement</td></tr></table>													C [7:4]				Description	0	0	0	0	Enhancement Disable	1	0	0	0	Low Enhancement	1	0	0	1	Medium Enhancement	1	0	1	1	High Enhancement
	C [7:4]				Description																																	
0	0	0	0	Enhancement Disable																																		
1	0	0	0	Low Enhancement																																		
1	0	0	1	Medium Enhancement																																		
1	0	1	1	High Enhancement																																		
X = Void																																						
Restriction																																						
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes													
Status	Availability																																					
Normal Mode On, Idle Mode Off, Sleep Out	Yes																																					
Normal Mode On, Idle Mode On, Sleep Out	Yes																																					
Partial Mode On, Idle Mode Off, Sleep Out	Yes																																					
Partial Mode On, Idle Mode On, Sleep Out	Yes																																					
Sleep In	Yes																																					
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>00h</td></tr><tr><td>S/W Reset</td><td>00h</td></tr><tr><td>H/W Reset</td><td>00h</td></tr></table>													Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h																	
Status	Default Value																																					
Power On Sequence	00h																																					
S/W Reset	00h																																					
H/W Reset	00h																																					



4.2.49. Write CABC Minimum Brightness (5Eh)

5Eh	WRCABCMB (Write CABC Minimum Brightness)																								
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	0	1	0	1	1	1	1	0	5Eh												
1 st Parameter	1	1	↑	XX	CMB [7:0]								XX												
Description	<p>This command is used to set the minimum brightness value of the display for the CABC function.</p> <p>CMB [7:0]: CABC minimum brightness control. This parameter is used to set a limit to the amount of brightness reduction allowed.</p> <p>When the CABC is active, it cannot reduce the display brightness to less than the CABC minimum brightness setting. Image processing function works normally, even if the brightness cannot be changed.</p> <p>This function does not affect the manual brightness setting. Manual brightness setting does not have a limit on allowable brightness reduction; display brightness can be set less than the CABC minimum brightness. Smooth transition and dimming function work normally.</p> <p>When the display brightness is turned off (BCTRL = 0 of Write CTRL Display (53h)), the CABC minimum brightness setting is ignored. The principle relationship is such that 00h value means the lowest brightness for the CABC, and FFh value means the highest brightness for the CABC.</p>																								
Restriction																									
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
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Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>00h</td></tr><tr><td>S/W Reset</td><td>No Change</td></tr><tr><td>H/W Reset</td><td>00h</td></tr></table>													Status	Default Value	Power On Sequence	00h	S/W Reset	No Change	H/W Reset	00h				
Status	Default Value																								
Power On Sequence	00h																								
S/W Reset	No Change																								
H/W Reset	00h																								
Flow Chart	<div><div><div>WRCABCMB(5Eh)</div><div>↓</div><div>1st Parameter: CMB[7:0]</div><div>↓</div><div>New Display Luminance Value Loaded</div></div><div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div></div>																								

4.2.50. Read CABC Minimum Brightness (5Fh)

5Fh	RDCABCMB (Read CABC Minimum Brightness)																								
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	0	1	0	1	1	1	1	1	5Fh												
1 st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	XX												
2 nd Parameter	1	↑	1	XX	CMB [7:0]							XX													
Description	<p>This command reads the minimum brightness value of the CABC function.</p> <p>The principle relationship is such that 00h value means the lowest brightness, and FFh value means the highest brightness.</p> <p>CMB [7:0] is the CABC minimum brightness specified by the Write CABC minimum brightness (5Eh) command.</p>																								
Restriction	<p>The ILI9806G sends the 2nd parameter value to the data lines if the MPU wants to read more than one parameter (= more than 2 RDX cycle) on parallel MPU interface.</p> <p>Only the 2nd parameter is sent on the DSI; the 1st parameter is not sent.</p>																								
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>00h</td></tr><tr><td>S/W Reset</td><td>No Change</td></tr><tr><td>H/W Reset</td><td>00h</td></tr></table>													Status	Default Value	Power On Sequence	00h	S/W Reset	No Change	H/W Reset	00h				
Status	Default Value																								
Power On Sequence	00h																								
S/W Reset	No Change																								
H/W Reset	00h																								
Flow Chart	<div><div><div>RDCABCMB(5Fh)</div><div>↓</div><div>1st Parameter: Dummy Read 2nd Parameter: CABC minimum Brightness Read</div></div><div>Host ----- Driver</div></div> <div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>																								

4.2.51. Read Automatic Brightness Control Self-diagnostic Result (68h)

68h	RDABCSDR (Read automatic brightness control self-diagnostic result)																								
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	0	1	1	0	1	0	0	0	68h												
1 st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	XX												
2 nd Parameter	1	↑	1	XX	D [7:6]		0	0	0	0	0	0	XX												
Description	<p>This command indicates the status of the display self-diagnostic results for automatic brightness control after the Sleep Out command, as described in the table below:</p> <p>Bit D7 – Register Loading Detection, see the section “Register loading Detection”.</p> <p>Bit D6 – Functionality Detection, see the section “Functionality Detection”.</p> <p>Bits D5, D4, D3, D2, D1 and D0 are for future use and are set to 0.</p>																								
Restriction																									
Register Availability	<table><thead><tr><th>Status</th><th>Availability</th></tr></thead><tbody><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></tbody></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
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Status	Default Value																								
Power On Sequence	00h																								
S/W Reset	00h																								
H/W Reset	00h																								
Flow Chart	<div><div><div>Read RDABCSDR(68h)</div><div>↓</div><div>1st Parameter: Dummy Read Send 2nd Parameter</div></div><div><div>Host</div><div>Driver</div></div></div> <div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>																								

4.2.52. Read Black/White Low Bits (70h)

70h	RDBWLB (Read Black/White Low Bits)																								
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	0	1	1	1	0	0	0	0	70h												
1 st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	XX												
2 nd Parameter	1	↑	1	XX	Bkx [1:0]		Bky [1:0]		Wx [1:0]		Wy [1:0]		XX												
Description	<p>This command reads the lowest bits of black and white color characteristics.</p> <p>Black: Bkx and Bky</p> <p>White: Wx and Wy</p> <p>X = void</p>																								
Restriction	<p>The ILI9806G sends the 2nd parameter value to the data lines if the MPU wants to read more than one parameter (= more than 2 RDX cycle) on the parallel MPU interface.</p> <p>Only the 2nd parameter is sent on the DSI; the 1st parameter is not sent.</p>																								
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>XXh</td></tr><tr><td>S/W Reset</td><td>XXh</td></tr><tr><td>H/W Reset</td><td>XXh</td></tr></table>													Status	Default Value	Power On Sequence	XXh	S/W Reset	XXh	H/W Reset	XXh				
Status	Default Value																								
Power On Sequence	XXh																								
S/W Reset	XXh																								
H/W Reset	XXh																								
Flow Chart	<div><div><div>RDBWLB(70h)</div><div>↓</div><div>Send 1st Parameter</div><div>↓</div><div>Send 2nd Parameter</div></div><div>Host ----- Driver</div><div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div></div>																								

4.2.53. Read Bkx (71h)

71h	RDBkx (Read Bkx)																								
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	0	1	1	1	0	0	0	1	71h												
1 st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	XX												
2 nd Parameter	1	↑	1	XX	Bkx [9:2]								XX												
Description	This command reads the Bkx bits (Bkx [9:2]) of black color characteristics. X = void																								
Restriction	The ILI9806G sends the 2 nd parameter value to the data lines if the MPU wants to read more than one parameter (= more than 2 RDX cycle) on the parallel MPU interface. Only the 2 nd parameter is sent on the DSI; the 1 st parameter is not sent.																								
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>XXh</td></tr><tr><td>S/W Reset</td><td>XXh</td></tr><tr><td>H/W Reset</td><td>XXh</td></tr></table>													Status	Default Value	Power On Sequence	XXh	S/W Reset	XXh	H/W Reset	XXh				
Status	Default Value																								
Power On Sequence	XXh																								
S/W Reset	XXh																								
H/W Reset	XXh																								
Flow Chart	<div><div><div>RDBkx(71h)</div><div>↓</div><div>Send 1st Parameter</div><div>↓</div><div>Send 2nd Parameter</div></div><div>Host ----- Driver</div><div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div></div>																								

4.2.54. Read Bky (72h)

72h	RDBky (Read Bky)																								
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	0	1	1	1	0	0	1	0	72h												
1 st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	XX												
2 nd Parameter	1	↑	1	XX	Bky [9:2]								XX												
Description	This command reads the Bky bits (Bky [9:2]) of black color characteristics. X = void																								
Restriction	The ILI9806G sends the 2 nd parameter value to the data lines if the MPU wants to read more than one parameter (= more than 2 RDX cycle) on the parallel MPU interface. Only the 2 nd parameter is sent on the DSI; the 1 st parameter is not sent.																								
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>XXh</td></tr><tr><td>S/W Reset</td><td>XXh</td></tr><tr><td>H/W Reset</td><td>XXh</td></tr></table>													Status	Default Value	Power On Sequence	XXh	S/W Reset	XXh	H/W Reset	XXh				
Status	Default Value																								
Power On Sequence	XXh																								
S/W Reset	XXh																								
H/W Reset	XXh																								
Flow Chart	<div><div><div>RDBky(72h)</div><div>↓</div><div>Send 1st Parameter</div><div>↓</div><div>Send 2nd Parameter</div></div><div>Host ----- Driver</div><div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div></div>																								

4.2.55. Read Wx (73h)

73h	RDWx (Read Wx)																								
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	0	1	1	1	0	0	1	1	73h												
1 st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	XX												
2 nd Parameter	1	↑	1	XX	Wx [9:2]								XX												
Description	This command reads the Wx bits (Wx [9:2]) of white color characteristics. X = void																								
Restriction	The ILI9806G sends the 2 nd parameter value to the data lines if the MPU wants to read more than one parameter (= more than 2 RDX cycle) on the parallel MPU interface. Only the 2 nd parameter is sent on the DSI; the 1 st parameter is not sent.																								
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
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Normal Mode On, Idle Mode On, Sleep Out	Yes																								
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Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
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Status	Default Value																								
Power On Sequence	XXh																								
S/W Reset	XXh																								
H/W Reset	XXh																								
Flow Chart	<div><div><div>RDWx(73h)</div><div>↓</div><div>Send 1st Parameter</div><div>↓</div><div>Send 2nd Parameter</div></div><div>Host ----- Driver</div><div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div></div>																								

4.2.56. Read Wy (74h)

74h	RDWy (Read Wy)																								
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	0	1	1	1	0	1	0	0	74h												
1 st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	XX												
2 nd Parameter	1	↑	1	XX	Wy [9:2]								XX												
Description	This command returns the Wy bits (Wy [9:2]) of white color characteristics. X = void																								
Restriction	The ILI9806G sends the 2 nd parameter value to the data lines if the MPU wants to read more than one parameter (= more than 2 RDX cycle) on the parallel MPU interface. Only the 2 nd parameter is sent on the DSI; the 1 st parameter is not sent.																								
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Sleep In	Yes																								
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Status	Default Value																								
Power On Sequence	XXh																								
S/W Reset	XXh																								
H/W Reset	XXh																								
Flow Chart	<div><div><div>RDWy(74h)</div><div>↓</div><div>Send 1st Parameter</div><div>↓</div><div>Send 2nd Parameter</div></div><div>Host ----- Driver</div><div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div></div>																								

4.2.57. Read Red/Green Low Bits (75h)

75h	RDRGLB (Read Red / Green Low Bits)																								
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	0	1	1	1	0	1	0	1	75h												
1 st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	XX												
2 nd Parameter	1	↑	1	XX	Rx [1:0]		Ry [1:0]		Gx [1:0]		Gy [1:0]		XX												
Description	<p>This command reads the lowest bits of red and green color characteristics.</p> <p>Red: Rx and Ry</p> <p>Green: Gx and Gy</p> <p>X = void</p>																								
Restriction	<p>The ILI9806G sends the 2nd parameter value to the data lines if the MPU wants to read more than one parameter (= more than 2 RDX cycle) on the parallel MPU interface.</p> <p>Only the 2nd parameter is sent on the DSI; the 1st parameter is not sent.</p>																								
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Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>XXh</td></tr><tr><td>S/W Reset</td><td>XXh</td></tr><tr><td>H/W Reset</td><td>XXh</td></tr></table>													Status	Default Value	Power On Sequence	XXh	S/W Reset	XXh	H/W Reset	XXh				
Status	Default Value																								
Power On Sequence	XXh																								
S/W Reset	XXh																								
H/W Reset	XXh																								
Flow Chart	<div><div><div>RDRGLB(75h)</div><div>↓</div><div>Send 1st Parameter</div><div>↓</div><div>Send 2nd Parameter</div></div><div>Host ----- Driver</div></div> <div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>																								

4.2.58. Read Rx (76h)

76h	RDRx (Read Rx)																								
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	0	1	1	1	0	1	1	0	76h												
1 st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	XX												
2 nd Parameter	1	↑	1	XX	Rx [9:2]								XX												
Description	This command reads the Rx bits (Rx [9:2]) of red color characteristics. X = void																								
Restriction	The ILI9806G sends the 2 nd parameter value to the data lines if the MPU wants to read more than one parameter (= more than 2 RDX cycle) on the parallel MPU interface. Only the 2 nd parameter is sent on the DSI; the 1 st parameter is not sent.																								
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>XXh</td></tr><tr><td>S/W Reset</td><td>XXh</td></tr><tr><td>H/W Reset</td><td>XXh</td></tr></table>													Status	Default Value	Power On Sequence	XXh	S/W Reset	XXh	H/W Reset	XXh				
Status	Default Value																								
Power On Sequence	XXh																								
S/W Reset	XXh																								
H/W Reset	XXh																								
Flow Chart	<div><div><div>RDRx(76h)</div><div>↓</div><div>Send 1st Parameter</div><div>↓</div><div>Send 2nd Parameter</div></div><div>Host ----- Driver</div><div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div></div>																								

4.2.59. Read Ry (77h)

77h	RDRy (Read Ry)																								
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	0	1	1	1	0	1	1	1	77h												
1 st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	XX												
2 nd Parameter	1	↑	1	XX	Ry [9:2]								XX												
Description	This command reads the Ry bits (Ry [9:2]) of red color characteristics. X = void																								
Restriction	The ILI9806G sends the 2 nd parameter value to the data lines if the MPU wants to read more than one parameter (= more than 2 RDX cycle) on the parallel MPU interface. Only the 2 nd parameter is sent on the DSI; the 1 st parameter is not sent.																								
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>XXh</td></tr><tr><td>S/W Reset</td><td>XXh</td></tr><tr><td>H/W Reset</td><td>XXh</td></tr></table>													Status	Default Value	Power On Sequence	XXh	S/W Reset	XXh	H/W Reset	XXh				
Status	Default Value																								
Power On Sequence	XXh																								
S/W Reset	XXh																								
H/W Reset	XXh																								
Flow Chart	<div><div><div>RDRy(77h)</div><div>↓</div><div>Send 1st Parameter</div><div>↓</div><div>Send 2nd Parameter</div></div><div>Host ----- Driver</div><div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div></div>																								

4.2.60. Read Gx (78h)

78h	RDGx (Read Gx)																								
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	0	1	1	1	1	0	0	0	78h												
1 st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	XX												
2 nd Parameter	1	↑	1	XX	Gx [9:2]								XX												
Description	This command reads the Gx bits (Gx [9:2]) of green color characteristics. X = void																								
Restriction	The ILI9806G sends the 2 nd parameter value to the data lines if the MPU wants to read more than one parameter (= more than 2 RDX cycle) on the parallel MPU interface. Only the 2 nd parameter is sent on the DSI; the 1 st parameter is not sent.																								
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>XXh</td></tr><tr><td>S/W Reset</td><td>XXh</td></tr><tr><td>H/W Reset</td><td>XXh</td></tr></table>													Status	Default Value	Power On Sequence	XXh	S/W Reset	XXh	H/W Reset	XXh				
Status	Default Value																								
Power On Sequence	XXh																								
S/W Reset	XXh																								
H/W Reset	XXh																								
Flow Chart	<div><div><div>RDGx(78h)</div><div>↓</div><div>Send 1st Parameter</div><div>↓</div><div>Send 2nd Parameter</div></div><div>Host ----- Driver</div><div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div></div>																								

4.2.61. Read Gy (79h)

79h	RDGy (Read Gy)																								
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	0	1	1	1	1	0	0	1	79h												
1 st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	XX												
2 nd Parameter	1	↑	1	XX	Gy [9:2]								XX												
Description	This command reads the Gy bits (Gy [9:2]) of green color characteristics. X = void																								
Restriction	The ILI9806G sends the 2 nd parameter value to the data lines if the MPU wants to read more than one parameter (= more than 2 RDX cycle) on the parallel MPU interface. Only the 2 nd parameter is sent on the DSI; the 1 st parameter is not sent.																								
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>XXh</td></tr><tr><td>S/W Reset</td><td>XXh</td></tr><tr><td>H/W Reset</td><td>XXh</td></tr></table>													Status	Default Value	Power On Sequence	XXh	S/W Reset	XXh	H/W Reset	XXh				
Status	Default Value																								
Power On Sequence	XXh																								
S/W Reset	XXh																								
H/W Reset	XXh																								
Flow Chart	<div><div><div>RDGy(79h)</div><div>↓</div><div>Send 1st Parameter</div><div>↓</div><div>Send 2nd Parameter</div></div><div>Host ----- Driver</div></div> <div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>																								

4.2.62. Read Blue/A Color Low Bits (7Ah)

7Ah	RDBALB (Read Blue / A Color Low Bits)																								
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	0	1	1	1	1	0	1	0	7Ah												
1 st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	XX												
2 nd Parameter	1	↑	1	XX	Bx [1:0]		By [1:0]		Ax [1:0]		Ay [1:0]		XX												
Description	<p>This command reads the lowest bits of blue and A color color characteristics.</p> <p>Blue: Bx and By</p> <p>A color: Ax and Ay</p> <p>X = void</p>																								
Restriction	<p>The ILI9806G sends the 2nd parameter value to the data lines if the MPU wants to read more than one parameter (= more than 2 RDX cycle) on the parallel MPU interface.</p> <p>Only the 2nd parameter is sent on the DSI; the 1st parameter is not sent.</p>																								
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>XXh</td></tr><tr><td>S/W Reset</td><td>XXh</td></tr><tr><td>H/W Reset</td><td>XXh</td></tr></table>													Status	Default Value	Power On Sequence	XXh	S/W Reset	XXh	H/W Reset	XXh				
Status	Default Value																								
Power On Sequence	XXh																								
S/W Reset	XXh																								
H/W Reset	XXh																								
Flow Chart	<div><div><div>RDBALB(7Ah)</div><div>↓</div><div>Send 1st Parameter</div><div>↓</div><div>Send 2nd Parameter</div></div><div>Host ----- Driver</div></div> <div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>																								

4.2.63. Read Bx (7Bh)

7Bh	RDBx (Read Bx)																								
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	0	1	1	1	1	0	1	1	7Bh												
1 st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	XX												
2 nd Parameter	1	↑	1	XX	Bx [9:2]								XX												
Description	This command reads the Bx bits (Bx [9:2]) of blue color characteristics. X = void																								
Restriction	The ILI9806G sends the 2 nd parameter value to the data lines if the MPU wants to read more than one parameter (= more than 2 RDX cycle) on the parallel MPU interface. Only the 2 nd parameter is sent on the DSI; the 1 st parameter is not sent.																								
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>XXh</td></tr><tr><td>S/W Reset</td><td>XXh</td></tr><tr><td>H/W Reset</td><td>XXh</td></tr></table>													Status	Default Value	Power On Sequence	XXh	S/W Reset	XXh	H/W Reset	XXh				
Status	Default Value																								
Power On Sequence	XXh																								
S/W Reset	XXh																								
H/W Reset	XXh																								
Flow Chart	<div><div><div>RDBx(7Bh)</div><div>↓</div><div>Send 1st Parameter</div><div>↓</div><div>Send 2nd Parameter</div></div><div>Host ----- Driver</div><div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div></div>																								

4.2.64. Read By (7Ch)

7Ch	RDBy (Read By)																								
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	0	1	1	1	1	1	0	0	7Ch												
1 st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	XX												
2 nd Parameter	1	↑	1	XX	By [9:2]								XX												
Description	This command reads the By bits (By [9:2]) of blue color characteristics. X = void																								
Restriction	The ILI9806G sends the 2 nd parameter value to the data lines if the MPU wants to read more than one parameter (= more than 2 RDX cycle) on the parallel MPU interface. Only the 2 nd parameter is sent on the DSI; the 1 st parameter is not sent.																								
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>XXh</td></tr><tr><td>S/W Reset</td><td>XXh</td></tr><tr><td>H/W Reset</td><td>XXh</td></tr></table>													Status	Default Value	Power On Sequence	XXh	S/W Reset	XXh	H/W Reset	XXh				
Status	Default Value																								
Power On Sequence	XXh																								
S/W Reset	XXh																								
H/W Reset	XXh																								
Flow Chart	<div><div><div>RDBy(7Ch)</div><div>↓</div><div>Send 1st Parameter</div><div>↓</div><div>Send 2nd Parameter</div></div><div>Host ----- Driver</div><div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div></div>																								

4.2.65. Read Ax (7Dh)

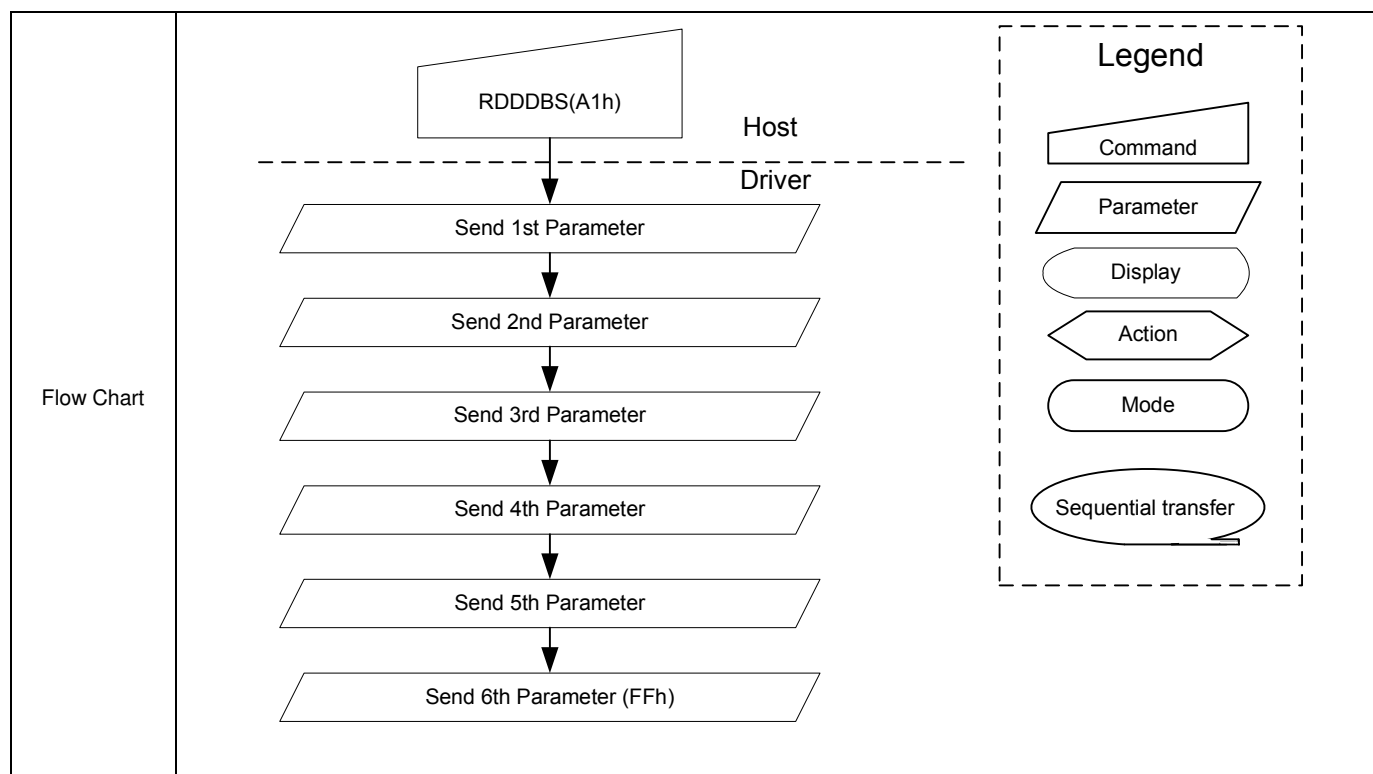
7Dh	RDAX (Read Ax)																								
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	0	1	1	1	1	1	0	1	7Dh												
1 st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	XX												
2 nd Parameter	1	↑	1	XX	Ax [9:2]								XX												
Description	<p>This command returns the Ax bits (Ax [9:2]) of A color characteristics.</p> <p>Ax [9:2] are set to 0 if they are not used.</p> <p>X = void</p>																								
Restriction	<p>The ILI9806G sends the 2nd parameter value to the data lines if the MPU wants to read more than one parameter (= more than 2 RDX cycle) on the parallel MPU interface.</p> <p>Only the 2nd parameter is sent on the DSI; the 1st parameter is not sent.</p>																								
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>XXh</td></tr><tr><td>S/W Reset</td><td>XXh</td></tr><tr><td>H/W Reset</td><td>XXh</td></tr></table>													Status	Default Value	Power On Sequence	XXh	S/W Reset	XXh	H/W Reset	XXh				
Status	Default Value																								
Power On Sequence	XXh																								
S/W Reset	XXh																								
H/W Reset	XXh																								
Flow Chart	<div><div><div>RDAx(7Dh)</div><div>↓</div><div>Send 1st Parameter</div><div>↓</div><div>Send 2nd Parameter</div></div><div>Host ----- Driver</div></div> <div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>																								

4.2.66. Read Ay (7Eh)

7Eh	RD _{Ay} (Read A _y)																								
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	0	1	1	1	1	1	1	0	7Eh												
1 st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	XX												
2 nd Parameter	1	↑	1	XX	A _y [9:2]								XX												
Description	<p>This command reads the A_y bits (A_y [9:2]) of A color characteristics.</p> <p>A_y [9:2] are set to 0 if they are not used.</p> <p>X = void</p>																								
Restriction	<p>The ILI9806G sends the 2nd parameter value to the data lines if the MPU wants to read more than one parameter (= more than 2 RDX cycle) on the parallel MPU interface.</p> <p>Only the 2nd parameter is sent on the DSI; the 1st parameter is not sent.</p>																								
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>XXh</td></tr><tr><td>S/W Reset</td><td>XXh</td></tr><tr><td>H/W Reset</td><td>XXh</td></tr></table>													Status	Default Value	Power On Sequence	XXh	S/W Reset	XXh	H/W Reset	XXh				
Status	Default Value																								
Power On Sequence	XXh																								
S/W Reset	XXh																								
H/W Reset	XXh																								
Flow Chart	<div><div><div>RD_{Ay}(7Eh)</div><div>↓</div><div>Send 1st Parameter</div><div>↓</div><div>Send 2nd Parameter</div></div><div>Host ----- Driver</div><div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div></div>																								

4.2.67. Read DDB Start (A1h)

A1h	RDDDBS (Read DDB Start)																																																																									
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																													
Command	0	1	↑	XX	1	0	1	0	0	0	0	1	A1h																																																													
1 st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	XX																																																													
2 nd Parameter	1	↑	1	XX	SID [7:0]								XX																																																													
3 rd Parameter	1	↑	1	XX	SID [15:8]								XX																																																													
4 th Parameter	1	↑	1	XX	MRID [7:0]								XX																																																													
5 th Parameter	1	↑	1	XX	MRID [15:8]								XX																																																													
6 th Parameter	1	↑	1	XX	1	1	1	1	1	1	1	1	FF																																																													
Description	This command reads the supplier identification and display module mode/revision information.																																																																									
	Note: This information is not the same as which “Read ID1 (DAh)”, “Read ID2 (DBh)” and “Read ID3 (DCh)” commands return.																																																																									
	Parameter 2: SID [7:0] LCD module’s manufacturer ID.																																																																									
	Parameter 3: SID [15:8] LCD module/driver version ID.																																																																									
	Parameter 4: MRID [7:0] LCD module/driver ID.																																																																									
	Parameter 5: MRID [15:8] IC version code.																																																																									
	Parameter 6: FFh - Exit code – there is no more data in the Descriptor Block																																																																									
	This read sequence can be interrupted by any command and it can be continued by the Read DDB Continue (A8h) command.																																																																									
Restriction	For example, RDDDBS => 1 st parameter has been sent => 2 nd parameter has been sent => interrupt => RDDDBC => 3 rd parameter of the RDDDBS has been sent.																																																																									
	Register Availability	<table><tr><th colspan="8">Status</th><th colspan="2">Availability</th></tr><tr><td colspan="8">Normal Mode On, Idle Mode Off, Sleep Out</td><td colspan="2">Yes</td></tr><tr><td colspan="8">Normal Mode On, Idle Mode On, Sleep Out</td><td colspan="2">Yes</td></tr><tr><td colspan="8">Partial Mode On, Idle Mode Off, Sleep Out</td><td colspan="2">Yes</td></tr><tr><td colspan="8">Partial Mode On, Idle Mode On, Sleep Out</td><td colspan="2">Yes</td></tr><tr><td colspan="8">Sleep In</td><td colspan="2">Yes</td></tr></table>													Status								Availability		Normal Mode On, Idle Mode Off, Sleep Out								Yes		Normal Mode On, Idle Mode On, Sleep Out								Yes		Partial Mode On, Idle Mode Off, Sleep Out								Yes		Partial Mode On, Idle Mode On, Sleep Out								Yes		Sleep In								Yes	
		Status								Availability																																																																
		Normal Mode On, Idle Mode Off, Sleep Out								Yes																																																																
		Normal Mode On, Idle Mode On, Sleep Out								Yes																																																																
		Partial Mode On, Idle Mode Off, Sleep Out								Yes																																																																
		Partial Mode On, Idle Mode On, Sleep Out								Yes																																																																
Sleep In								Yes																																																																		
Default																																																																										
	<table><tr><th rowspan="2">Status</th><th colspan="12">Default Value</th></tr><tr><th colspan="2">SID [7:0]</th><th colspan="2">SID [15:8]</th><th colspan="2">MRID [7:0]</th><th colspan="2">MRID [15:8]</th></tr><tr><td>Power On Sequence</td><td colspan="2">00h</td><td colspan="2">00h</td><td colspan="2">00h</td><td colspan="2">00h</td></tr><tr><td>S/W Reset</td><td colspan="2">00h</td><td colspan="2">00h</td><td colspan="2">00h</td><td colspan="2">00h</td></tr><tr><td>H/W Reset</td><td colspan="2">00h</td><td colspan="2">00h</td><td colspan="2">00h</td><td colspan="2">00h</td></tr></table>													Status	Default Value												SID [7:0]		SID [15:8]		MRID [7:0]		MRID [15:8]		Power On Sequence	00h		00h		00h		00h		S/W Reset	00h		00h		00h		00h		H/W Reset	00h		00h		00h		00h														
	Status	Default Value																																																																								
		SID [7:0]		SID [15:8]		MRID [7:0]		MRID [15:8]																																																																		
	Power On Sequence	00h		00h		00h		00h																																																																		
S/W Reset	00h		00h		00h		00h																																																																			
H/W Reset	00h		00h		00h		00h																																																																			



4.2.68. Read DDB Continue (A8h)

A8h	RDDDBC (Read DDB Continue)																								
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	1	0	1	0	1	0	0	0	A8h												
1 st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	XX												
2 nd Parameter	1	↑	1	XX	D1 [7:0]								XX												
:	1	↑	1	XX	Dx [7:0]								XX												
N th Parameter	1	↑	1	XX	Dn [7:0]								XX												
Description	This command is used to read the supplier’s identification and revision information from the point where RDDDBS (A1h) was interrupted by another command.																								
Restriction	-																								
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power ON Sequence</td><td>XXh</td></tr><tr><td>S/W Reset</td><td>XXh</td></tr><tr><td>H/W Reset</td><td>XXh</td></tr></table>													Status	Default Value	Power ON Sequence	XXh	S/W Reset	XXh	H/W Reset	XXh				
Status	Default Value																								
Power ON Sequence	XXh																								
S/W Reset	XXh																								
H/W Reset	XXh																								
Flow Chart	<div><div><div>RDDDBC(A8h)</div><div>Host</div><div>Driver</div><div>RDDDBS Data D1[7:0], D2[7:0],...Dn[7:0],</div></div><div><div>Legend</div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>																								

4.2.69. Read First Checksum (AAh)

AAh	RDFCS (Read First Checksum)																								
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	1	0	1	0	1	0	1	0	AAh												
1 st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	XX												
2 nd Parameter	1	↑	1	XX	FCS [7:0]							XX													
Description	This command reads the first checksum calculated from registers of the User’s area and the Frame Memory after the write access to those registers and/or Frame Memory has been done. X = void																								
Restriction	It is necessary to wait 150ms after the last write access to registers on the User area before this checksum value can be read. The ILI9806G sends the 2 nd parameter value to the data lines if the MPU wants to read more than one parameter (= more than 2 RDX cycle) on the parallel MPU interface. Only the 2 nd parameter is sent on the DSI; the 1 st parameter is not sent.																								
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>00h</td></tr><tr><td>S/W Reset</td><td>00h</td></tr><tr><td>H/W Reset</td><td>00h</td></tr></table>													Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h				
Status	Default Value																								
Power On Sequence	00h																								
S/W Reset	00h																								
H/W Reset	00h																								
Flow Chart	<div><div><div>RDFCS(AAh)</div><div>↓</div><div>Send 1st Parameter</div><div>↓</div><div>Send FCS[7:0]</div></div><div>Host Driver</div><div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div></div>																								

4.2.70. Read Continue Checksum (AFh)

AFh	RDCFCS (Read Continue Checksum)																								
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	1	0	1	0	1	1	1	1	AFh												
1 st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	XX												
2 nd Parameter	1	↑	1	XX	CCS [7:0]							XX													
Description	This command reads the following checksum that is calculated continuously after the first checksum from registers of the User's area and the Frame Memory after the write access to those registers and/or Frame Memory is done. X = void																								
Restriction	It is necessary to wait 300ms after the last write access to registers of the User's area before this checksum value can be read the first time. The ILI9806G sends the 2 nd parameter value to the data lines if the MPU wants to read more than one parameter (= more than 2 RDX cycle) on the parallel MPU interface. Only the 2 nd parameter is sent on the DSI; the 1 st parameter is not sent.																								
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>00h</td></tr><tr><td>S/W Reset</td><td>00h</td></tr><tr><td>H/W Reset</td><td>00h</td></tr></table>													Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h				
Status	Default Value																								
Power On Sequence	00h																								
S/W Reset	00h																								
H/W Reset	00h																								
Flow Chart	<div><div><div>RDCCS(AFh)</div><div>↓</div><div>Send 1st Parameter</div><div>↓</div><div>Send CCS[7:0]</div></div><div>Host ----- Driver</div><div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div></div>																								

4.2.71. Read Device Code (D3h)

D3h	Read Device Code																								
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	1	1	0	1	0	0	1	1	D3h												
1 st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	XX												
2 nd Parameter	1	↑	1	XX	0	0	0	0	0	0	0	0	00h												
3 rd Parameter	1	↑	1	XX	1	0	0	1	1	0	0	0	98h												
4 th Parameter	1	↑	1	XX	0	0	0	0	0	1	1	0	06h												
Description	Read IC device code.																								
	The 1 st parameter is a dummy data																								
	The 2 nd parameter is reserved for future use.																								
	The 3 rd and 4 th parameters indicate the IC model name.																								
	X=void																								
Restriction	To enable this command, EXTC Command Set Enable Register (FFh) must be set first.																								
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power ON Sequence</td><td>24'h009806</td></tr><tr><td>S/W Reset</td><td>24'h009806</td></tr><tr><td>H/W Reset</td><td>24'h009806</td></tr></table>													Status	Default Value	Power ON Sequence	24'h009806	S/W Reset	24'h009806	H/W Reset	24'h009806				
Status	Default Value																								
Power ON Sequence	24'h009806																								
S/W Reset	24'h009806																								
H/W Reset	24'h009806																								

4.2.72. Read ID1 (DAh)

DBh	RDID1 (Read ID1)																								
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	1	1	0	1	1	0	1	0	DAh												
1 st parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	XX												
2 nd parameter	1	↑	1	XX	ID1 [7:0]								XX												
Description	<p>This read byte is used to track the LCD module/driver version. It is defined by the display supplier (with User’s agreement) and changes each time a revision is made to the display, material or construction specifications.</p> <p>The 1st parameter is a dummy data.</p> <p>The 2nd parameter is the LCD module/driver’s version ID. The ID parameter range is from 80h to FFh.</p> <p>The ID2 is programmed by the OTP function.</p> <p>X = Void</p>																								
Restriction	<p>The ILI9806G sends the 2nd parameter value to the data lines if the MPU wants to read more than one parameter (= more than 2 RDX cycle) on the parallel MPU interface.</p> <p>Only the 2nd parameter is sent on the DSI; the 1st parameter is not sent.</p>																								
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><tr><th>Status</th><th>Default Value (Before OTP program)</th><th>Default Value (After OTP program)</th></tr><tr><td>Power On Sequence</td><td>00h</td><td>OTP value</td></tr><tr><td>H/W Reset</td><td>00h</td><td>OTP value</td></tr></table>													Status	Default Value (Before OTP program)	Default Value (After OTP program)	Power On Sequence	00h	OTP value	H/W Reset	00h	OTP value			
Status	Default Value (Before OTP program)	Default Value (After OTP program)																							
Power On Sequence	00h	OTP value																							
H/W Reset	00h	OTP value																							
Flow Chart	<div><div><div><div>RDID1(DAh)</div><div>↓</div><div>1st Parameter: Dummy Read</div><div>↓</div><div>2nd Parameter: Send ID1[7:0]</div></div><div>Host Driver</div></div><div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div></div>																								

4.2.73. Read ID2 (DBh)

DBh	RDID2 (Read ID2)																								
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	1	1	0	1	1	0	1	1	DBh												
1 st parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	XX												
2 nd parameter	1	↑	1	XX	ID2 [7:0]								XX												
Description	<p>This read byte is used to track the LCD module/driver version. It is defined by the display supplier (with User’s agreement) and changes each time a revision is made to the display, material or construction specifications.</p> <p>The 1st parameter is a dummy data.</p> <p>The 2nd parameter is the LCD module/driver’s version ID. The ID parameter range is from 80h to FFh.</p> <p>The ID2 is programmed by the OTP function.</p> <p>X = Void</p>																								
Restriction	<p>The ILI9806G sends the 2nd parameter value to the data lines if the MPU wants to read more than one parameter (= more than 2 RDX cycle) on the parallel MPU interface.</p> <p>Only the 2nd parameter is sent on the DSI; the 1st parameter is not sent.</p>																								
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><tr><th>Status</th><th>Default Value (Before OTP program)</th><th>Default Value (After OTP program)</th></tr><tr><td>Power On Sequence</td><td>80h</td><td>OTP value</td></tr><tr><td>H/W Reset</td><td>80h</td><td>OTP value</td></tr></table>													Status	Default Value (Before OTP program)	Default Value (After OTP program)	Power On Sequence	80h	OTP value	H/W Reset	80h	OTP value			
Status	Default Value (Before OTP program)	Default Value (After OTP program)																							
Power On Sequence	80h	OTP value																							
H/W Reset	80h	OTP value																							
Flow Chart	<div><div><div>RDID2(DBh)</div><div>↓</div><div>1st Parameter: Dummy Read</div><div>↓</div><div>2nd Parameter: Send ID2 [7:0]</div></div><div><div>Host</div><div>Driver</div></div><div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div></div>																								

4.2.74. Read ID3 (DCh)

DCh	RDID3 (Read ID3)																								
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	1	1	0	1	1	1	0	0	DCh												
1 st parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	XX												
2 nd parameter	1	↑	1	XX	ID3 [7:0]							XX													
Description	<p>This read byte identifies the LCD module/driver. It is specified by users.</p> <p>The 1st parameter is a dummy data.</p> <p>The 2nd parameter is the LCD module/driver's ID.</p> <p>The ID3 is programmed by the OTP function.</p> <p>X = Void</p>																								
Restriction	<p>The ILI9806G sends the 2nd parameter value to the data lines if the MPU wants to read more than one parameter (= more than 2 RDX cycle) on the parallel MPU interface.</p> <p>Only the 2nd parameter is sent on the DSI; the 1st parameter is not sent.</p>																								
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><tr><th>Status</th><th>Default Value (Before OTP program)</th><th>Default Value (After OTP program)</th></tr><tr><td>Power On Sequence</td><td>00h</td><td>OTP value</td></tr><tr><td>H/W Reset</td><td>00h</td><td>OTP value</td></tr></table>													Status	Default Value (Before OTP program)	Default Value (After OTP program)	Power On Sequence	00h	OTP value	H/W Reset	00h	OTP value			
Status	Default Value (Before OTP program)	Default Value (After OTP program)																							
Power On Sequence	00h	OTP value																							
H/W Reset	00h	OTP value																							
Flow Chart	<div><div><div>RDID3(DCh)</div><div>↓</div><div>1st Parameter: Dummy Read</div><div>↓</div><div>2nd Parameter: Send ID3 [7:0]</div></div><div><div>Host Driver</div></div><div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div></div>																								

4.3. Extend Command (EXTC) Description

4.3.1. Interface Mode Control (B0h)

B0h	IFMODE (Interface Mode Control)																																				
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX																								
Command	0	1	↑	XX	1	0	1	1	0	0	0	0	B0h																								
1 st Parameter	1	1	↑	XX	0	0	0	0	VSPL	HSPL	DPL	EPL	00																								
Description	Sets the operation status of the RGB interface. The setting becomes effective as soon as the command is received. EPL : Enable polarity (0 = Low level enable, 1 = High level enable) DPL : DCK polarity set (0 = data latched at the rising edge, 1 = data latched at the falling edge) HSPL : HSYNC polarity (0 = Low pulse active, 1 = High pulse active) VSPL : VSYNC polarity (0 = Low pulse active, 1 = High pulse active)																																				
Restriction	To enable this command, EXTC Command Set Enable Register (FFh) must be set first.																																				
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes												
Status	Availability																																				
Normal Mode On, Idle Mode Off, Sleep Out	Yes																																				
Normal Mode On, Idle Mode On, Sleep Out	Yes																																				
Partial Mode On, Idle Mode Off, Sleep Out	Yes																																				
Partial Mode On, Idle Mode On, Sleep Out	Yes																																				
Sleep In	Yes																																				
Default	<table><tr><th rowspan="2">Status</th><th colspan="4">Default Value</th></tr><tr><th>EPL</th><th>DPL</th><th>HSPL</th><th>VSPL</th></tr><tr><td>Power ON Sequence</td><td>1'b0</td><td>1'b0</td><td>1'b0</td><td>1'b0</td></tr><tr><td>S/W Reset</td><td>1'b0</td><td>1'b0</td><td>1'b0</td><td>1'b0</td></tr><tr><td>H/W Reset</td><td>1'b0</td><td>1'b0</td><td>1'b0</td><td>1'b0</td></tr></table>													Status	Default Value				EPL	DPL	HSPL	VSPL	Power ON Sequence	1'b0	1'b0	1'b0	1'b0	S/W Reset	1'b0	1'b0	1'b0	1'b0	H/W Reset	1'b0	1'b0	1'b0	1'b0
Status	Default Value																																				
	EPL	DPL	HSPL	VSPL																																	
Power ON Sequence	1'b0	1'b0	1'b0	1'b0																																	
S/W Reset	1'b0	1'b0	1'b0	1'b0																																	
H/W Reset	1'b0	1'b0	1'b0	1'b0																																	

4.3.2. Frame Rate Control 1 (In Normal Mode/Full Colors) (B1h)

B1h	FRMCTR1 (Frame Rate Control In Normal Mode)																																																																																																																																																												
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																																																																																																																
Command	0	1	↑	XX	1	0	1	1	0	0	0	1	B1h																																																																																																																																																
1 st parameter	1	1	↑	XX	0	0	0	0	0	0	DIVA[1:0]		00																																																																																																																																																
2 nd parameter	1	1	↑	XX	0	0	0	RTNA [4:0]						10																																																																																																																																															
3 rd parameter	1	1	↑	XX	0	0	FRSA [5:0]						14																																																																																																																																																
Description	Sets the division ratio for internal clocks of the Normal Display Mode On																																																																																																																																																												
	<div>Frame Rate=$\frac{\text{Fosc}}{(\text{DIVA} \times (\text{FRSA} + 1)) \times \text{RTNA} \times (\text{Display Line} + \text{VBP} + \text{VFP})}$</div>																																																																																																																																																												
	Fosc: Internal oscillator frequency																																																																																																																																																												
	DIVA: Division Ratio																																																																																																																																																												
	FRSA: Frame rate setting																																																																																																																																																												
	RTNA: Clocks per line																																																																																																																																																												
	Display Line: Total driving line number																																																																																																																																																												
	VBP: Back porch line number																																																																																																																																																												
	VFP: Front porch line number																																																																																																																																																												
	Note: If “VBP+VFP” < 60 or = 60, The “VBP+VFP” data of the frame rate calculation formula = 60.																																																																																																																																																												
	If “VBP+VFP” > 60 , The “VBP+VFP” data of the frame rate calculation formula = “VBP+VFP” real data.																																																																																																																																																												
	<table><tr><th colspan="6">FRSA [5:0]</th><th>Decimal</th><th>Frame rate (Hz)</th></tr><tr><td colspan="6">000000~010001</td><td>0~17</td><td>Setting prohibited</td></tr><tr><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>18</td><td>75.19</td></tr><tr><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>19</td><td>71.43</td></tr><tr><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>20</td><td>68.03</td></tr><tr><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>21</td><td>64.94</td></tr><tr><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>22</td><td>62.11</td></tr><tr><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>23</td><td>59.52</td></tr><tr><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>24</td><td>57.14</td></tr><tr><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>25</td><td>54.95</td></tr><tr><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>26</td><td>52.91</td></tr><tr><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>27</td><td>51.02</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>28</td><td>49.26</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>29</td><td>47.62</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>30</td><td>46.08</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>31</td><td>44.64</td></tr><tr><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>32</td><td>43.29</td></tr><tr><td colspan="6">100001~111111</td><td>33~63</td><td>Setting prohibited</td></tr></table>													FRSA [5:0]						Decimal	Frame rate (Hz)	000000~010001						0~17	Setting prohibited	0	1	0	0	1	0	18	75.19	0	1	0	0	1	1	19	71.43	0	1	0	1	0	0	20	68.03	0	1	0	1	0	1	21	64.94	0	1	0	1	1	0	22	62.11	0	1	0	1	1	1	23	59.52	0	1	1	0	0	0	24	57.14	0	1	1	0	0	1	25	54.95	0	1	1	0	1	0	26	52.91	0	1	1	0	1	1	27	51.02	0	1	1	1	0	0	28	49.26	0	1	1	1	0	1	29	47.62	0	1	1	1	1	0	30	46.08	0	1	1	1	1	1	31	44.64	1	0	0	0	0	0	32	43.29	100001~111111						33~63	Setting prohibited
	FRSA [5:0]						Decimal	Frame rate (Hz)																																																																																																																																																					
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100001~111111						33~63	Setting prohibited																																																																																																																																																						
Frame rate calculation example:																																																																																																																																																													
Fosc = 18MHz, DIVA = 1, FRSA = 20, RTNA = 15 clock, Display Line = 800lines, VBP = VFP = 20lines.																																																																																																																																																													
Following the formula, the frame rate = 67.04Hz.																																																																																																																																																													

	<div>DIVA [1:0]: division ratio for internal clocks for the Normal Display Mode On.</div> <table><tr><th colspan="2">DIVA [1:0]</th><th>Division Ratio</th></tr><tr><td>0</td><td>0</td><td>fosc</td></tr><tr><td>0</td><td>1</td><td>fosc/2</td></tr><tr><td>1</td><td>0</td><td>fosc/4</td></tr><tr><td>1</td><td>1</td><td>fosc/8</td></tr></table> <div>RTNA [4:0]: RTNA [4:0] is used to set 1H (line) period for the Normal Display Mode On.</div> <table><tr><th colspan="5">RTNA [4:0]</th><th>Clock per Line</th></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>Setting prohibited</td></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>Setting prohibited</td></tr><tr><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>Setting prohibited</td></tr><tr><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>Setting prohibited</td></tr><tr><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>Setting prohibited</td></tr><tr><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>Setting prohibited</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>Setting prohibited</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>Setting prohibited</td></tr><tr><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>Setting prohibited</td></tr><tr><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>Setting prohibited</td></tr><tr><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>Setting prohibited</td></tr><tr><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>Setting prohibited</td></tr></table> <table><tr><th colspan="5">RTNA [4:0]</th><th>Clock per Line</th></tr><tr><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>Setting prohibited</td></tr><tr><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>Setting prohibited</td></tr><tr><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>12 clocks</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>13 clocks</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>14 clocks</td></tr><tr><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>15 clocks</td></tr><tr><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>16 clocks</td></tr><tr><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>17 clocks</td></tr><tr><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>18 clocks</td></tr><tr><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>19 clocks</td></tr><tr><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>20 clocks</td></tr></table> <table><tr><th colspan="5">RTNA [4:0]</th><th>Clock per Line</th></tr><tr><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>21 clocks</td></tr><tr><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>22 clocks</td></tr><tr><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>23 clocks</td></tr><tr><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>24 clocks</td></tr><tr><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>25 clocks</td></tr><tr><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>26 clocks</td></tr><tr><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>27 clocks</td></tr><tr><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>28 clocks</td></tr><tr><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>29 clocks</td></tr><tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>30 clocks</td></tr></table>	DIVA [1:0]		Division Ratio	0	0	fosc	0	1	fosc/2	1	0	fosc/4	1	1	fosc/8	RTNA [4:0]					Clock per Line	0	0	0	0	0	Setting prohibited	0	0	0	0	1	Setting prohibited	0	0	0	1	0	Setting prohibited	0	0	0	1	1	Setting prohibited	0	0	1	0	0	Setting prohibited	0	0	1	0	1	Setting prohibited	0	0	1	1	0	Setting prohibited	0	0	1	1	1	Setting prohibited	0	1	0	0	0	Setting prohibited	0	1	0	0	1	Setting prohibited	0	1	0	1	0	Setting prohibited	0	1	0	1	1	Setting prohibited	RTNA [4:0]					Clock per Line	0	1	0	1	1	Setting prohibited	0	1	1	0	0	Setting prohibited	0	1	1	0	1	12 clocks	0	1	1	1	0	13 clocks	0	1	1	1	1	14 clocks	1	0	0	0	0	15 clocks	1	0	0	0	1	16 clocks	1	0	0	1	0	17 clocks	1	0	0	1	1	18 clocks	1	0	1	0	0	19 clocks	1	0	1	0	1	20 clocks	RTNA [4:0]					Clock per Line	1	0	1	1	0	21 clocks	1	0	1	1	1	22 clocks	1	1	0	0	0	23 clocks	1	1	0	0	1	24 clocks	1	1	0	1	0	25 clocks	1	1	0	1	1	26 clocks	1	1	1	0	0	27 clocks	1	1	1	0	1	28 clocks	1	1	1	1	0	29 clocks	1	1	1	1	1	30 clocks
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4.3.3. Frame Rate Control 2 (In Idle Mode/8 colors) (B2h)

B2h	FRMCTR2 (Frame Rate Control In Idle Mode)																																																																																																																																																												
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																																																																																																																
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Description	Sets the division ratio for internal clocks of the Idle Mode On																																																																																																																																																												
	<div>Frame Rate=$\frac{\text{Fosc}}{(\text{DIVB} \times (\text{FRSB} + 1)) \times \text{RTNB} \times (\text{Display Line} + \text{VBP} + \text{VFP})}$</div>																																																																																																																																																												
	Fosc: Internal oscillator frequency																																																																																																																																																												
	DIVB: Division Ratio																																																																																																																																																												
	FRSB: Frame rate setting																																																																																																																																																												
	RTNB: Clocks per line																																																																																																																																																												
	Display Line: Total driving line number																																																																																																																																																												
	VBP: Back porch line number																																																																																																																																																												
	VFP: Front porch line number																																																																																																																																																												
	Note: If “VBP+VFP” < 60 or = 60, The “VBP+VFP” data of the frame rate calculation formula = 60.																																																																																																																																																												
	If “VBP+VFP” > 60 , The “VBP+VFP” data of the frame rate calculation formula = “VBP+VFP” real data.																																																																																																																																																												
	<table><thead><tr><th colspan="6">FRSB [5:0]</th><th>Decimal</th><th>Frame rate (Hz)</th></tr></thead><tbody><tr><td colspan="6">000000~010001</td><td>0~17</td><td>Setting prohibited</td></tr><tr><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>18</td><td>75.19</td></tr><tr><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>19</td><td>71.43</td></tr><tr><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>20</td><td>68.03</td></tr><tr><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>21</td><td>64.94</td></tr><tr><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>22</td><td>62.11</td></tr><tr><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>23</td><td>59.52</td></tr><tr><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>24</td><td>57.14</td></tr><tr><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>25</td><td>54.95</td></tr><tr><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>26</td><td>52.91</td></tr><tr><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>27</td><td>51.02</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>28</td><td>49.26</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>29</td><td>47.62</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>30</td><td>46.08</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>31</td><td>44.64</td></tr><tr><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>32</td><td>43.29</td></tr><tr><td colspan="6">100001~111111</td><td>33~63</td><td>Setting prohibited</td></tr></tbody></table>													FRSB [5:0]						Decimal	Frame rate (Hz)	000000~010001						0~17	Setting prohibited	0	1	0	0	1	0	18	75.19	0	1	0	0	1	1	19	71.43	0	1	0	1	0	0	20	68.03	0	1	0	1	0	1	21	64.94	0	1	0	1	1	0	22	62.11	0	1	0	1	1	1	23	59.52	0	1	1	0	0	0	24	57.14	0	1	1	0	0	1	25	54.95	0	1	1	0	1	0	26	52.91	0	1	1	0	1	1	27	51.02	0	1	1	1	0	0	28	49.26	0	1	1	1	0	1	29	47.62	0	1	1	1	1	0	30	46.08	0	1	1	1	1	1	31	44.64	1	0	0	0	0	0	32	43.29	100001~111111						33~63	Setting prohibited
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Frame rate calculation example:																																																																																																																																																													
Fosc = 18MHz, DIVB = 1, FRSB = 20, RTNB = 15 clock, Display Line = 800lines, VBP = VFP = 20lines.																																																																																																																																																													
Following the formula, the frame rate = 67.04Hz.																																																																																																																																																													

	<div>DIVB [1:0]: division ratio for internal clocks for the Idle Mode On.</div> <table><tr><th colspan="2">DIVB [1:0]</th><th>Division Ratio</th></tr><tr><td>0</td><td>0</td><td>fosc</td></tr><tr><td>0</td><td>1</td><td>fosc/2</td></tr><tr><td>1</td><td>0</td><td>fosc/4</td></tr><tr><td>1</td><td>1</td><td>fosc/8</td></tr></table> <div>RTNB [4:0]: RTNB [4:0] is used to set 1H (line) period for the Idle Mode On.</div> <table><tr><th colspan="5">RTNB [4:0]</th><th>Clock per Line</th></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>Setting prohibited</td></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>Setting prohibited</td></tr><tr><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>Setting prohibited</td></tr><tr><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>Setting prohibited</td></tr><tr><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>Setting prohibited</td></tr><tr><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>Setting prohibited</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>Setting prohibited</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>Setting prohibited</td></tr><tr><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>Setting prohibited</td></tr><tr><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>Setting prohibited</td></tr><tr><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>Setting prohibited</td></tr></table> <table><tr><th colspan="5">RTNB [4:0]</th><th>Clock per Line</th></tr><tr><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>Setting prohibited</td></tr><tr><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>Setting prohibited</td></tr><tr><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>12 clocks</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>13 clocks</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>14 clocks</td></tr><tr><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>15 clocks</td></tr><tr><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>16 clocks</td></tr><tr><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>17 clocks</td></tr><tr><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>18 clocks</td></tr><tr><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>19 clocks</td></tr><tr><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>20 clocks</td></tr></table> <table><tr><th colspan="5">RTNB [4:0]</th><th>Clock per Line</th></tr><tr><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>21 clocks</td></tr><tr><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>22 clocks</td></tr><tr><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>23 clocks</td></tr><tr><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>24 clocks</td></tr><tr><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>25 clocks</td></tr><tr><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>26 clocks</td></tr><tr><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>27 clocks</td></tr><tr><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>28 clocks</td></tr><tr><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>29 clocks</td></tr><tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>30 clocks</td></tr></table>	DIVB [1:0]		Division Ratio	0	0	fosc	0	1	fosc/2	1	0	fosc/4	1	1	fosc/8	RTNB [4:0]					Clock per Line	0	0	0	0	0	Setting prohibited	0	0	0	0	1	Setting prohibited	0	0	0	1	0	Setting prohibited	0	0	0	1	1	Setting prohibited	0	0	1	0	0	Setting prohibited	0	0	1	0	1	Setting prohibited	0	0	1	1	0	Setting prohibited	0	0	1	1	1	Setting prohibited	0	1	0	0	0	Setting prohibited	0	1	0	0	1	Setting prohibited	0	1	0	1	0	Setting prohibited	RTNB [4:0]					Clock per Line	0	1	0	1	1	Setting prohibited	0	1	1	0	0	Setting prohibited	0	1	1	0	1	12 clocks	0	1	1	1	0	13 clocks	0	1	1	1	1	14 clocks	1	0	0	0	0	15 clocks	1	0	0	0	1	16 clocks	1	0	0	1	0	17 clocks	1	0	0	1	1	18 clocks	1	0	1	0	0	19 clocks	1	0	1	0	1	20 clocks	RTNB [4:0]					Clock per Line	1	0	1	1	0	21 clocks	1	0	1	1	1	22 clocks	1	1	0	0	0	23 clocks	1	1	0	0	1	24 clocks	1	1	0	1	0	25 clocks	1	1	0	1	1	26 clocks	1	1	1	0	0	27 clocks	1	1	1	0	1	28 clocks	1	1	1	1	0	29 clocks	1	1	1	1	1	30 clocks
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Default	<table><tr><th rowspan="2">Status</th><th colspan="3">Default Value</th></tr><tr><th>DIVB [1:0]</th><th>RTNB [4:0]</th><th>FRSB [5:0]</th></tr><tr><td>Power ON Sequence</td><td>2'b00</td><td>5'b10000</td><td>6'b010100</td></tr><tr><td>S/W Reset</td><td>2'b00</td><td>5'b10000</td><td>6'b010100</td></tr><tr><td>H/W Reset</td><td>2'b00</td><td>5'b10000</td><td>6'b010100</td></tr></table>	Status	Default Value			DIVB [1:0]	RTNB [4:0]	FRSB [5:0]	Power ON Sequence	2'b00	5'b10000	6'b010100	S/W Reset	2'b00	5'b10000	6'b010100	H/W Reset	2'b00	5'b10000	6'b010100																																																																																																																																																																																																														
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H/W Reset	2'b00	5'b10000	6'b010100																																																																																																																																																																																																																															

4.3.4. Frame Rate control 3 (In Partial Mode/Full Colors) (B3h)

B3h	FRMCTR3 (Frame Rate Control In Partial Mode)																																																																																																																																																												
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																																																																																																																
Command	0	1	↑	XX	1	0	1	1	0	0	1	1	B3h																																																																																																																																																
1 st parameter	1	1	↑	XX	0	0	0	0	0	0	DIVC[1:0]		00																																																																																																																																																
2 nd parameter	1	1	↑	XX	0	0	0	RTNC [4:0]						10																																																																																																																																															
3 rd parameter	1	1	↑	XX	0	0	FRSC [5:0]						14																																																																																																																																																
Description	Sets the division ratio for internal clocks of Partial Mode On.																																																																																																																																																												
	<div>Frame Rate=$\frac{Fosc}{(DIVCx(FRSC+1)) \times RTNC \times (Display\ Line+VBP+VFP)}$</div>																																																																																																																																																												
	Fosc: Internal oscillator frequency																																																																																																																																																												
	DIVC: Division Ratio																																																																																																																																																												
	FRSC: Frame rate setting																																																																																																																																																												
	RTNC: Clocks per line																																																																																																																																																												
	Display Line: Total driving line number																																																																																																																																																												
	VBP: Back porch line number																																																																																																																																																												
	VFP: Front porch line number																																																																																																																																																												
	Note: If “VBP+VFP” < 60 or = 60, The “VBP+VFP” data of the frame rate calculation formula = 60.																																																																																																																																																												
	If “VBP+VFP” > 60 , The “VBP+VFP” data of the frame rate calculation formula = “VBP+VFP” real data.																																																																																																																																																												
	<table><thead><tr><th colspan="6">FRSC [5:0]</th><th>Decimal</th><th>Frame rate (Hz)</th></tr></thead><tbody><tr><td colspan="6">000000~010001</td><td>0~17</td><td>Setting prohibited</td></tr><tr><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>18</td><td>75.19</td></tr><tr><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>19</td><td>71.43</td></tr><tr><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>20</td><td>68.03</td></tr><tr><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>21</td><td>64.94</td></tr><tr><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>22</td><td>62.11</td></tr><tr><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>23</td><td>59.52</td></tr><tr><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>24</td><td>57.14</td></tr><tr><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>25</td><td>54.95</td></tr><tr><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>26</td><td>52.91</td></tr><tr><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>27</td><td>51.02</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>28</td><td>49.26</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>29</td><td>47.62</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>30</td><td>46.08</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>31</td><td>44.64</td></tr><tr><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>32</td><td>43.29</td></tr><tr><td colspan="6">100001~111111</td><td>33~63</td><td>Setting prohibited</td></tr></tbody></table>													FRSC [5:0]						Decimal	Frame rate (Hz)	000000~010001						0~17	Setting prohibited	0	1	0	0	1	0	18	75.19	0	1	0	0	1	1	19	71.43	0	1	0	1	0	0	20	68.03	0	1	0	1	0	1	21	64.94	0	1	0	1	1	0	22	62.11	0	1	0	1	1	1	23	59.52	0	1	1	0	0	0	24	57.14	0	1	1	0	0	1	25	54.95	0	1	1	0	1	0	26	52.91	0	1	1	0	1	1	27	51.02	0	1	1	1	0	0	28	49.26	0	1	1	1	0	1	29	47.62	0	1	1	1	1	0	30	46.08	0	1	1	1	1	1	31	44.64	1	0	0	0	0	0	32	43.29	100001~111111						33~63	Setting prohibited
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100001~111111						33~63	Setting prohibited																																																																																																																																																						
Frame rate calculation example:																																																																																																																																																													
Fosc = 18MHz, DIVC = 1, FRSC = 20, RTNC = 15 clock, Display Line = 800lines, VBP = VFP = 20lines.																																																																																																																																																													
Following the formula, the frame rate = 67.04Hz.																																																																																																																																																													

	<div>DIVC [1:0]: division ratio for internal clocks for the Partial Mode On</div> <table><tr><th colspan="2">DIVC [1:0]</th><th>Division Ratio</th></tr><tr><td>0</td><td>0</td><td>fosc</td></tr><tr><td>0</td><td>1</td><td>fosc/2</td></tr><tr><td>1</td><td>0</td><td>fosc/4</td></tr><tr><td>1</td><td>1</td><td>fosc/8</td></tr></table> <div>RTNC [4:0]: RTNC [4:0] is used to set 1H (line) period for the Partial Mode On.</div> <table><tr><th colspan="5">RTNC [4:0]</th><th>Clock per Line</th></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>Setting prohibited</td></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>Setting prohibited</td></tr><tr><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>Setting prohibited</td></tr><tr><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>Setting prohibited</td></tr><tr><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>Setting prohibited</td></tr><tr><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>Setting prohibited</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>Setting prohibited</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>Setting prohibited</td></tr><tr><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>Setting prohibited</td></tr><tr><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>Setting prohibited</td></tr><tr><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>Setting prohibited</td></tr><tr><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>Setting prohibited</td></tr></table> <table><tr><th colspan="5">RTNC [4:0]</th><th>Clock per Line</th></tr><tr><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>Setting prohibited</td></tr><tr><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>Setting prohibited</td></tr><tr><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>12 clocks</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>13 clocks</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>14 clocks</td></tr><tr><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>15 clocks</td></tr><tr><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>16 clocks</td></tr><tr><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>17 clocks</td></tr><tr><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>18 clocks</td></tr><tr><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>19 clocks</td></tr><tr><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>20 clocks</td></tr></table> <table><tr><th colspan="5">RTNC [4:0]</th><th>Clock per Line</th></tr><tr><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>21 clocks</td></tr><tr><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>22 clocks</td></tr><tr><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>23 clocks</td></tr><tr><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>24 clocks</td></tr><tr><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>25 clocks</td></tr><tr><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>26 clocks</td></tr><tr><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>27 clocks</td></tr><tr><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>28 clocks</td></tr><tr><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>29 clocks</td></tr><tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>30 clocks</td></tr></table>	DIVC [1:0]		Division Ratio	0	0	fosc	0	1	fosc/2	1	0	fosc/4	1	1	fosc/8	RTNC [4:0]					Clock per Line	0	0	0	0	0	Setting prohibited	0	0	0	0	1	Setting prohibited	0	0	0	1	0	Setting prohibited	0	0	0	1	1	Setting prohibited	0	0	1	0	0	Setting prohibited	0	0	1	0	1	Setting prohibited	0	0	1	1	0	Setting prohibited	0	0	1	1	1	Setting prohibited	0	1	0	0	0	Setting prohibited	0	1	0	0	1	Setting prohibited	0	1	0	1	0	Setting prohibited	0	1	0	1	0	Setting prohibited	RTNC [4:0]					Clock per Line	0	1	0	1	1	Setting prohibited	0	1	1	0	0	Setting prohibited	0	1	1	0	1	12 clocks	0	1	1	1	0	13 clocks	0	1	1	1	1	14 clocks	1	0	0	0	0	15 clocks	1	0	0	0	1	16 clocks	1	0	0	1	0	17 clocks	1	0	0	1	1	18 clocks	1	0	1	0	0	19 clocks	1	0	1	0	1	20 clocks	RTNC [4:0]					Clock per Line	1	0	1	1	0	21 clocks	1	0	1	1	1	22 clocks	1	1	0	0	0	23 clocks	1	1	0	0	1	24 clocks	1	1	0	1	0	25 clocks	1	1	0	1	1	26 clocks	1	1	1	0	0	27 clocks	1	1	1	0	1	28 clocks	1	1	1	1	0	29 clocks	1	1	1	1	1	30 clocks
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Partial Mode On, Idle Mode On, Sleep Out	Yes																																																																																																																																																																																																																																							
Sleep In	Yes																																																																																																																																																																																																																																							
Default	<table><tr><th rowspan="2">Status</th><th colspan="3">Default Value</th></tr><tr><th>DIVC [1:0]</th><th>RTNC [4:0]</th><th>FRSC [5:0]</th></tr><tr><td>Power ON Sequence</td><td>2'b00</td><td>5'b10000</td><td>6'b010100</td></tr><tr><td>S/W Reset</td><td>2'b00</td><td>5'b10000</td><td>6'b010100</td></tr><tr><td>H/W Reset</td><td>2'b00</td><td>5'b10000</td><td>6'b010100</td></tr></table>					Status	Default Value			DIVC [1:0]	RTNC [4:0]	FRSC [5:0]	Power ON Sequence	2'b00	5'b10000	6'b010100	S/W Reset	2'b00	5'b10000	6'b010100	H/W Reset	2'b00	5'b10000	6'b010100																																																																																																																																																																																																																
Status	Default Value																																																																																																																																																																																																																																							
	DIVC [1:0]	RTNC [4:0]	FRSC [5:0]																																																																																																																																																																																																																																					
Power ON Sequence	2'b00	5'b10000	6'b010100																																																																																																																																																																																																																																					
S/W Reset	2'b00	5'b10000	6'b010100																																																																																																																																																																																																																																					
H/W Reset	2'b00	5'b10000	6'b010100																																																																																																																																																																																																																																					

4.3.5. Display Inversion Control (B4h)

_B4h		INVTR (Display Inversion Control)																																																																		
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																							
Command	0	1	↑	XX	1	0	1	1	0	1	0	0	B4h																																																							
1 st parameter	1	1	↑	XX	0	0	0	0	NLA [3:0]				00																																																							
2 nd parameter	1	1	↑	XX	0	0	0	0	NLB [3:0]				00																																																							
3 rd parameter	1	1	↑	XX	0	0	0	0	NLC [3:0]				00																																																							
Description	Set Display inversion mode																																																																			
	NLA [3:0]: Inversion setting in full colors normal mode (Normal Mode On)																																																																			
	NLB [3:0]: Inversion setting in Idle mode (Idle Mode On)																																																																			
	NLC [3:0]: Inversion setting in full colors partial mode (Partial Mode On/Idle Mode Off)																																																																			
	<table><tr><th colspan="4">NLA/NLB/NLC [3:0]</th><th>Inversion</th></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>Column inversion</td></tr><tr><td>0</td><td>0</td><td>0</td><td>1</td><td>1 dot inversion</td></tr><tr><td>0</td><td>0</td><td>1</td><td>0</td><td>2 dot inversion</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1</td><td>4 dot inversion</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1</td><td>3 dot inversion</td></tr></table>													NLA/NLB/NLC [3:0]				Inversion	0	0	0	0	Column inversion	0	0	0	1	1 dot inversion	0	0	1	0	2 dot inversion	0	0	1	1	4 dot inversion	0	1	1	1	3 dot inversion																									
	NLA/NLB/NLC [3:0]				Inversion																																																															
	0	0	0	0	Column inversion																																																															
	0	0	0	1	1 dot inversion																																																															
	0	0	1	0	2 dot inversion																																																															
	0	0	1	1	4 dot inversion																																																															
0	1	1	1	3 dot inversion																																																																
<p style="text-align: center;">Column Inversion</p> <div><div><p>1st frame</p><table><tr><td>1 line</td><td>+</td><td>-</td><td>+</td><td>-</td><td>+</td><td>-</td></tr><tr><td>2 line</td><td>+</td><td>-</td><td>+</td><td>-</td><td>+</td><td>-</td></tr><tr><td>3 line</td><td>+</td><td>-</td><td>+</td><td>-</td><td>+</td><td>-</td></tr><tr><td>4 line</td><td>+</td><td>-</td><td>+</td><td>-</td><td>+</td><td>-</td></tr></table></div><div>→</div><div><p>2nd frame</p><table><tr><td>1 line</td><td>-</td><td>+</td><td>-</td><td>+</td><td>-</td><td>+</td></tr><tr><td>2 line</td><td>-</td><td>+</td><td>-</td><td>+</td><td>-</td><td>+</td></tr><tr><td>3 line</td><td>-</td><td>+</td><td>-</td><td>+</td><td>-</td><td>+</td></tr><tr><td>4 line</td><td>-</td><td>+</td><td>-</td><td>+</td><td>-</td><td>+</td></tr></table></div></div>													1 line	+	-	+	-	+	-	2 line	+	-	+	-	+	-	3 line	+	-	+	-	+	-	4 line	+	-	+	-	+	-	1 line	-	+	-	+	-	+	2 line	-	+	-	+	-	+	3 line	-	+	-	+	-	+	4 line	-	+	-	+	-	+
1 line	+	-	+	-	+	-																																																														
2 line	+	-	+	-	+	-																																																														
3 line	+	-	+	-	+	-																																																														
4 line	+	-	+	-	+	-																																																														
1 line	-	+	-	+	-	+																																																														
2 line	-	+	-	+	-	+																																																														
3 line	-	+	-	+	-	+																																																														
4 line	-	+	-	+	-	+																																																														
<p style="text-align: center;">1-Dot Inversion</p> <div><div><p>1st frame</p><table><tr><td>1 line</td><td>+</td><td>-</td><td>+</td><td>-</td><td>+</td><td>-</td></tr><tr><td>2 line</td><td>-</td><td>+</td><td>-</td><td>+</td><td>-</td><td>+</td></tr><tr><td>3 line</td><td>+</td><td>-</td><td>+</td><td>-</td><td>+</td><td>-</td></tr><tr><td>4 line</td><td>-</td><td>+</td><td>-</td><td>+</td><td>-</td><td>+</td></tr></table></div><div>→</div><div><p>2nd frame</p><table><tr><td>1 line</td><td>-</td><td>+</td><td>-</td><td>+</td><td>-</td><td>+</td></tr><tr><td>2 line</td><td>+</td><td>-</td><td>+</td><td>-</td><td>+</td><td>-</td></tr><tr><td>3 line</td><td>-</td><td>+</td><td>-</td><td>+</td><td>-</td><td>+</td></tr><tr><td>4 line</td><td>+</td><td>-</td><td>+</td><td>-</td><td>+</td><td>-</td></tr></table></div></div>													1 line	+	-	+	-	+	-	2 line	-	+	-	+	-	+	3 line	+	-	+	-	+	-	4 line	-	+	-	+	-	+	1 line	-	+	-	+	-	+	2 line	+	-	+	-	+	-	3 line	-	+	-	+	-	+	4 line	+	-	+	-	+	-
1 line	+	-	+	-	+	-																																																														
2 line	-	+	-	+	-	+																																																														
3 line	+	-	+	-	+	-																																																														
4 line	-	+	-	+	-	+																																																														
1 line	-	+	-	+	-	+																																																														
2 line	+	-	+	-	+	-																																																														
3 line	-	+	-	+	-	+																																																														
4 line	+	-	+	-	+	-																																																														
<p style="text-align: center;">2-Dot Inversion</p> <div><div><p>1st frame</p><table><tr><td>1 line</td><td>+</td><td>-</td><td>+</td><td>-</td><td>+</td><td>-</td></tr><tr><td>2 line</td><td>+</td><td>-</td><td>+</td><td>-</td><td>+</td><td>-</td></tr><tr><td>3 line</td><td>-</td><td>+</td><td>-</td><td>+</td><td>-</td><td>+</td></tr><tr><td>4 line</td><td>-</td><td>+</td><td>-</td><td>+</td><td>-</td><td>+</td></tr></table></div><div>→</div><div><p>2nd frame</p><table><tr><td>1 line</td><td>-</td><td>+</td><td>-</td><td>+</td><td>-</td><td>+</td></tr><tr><td>2 line</td><td>-</td><td>+</td><td>-</td><td>+</td><td>-</td><td>+</td></tr><tr><td>3 line</td><td>+</td><td>-</td><td>+</td><td>-</td><td>+</td><td>-</td></tr><tr><td>4 line</td><td>+</td><td>-</td><td>+</td><td>-</td><td>+</td><td>-</td></tr></table></div></div>													1 line	+	-	+	-	+	-	2 line	+	-	+	-	+	-	3 line	-	+	-	+	-	+	4 line	-	+	-	+	-	+	1 line	-	+	-	+	-	+	2 line	-	+	-	+	-	+	3 line	+	-	+	-	+	-	4 line	+	-	+	-	+	-
1 line	+	-	+	-	+	-																																																														
2 line	+	-	+	-	+	-																																																														
3 line	-	+	-	+	-	+																																																														
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1 line	-	+	-	+	-	+																																																														
2 line	-	+	-	+	-	+																																																														
3 line	+	-	+	-	+	-																																																														
4 line	+	-	+	-	+	-																																																														

	<div><div>3-Dot Inversion</div><div><div><div>1st frame</div><div><div>1 line</div><div><div><div>+</div><div>-</div><div>+</div><div>-</div><div>+</div><div>-</div></div></div><div>2 line</div><div><div><div>+</div><div>-</div><div>+</div><div>-</div><div>+</div><div>-</div></div></div><div>3 line</div><div><div><div>+</div><div>-</div><div>+</div><div>-</div><div>+</div><div>-</div></div></div><div>4 line</div><div><div><div>-</div><div>+</div><div>-</div><div>+</div><div>-</div><div>+</div></div></div><div>5 line</div><div><div><div>-</div><div>+</div><div>-</div><div>+</div><div>-</div><div>+</div></div></div><div>6 line</div><div><div><div>-</div><div>+</div><div>-</div><div>+</div><div>-</div><div>+</div></div></div></div><div>→</div><div><div>2nd frame</div><div><div>1 line</div><div><div><div>-</div><div>+</div><div>-</div><div>+</div><div>-</div><div>+</div></div></div><div>2 line</div><div><div><div>-</div><div>+</div><div>-</div><div>+</div><div>-</div><div>+</div></div></div><div>3 line</div><div><div><div>-</div><div>+</div><div>-</div><div>+</div><div>-</div><div>+</div></div></div><div>4 line</div><div><div><div>+</div><div>-</div><div>+</div><div>-</div><div>+</div><div>-</div></div></div><div>5 line</div><div><div><div>+</div><div>-</div><div>+</div><div>-</div><div>+</div><div>-</div></div></div><div>6 line</div><div><div><div>+</div><div>-</div><div>+</div><div>-</div><div>+</div><div>-</div></div></div></div></div></div></div></div>												
	<div><div>4-Dot Inversion</div><div><div><div>1st frame</div><div><div>1 line</div><div><div><div>+</div><div>-</div><div>+</div><div>-</div><div>+</div><div>-</div></div></div><div>2 line</div><div><div><div>+</div><div>-</div><div>+</div><div>-</div><div>+</div><div>-</div></div></div><div>3 line</div><div><div><div>+</div><div>-</div><div>+</div><div>-</div><div>+</div><div>-</div></div></div><div>4 line</div><div><div><div>+</div><div>-</div><div>+</div><div>-</div><div>+</div><div>-</div></div></div><div>5 line</div><div><div><div>-</div><div>+</div><div>-</div><div>+</div><div>-</div><div>+</div></div></div><div>6 line</div><div><div><div>-</div><div>+</div><div>-</div><div>+</div><div>-</div><div>+</div></div></div><div>7 line</div><div><div><div>-</div><div>+</div><div>-</div><div>+</div><div>-</div><div>+</div></div></div><div>8 line</div><div><div><div>-</div><div>+</div><div>-</div><div>+</div><div>-</div><div>+</div></div></div></div><div>→</div><div><div>2nd frame</div><div><div>1 line</div><div><div><div>-</div><div>+</div><div>-</div><div>+</div><div>-</div><div>+</div></div></div><div>2 line</div><div><div><div>-</div><div>+</div><div>-</div><div>+</div><div>-</div><div>+</div></div></div><div>3 line</div><div><div><div>-</div><div>+</div><div>-</div><div>+</div><div>-</div><div>+</div></div></div><div>4 line</div><div><div><div>-</div><div>+</div><div>-</div><div>+</div><div>-</div><div>+</div></div></div><div>5 line</div><div><div><div>+</div><div>-</div><div>+</div><div>-</div><div>+</div><div>-</div></div></div><div>6 line</div><div><div><div>+</div><div>-</div><div>+</div><div>-</div><div>+</div><div>-</div></div></div><div>7 line</div><div><div><div>+</div><div>-</div><div>+</div><div>-</div><div>+</div><div>-</div></div></div><div>8 line</div><div><div><div>+</div><div>-</div><div>+</div><div>-</div><div>+</div><div>-</div></div></div></div></div></div></div></div>												
Restriction	To enable this command, EXTC Command Set Enable Register (FFh) must be set first.												
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default	<table><tr><th rowspan="2">Status</th><th>Default Value</th></tr><tr><th>NLA/NLB/NLC [3:0]</th></tr><tr><td>Power ON Sequence</td><td>4'b0000</td></tr><tr><td>S/W Reset</td><td>4'b0000</td></tr><tr><td>H/W Reset</td><td>4'b0000</td></tr></table>	Status	Default Value	NLA/NLB/NLC [3:0]	Power ON Sequence	4'b0000	S/W Reset	4'b0000	H/W Reset	4'b0000			
Status	Default Value												
	NLA/NLB/NLC [3:0]												
Power ON Sequence	4'b0000												
S/W Reset	4'b0000												
H/W Reset	4'b0000												

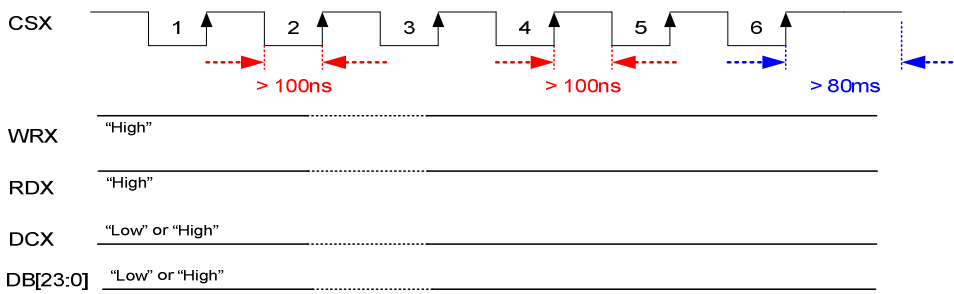
4.3.6. Blanking Porch Control (B5h)

B5h				BLKPRH (Blanking Porch)																													
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX																				
Command	0	1	↑	XX	1	0	1	1	0	1	0	1	B5h																				
1 st Parameter	1	1	↑	XX	0	VFP [6:0]							14																				
2 nd Parameter	1	1	↑	XX	0	VBP [6:0]							14																				
3 rd Parameter	1	1	↑	XX	HBP [7:0]								04																				
4 th Parameter	1	1	↑	XX	0	0	0	0	0	0	HBP [9:8]		00																				
Description	VFP [6:0]/VBP [6:0]: The VFP [6:0] and VBP [6:0] bits specify the line number of vertical front and back porch period respectively.																																
	<table><tr><th>VFP [6:0] VBP [6:0]</th><th>Number of HSYNC of front/back porch</th></tr><tr><td>0000000</td><td>Setting prohibited</td></tr><tr><td>0000001</td><td>Setting prohibited</td></tr><tr><td>0000010</td><td>2</td></tr><tr><td>0000011</td><td>3</td></tr><tr><td>:</td><td>:</td></tr><tr><td>:</td><td>:</td></tr><tr><td>1111101</td><td>125</td></tr><tr><td>1111110</td><td>126</td></tr><tr><td>1111111</td><td>127</td></tr></table>													VFP [6:0] VBP [6:0]	Number of HSYNC of front/back porch	0000000	Setting prohibited	0000001	Setting prohibited	0000010	2	0000011	3	:	:	:	:	1111101	125	1111110	126	1111111	127
	VFP [6:0] VBP [6:0]	Number of HSYNC of front/back porch																															
	0000000	Setting prohibited																															
	0000001	Setting prohibited																															
	0000010	2																															
	0000011	3																															
	:	:																															
	:	:																															
	1111101	125																															
	1111110	126																															
	1111111	127																															
	HBP [9:0]: The HBP [9:0] bits specify the line number of horizontal back porch period.																																
	<table><tr><th>HBP [9:0]</th><th>Number of DCK of the back porch</th></tr><tr><td>0000000000</td><td>Setting prohibited</td></tr><tr><td>0000000001</td><td>Setting prohibited</td></tr><tr><td>0000000010</td><td>2</td></tr><tr><td>0000000011</td><td>3</td></tr><tr><td>0000000100</td><td>4 (HBP [9:0] default)</td></tr><tr><td>:</td><td>:</td></tr><tr><td>:</td><td>:</td></tr><tr><td>1111111110</td><td>1022</td></tr><tr><td>1111111111</td><td>1023</td></tr></table>													HBP [9:0]	Number of DCK of the back porch	0000000000	Setting prohibited	0000000001	Setting prohibited	0000000010	2	0000000011	3	0000000100	4 (HBP [9:0] default)	:	:	:	:	1111111110	1022	1111111111	1023
	HBP [9:0]	Number of DCK of the back porch																															
0000000000	Setting prohibited																																
0000000001	Setting prohibited																																
0000000010	2																																
0000000011	3																																
0000000100	4 (HBP [9:0] default)																																
:	:																																
:	:																																
1111111110	1022																																
1111111111	1023																																
Restriction	To enable this command, EXTC Command Set Enable Register (FFh) must be set first.																																
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes								
Status	Availability																																
Normal Mode On, Idle Mode Off, Sleep Out	Yes																																
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Partial Mode On, Idle Mode Off, Sleep Out	Yes																																
Partial Mode On, Idle Mode On, Sleep Out	Yes																																
Sleep In	Yes																																
Default	<table><tr><th rowspan="2">Status</th><th colspan="3">Default Value</th></tr><tr><th>VFP [6:0]</th><th>VBP [6:0]</th><th>HBP [9:0]</th></tr><tr><td>Power ON Sequence</td><td>7'h14</td><td>7'h14</td><td>10'h04</td></tr><tr><td>S/W Reset</td><td>7'h14</td><td>7'h14</td><td>10'h04</td></tr><tr><td>H/W Reset</td><td>7'h14</td><td>7'h14</td><td>10'h04</td></tr></table>													Status	Default Value			VFP [6:0]	VBP [6:0]	HBP [9:0]	Power ON Sequence	7'h14	7'h14	10'h04	S/W Reset	7'h14	7'h14	10'h04	H/W Reset	7'h14	7'h14	10'h04	
Status	Default Value																																
	VFP [6:0]	VBP [6:0]	HBP [9:0]																														
Power ON Sequence	7'h14	7'h14	10'h04																														
S/W Reset	7'h14	7'h14	10'h04																														
H/W Reset	7'h14	7'h14	10'h04																														

4.3.7. Display Function Control (B6h)

B6h	DISCTRL (Display Function Control)																															
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX																			
Command	0	1	↑	XX	1	0	1	1	0	1	1	0	B6h																			
1 st parameter	1	1	↑	XX	SYNC mode	0	RM	0	0	0	1	PT	02																			
Description	SYNC mode: Select the operation mode of the RGB interface																															
	<table><tr><th>SYNC mode</th><th>RGB interface selection</th></tr><tr><td>0</td><td>DE mode</td></tr><tr><td>1</td><td>SYNC mode</td></tr></table>													SYNC mode	RGB interface selection	0	DE mode	1	SYNC mode													
	SYNC mode	RGB interface selection																														
	0	DE mode																														
	1	SYNC mode																														
	RM: Select the interface to access the GRAM. When RM = 0, the driver will write display data to the GRAM via the system interface, and the driver will write display data to the GRAM via RGB interface when RM = 1.																															
<table><tr><th>RM</th><th>Interface for RAM access</th></tr><tr><td>0</td><td>System interface</td></tr><tr><td>1</td><td>RGB interface</td></tr></table>													RM	Interface for RAM access	0	System interface	1	RGB interface														
RM	Interface for RAM access																															
0	System interface																															
1	RGB interface																															
PT : Determine source/VCOM output in a non-display area in the partial display mode.																																
<table><tr><th>PT</th><th>Source output on non-display area</th></tr><tr><td>0</td><td>V255</td></tr><tr><td>1</td><td>V0</td></tr></table>													PT	Source output on non-display area	0	V255	1	V0														
PT	Source output on non-display area																															
0	V255																															
1	V0																															
Restriction	To enable this command, EXTC Command Set Enable Register (FFh) must be set first.																															
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes							
Status	Availability																															
Normal Mode On, Idle Mode Off, Sleep Out	Yes																															
Normal Mode On, Idle Mode On, Sleep Out	Yes																															
Partial Mode On, Idle Mode Off, Sleep Out	Yes																															
Partial Mode On, Idle Mode On, Sleep Out	Yes																															
Sleep In	Yes																															
Default	<table><tr><th rowspan="2">Status</th><th colspan="3">Default Value</th></tr><tr><th>PT</th><th>RM</th><th>SYNC Mode</th></tr><tr><td>Power ON Sequence</td><td>1'b0</td><td>1'b0</td><td>1'b0</td></tr><tr><td>S/W Reset</td><td>1'b0</td><td>1'b0</td><td>1'b0</td></tr><tr><td>H/W Reset</td><td>1'b0</td><td>1'b0</td><td>1'b0</td></tr></table>													Status	Default Value			PT	RM	SYNC Mode	Power ON Sequence	1'b0	1'b0	1'b0	S/W Reset	1'b0	1'b0	1'b0	H/W Reset	1'b0	1'b0	1'b0
Status	Default Value																															
	PT	RM	SYNC Mode																													
Power ON Sequence	1'b0	1'b0	1'b0																													
S/W Reset	1'b0	1'b0	1'b0																													
H/W Reset	1'b0	1'b0	1'b0																													

4.3.8. Entry Mode Set (B7h)

B7h	ETMOD (Entry Mode Set)																								
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	1	0	1	1	0	1	1	1	B7h												
1 st Parameter	1	1	↑	XX	0	0	0	0	DSTB	1	1	0	06												
Description	<p>DSTB: The ILI9806G driver enters the Deep Standby Mode when DSTB is set to high (= 1). In the Deep Standby mode, both internal logic power and SRAM power are turned off, and the display data stored in the Frame Memory and the instructions are not saved. Rewrite Frame Memory content and instructions after exiting the Deep Standby Mode.</p> <p>The ILI9806G provides two ways to exit the Deep Standby Mode:</p> <p>(1) Exit the Deep Standby Mode by pulling down the CSX to low (= 0) 6 times.</p> <p>(2) Input a RESX pulse with effective low level duration to start up the inner logic regulator and make a transition to the initial state.</p> 																								
Restriction	To enable this command, EXTC Command Set Enable Register (FFh) must be set first.																								
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><tr><th rowspan="2">Status</th><th>Default Value</th></tr><tr><th>DSTB</th></tr><tr><td>Power ON Sequence</td><td>1'b0</td></tr><tr><td>S/W Reset</td><td>1'b0</td></tr><tr><td>H/W Reset</td><td>1'b0</td></tr></table>													Status	Default Value	DSTB	Power ON Sequence	1'b0	S/W Reset	1'b0	H/W Reset	1'b0			
Status	Default Value																								
	DSTB																								
Power ON Sequence	1'b0																								
S/W Reset	1'b0																								
H/W Reset	1'b0																								

4.3.9. DBI Type B Interface Setting (B8h)

B8H		Frame Memory Access and Interface Setting																							
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	1	0	1	1	1	0	0	0	B8h												
1 st parameter	1	1	↑	XX	0	WEMODE	EPF [1:0]		0	0	0	0	70												
Description	<p>WEMODE: Memory write control</p> <p>WEMODE = 0: When the transfer number of data exceeds (EC-SC+1)*(EP-SP+1), the exceeding data is ignored.</p> <p>WEMODE = 1: When the transfer number of data exceeds (EC-SC+1)*(EP-SP+1), the column and page number are reset, and the exceeding data is written into the following column and page.</p> <p>EPF [1:0]: Set the data format from 16/18-bit (R, G, B) to 24-bit (r, g, b) that is stored in the internal GRAM.</p> <p>See chapter 3.14.28 “16/18-bit color data mapping to 24-bit pixel data operation” for detail description.</p>																								
Restriction	To enable this command, EXTC Command Set Enable Register (FFh) must be set first.																								
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr><tr><th>WEMODE</th><th>EPF [1:0]</th></tr><tr><td>Power ON Sequence</td><td>1b'1</td><td>2b'11</td></tr><tr><td>H/W Reset</td><td>1b'1</td><td>2b'11</td></tr></table>													Status	Default Value		WEMODE	EPF [1:0]	Power ON Sequence	1b'1	2b'11	H/W Reset	1b'1	2b'11	
Status	Default Value																								
	WEMODE	EPF [1:0]																							
Power ON Sequence	1b'1	2b'11																							
H/W Reset	1b'1	2b'11																							

4.3.10. Panel Control (B9h)

B9h	PANELCTRL (Set panel operation mode)																																	
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX																					
Command	0	1	↑	XX	1	0	1	1	1	0	0	1	B9h																					
1 st parameter	1	1	↑	XX	MY_ Panel	MX_ Panel	MV_ Panel	ML_ Panel	BGR_ Panel	MH_ Panel	SS_ Panel	GS_ Panel	00																					
2 nd parameter	1	1	↑	XX	0	0	0	0	0	0	REV_ Panel	0	00																					
Description	This command defines the panel operation mode.																																	
	Symbol		Name		Description																													
	MY_ Panel		Panel Row Address Order		These 3 bits control the write/read direction from the MPU to the memory.																													
	MX_ Panel		Panel Column Address Order																															
	MV_ Panel		Panel Row/Column Exchange																															
	ML_ Panel		Panel Vertical Refresh Order		LCD vertical refresh direction control																													
	BGR_ Panel		Panel RGB-BGR Order		Color selector switch control (0 = RGB color filter panel, 1 = BGR color filter panel)																													
	MH_ Panel		Panel Horizontal Refresh Order		LCD horizontal refreshing direction control																													
	SS_ Panel		Panel Flip Horizontal		Select the Source driver scan direction on the panel module																													
	GS_ Panel		Panel Flip Vertical		Select the Gate driver scan direction on the panel module																													
REV_ Panel		Panel inversion mode		Panel display inversion on the panel module																														
REV_ Panel: Select normally white or normally black panel.																																		
					<table><tr><th>REV</th><th>Panel</th><th>Data</th><th>Color</th><th>Source</th></tr><tr><td rowspan="2">0</td><td rowspan="2">Normally white</td><td>0 x 00</td><td>Black</td><td>V0+/V0-</td></tr><tr><td>0 x FF</td><td>White</td><td>V255+/V255-</td></tr><tr><td rowspan="2">1</td><td rowspan="2">normally black</td><td>0 x 00</td><td>Black</td><td>V255+/V255-</td></tr><tr><td>0 x FF</td><td>White</td><td>V0+/V0-</td></tr></table>									REV	Panel	Data	Color	Source	0	Normally white	0 x 00	Black	V0+/V0-	0 x FF	White	V255+/V255-	1	normally black	0 x 00	Black	V255+/V255-	0 x FF	White	V0+/V0-
REV	Panel	Data	Color	Source																														
0	Normally white	0 x 00	Black	V0+/V0-																														
		0 x FF	White	V255+/V255-																														
1	normally black	0 x 00	Black	V255+/V255-																														
		0 x FF	White	V0+/V0-																														
SS_ Panel: Select the shift direction of outputs from the source driver.																																		
					<table><tr><th>SS_ Panel</th><th>Source Output Scan Direction</th></tr><tr><td>0</td><td>S1 → S1440</td></tr><tr><td>1</td><td>S1440 → S1</td></tr></table>									SS_ Panel	Source Output Scan Direction	0	S1 → S1440	1	S1440 → S1															
SS_ Panel	Source Output Scan Direction																																	
0	S1 → S1440																																	
1	S1440 → S1																																	
GS_ Panel: Set the direction of the gate driver scan in the display range.																																		
Note: Its usage depends on the design of the Panel.																																		
Restriction	To enable this command, EXTC Command Set Enable Register (FFh) must be set first.																																	
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes									
Status	Availability																																	
Normal Mode On, Idle Mode Off, Sleep Out	Yes																																	
Normal Mode On, Idle Mode On, Sleep Out	Yes																																	
Partial Mode On, Idle Mode Off, Sleep Out	Yes																																	
Partial Mode On, Idle Mode On, Sleep Out	Yes																																	
Sleep In	Yes																																	

Default

Status	Default Value				
	MY_ Panel	MX_ Panel	MV_ Panel	ML_ Panel	BGR_ Panel
Power On Sequence	1b'0	1b'0	1b'0	1b'0	1b'0
S/W Reset	1b'0	1b'0	1b'0	1b'0	1b'0
H/W Reset	1b'0	1b'0	1b'0	1b'0	1b'0

Status	Default Value			
	MH_ Panel	SS_ Panel	GS_ Panel	REV_ Panel
Power On Sequence	1b'0	1b'0	1b'0	1b'0
S/W Reset	1b'0	1b'0	1b'0	1b'0
H/W Reset	1b'0	1b'0	1b'0	1b'0

4.3.11. SPI Interface Setting (BAh)

BAH	Frame Memory Access and Interface Setting																								
	DCX	RDX	WRX	D[23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	1	0	1	1	1	0	1	0	BAh												
1 st parameter	1	1	↑	XX	Spitype	1	1	0	0	0	0	0	XX												
Description	Spitype: Spitype = 0: SPI interface transfers data through SDI and SDO pins. Spitype = 1: SPI interface transfers data through SDI (SDA) pin.																								
Restriction	To enable this command, EXTC Command Set Enable Register (FFh) must be set first.																								
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><tr><th rowspan="2">Status</th><th>Default Value</th></tr><tr><th>Spitype</th></tr><tr><td>Power ON Sequence</td><td>1b'1</td></tr><tr><td>S/W Reset</td><td>1b'1</td></tr><tr><td>H/W Reset</td><td>1b'1</td></tr></table>													Status	Default Value	Spitype	Power ON Sequence	1b'1	S/W Reset	1b'1	H/W Reset	1b'1			
Status	Default Value																								
	Spitype																								
Power ON Sequence	1b'1																								
S/W Reset	1b'1																								
H/W Reset	1b'1																								

4.3.12. Power Control 1 (C0h)

C0h	PWCTRL 1 (Power Control 1)																															
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX																			
Command	0	1	↑	XX	1	1	0	0	0	0	0	0	C0h																			
1 st parameter	1	1	↑	XX	VD[2:0]			VE[2:0]			1	1	03																			
2 nd parameter	1	1	↑	XX	0	0	0	0	1	0	1	1	0B																			
3 rd parameter	1	1	↑	XX	0	BH	0	0	BL [1:0]		1	0	0A																			
4 th parameter	1	1	↑	XX	0	0	0	0	0	0	0	0	00																			
5 th parameter	1	1	↑	XX	0	0	0	0	0	0	0	0	00																			
6 th parameter	1	1	↑	XX	1	0	0	0	1	0	0	0	88																			
7 th parameter	1	1	↑	XX	0	0	1	0	1	1	0	0	2C																			
8 th parameter	1	1	↑	XX	0	1	0	1	0	0	0	0	50																			
9 th parameter	1	1	↑	XX	0	0	0	0	0	0	0	0	00																			
10 th parameter	1	1	↑	XX	0	0	0	0	0	0	0	0	00																			
11 th parameter	1	1	↑	XX	0	0	0	0	0	0	0	0	00																			
12 th parameter	1	1	↑	XX	0	0	0	0	0	0	0	0	00																			
13 th parameter	1	1	↑	XX	PCK_1[1:0]		PCK_2[1:0]		PCK_3[1:0]		PCK_4[1:0]		FF																			
Description	VD [2:0]: Set the AVDD clamp level.																															
	<table><tr><th colspan="2">AVDD Cla p Level</th></tr><tr><th>VD[2:0]</th><th>Voltage</th></tr><tr><td>000</td><td>5.2</td></tr><tr><td>001</td><td>5.3</td></tr><tr><td>010</td><td>5.4</td></tr><tr><td>011</td><td>5.5</td></tr><tr><td>100</td><td>5.6</td></tr><tr><td>101</td><td>5.1</td></tr><tr><td>110</td><td>5.0</td></tr><tr><td>111</td><td>5.7</td></tr></table>													AVDD Cla p Level		VD[2:0]	Voltage	000	5.2	001	5.3	010	5.4	011	5.5	100	5.6	101	5.1	110	5.0	111
AVDD Cla p Level																																
VD[2:0]	Voltage																															
000	5.2																															
001	5.3																															
010	5.4																															
011	5.5																															
100	5.6																															
101	5.1																															
110	5.0																															
111	5.7																															
	VE [2:0]: Set the AVEE clamp level.																															
	<table><tr><th colspan="2">AVEE Clamp Level</th></tr><tr><th>VE[2:0]</th><th>Voltage</th></tr><tr><td>000</td><td>-4.9</td></tr><tr><td>001</td><td>-5.0</td></tr><tr><td>010</td><td>-5.1</td></tr><tr><td>011</td><td>-5.2</td></tr><tr><td>100</td><td>-5.2</td></tr><tr><td>101</td><td>-5.3</td></tr><tr><td>110</td><td>-5.4</td></tr><tr><td>111</td><td>-5.5</td></tr></table>													AVEE Clamp Level		VE[2:0]	Voltage	000	-4.9	001	-5.0	010	-5.1	011	-5.2	100	-5.2	101	-5.3	110	-5.4	111
AVEE Clamp Level																																
VE[2:0]	Voltage																															
000	-4.9																															
001	-5.0																															
010	-5.1																															
011	-5.2																															
100	-5.2																															
101	-5.3																															
110	-5.4																															
111	-5.5																															

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	<p>BH : Sets the factor used in the step-up circuits for VGH.</p> <p>Select the optimal step-up factor for the operating voltage. To reduce power consumption, set a smaller factor.</p> <table><tr><th colspan="2">VGH operation voltage</th></tr><tr><th>BH</th><th>VGH</th></tr><tr><td>0</td><td>2AVDD – AVEE</td></tr><tr><td>1</td><td>AVDD – AVEE + VCI</td></tr></table> <p>BL [1:0]: Sets the factor used in the step-up circuits for VGL.</p> <p>Select the optimal step-up factor for the operating voltage. To reduce power consumption, set a smaller factor.</p> <table><tr><th colspan="4">VGH / VGL operation voltage</th></tr><tr><th colspan="2">BL [1:0]</th><th>VGH</th><th>VGL</th></tr><tr><td>0</td><td>0</td><td>2AVDD - AVEE</td><td>AVEE - AVDD</td></tr><tr><td>0</td><td>1</td><td>2AVDD - AVEE</td><td>2AVEE - AVDD</td></tr><tr><td>1</td><td>0</td><td>2AVDD - AVEE</td><td>AVEE – AVDD + VCL</td></tr><tr><td>1</td><td>1</td><td>2AVDD - AVEE</td><td>AVEE - VDDDB + VCL</td></tr></table> <p>Note. The restriction setting $VGH - VGL < 32\text{ V}$.</p>	VGH operation voltage		BH	VGH	0	2AVDD – AVEE	1	AVDD – AVEE + VCI	VGH / VGL operation voltage				BL [1:0]		VGH	VGL	0	0	2AVDD - AVEE	AVEE - AVDD	0	1	2AVDD - AVEE	2AVEE - AVDD	1	0	2AVDD - AVEE	AVEE – AVDD + VCL	1	1	2AVDD - AVEE	AVEE - VDDDB + VCL
VGH operation voltage																																	
BH	VGH																																
0	2AVDD – AVEE																																
1	AVDD – AVEE + VCI																																
VGH / VGL operation voltage																																	
BL [1:0]		VGH	VGL																														
0	0	2AVDD - AVEE	AVEE - AVDD																														
0	1	2AVDD - AVEE	2AVEE - AVDD																														
1	0	2AVDD - AVEE	AVEE – AVDD + VCL																														
1	1	2AVDD - AVEE	AVEE - VDDDB + VCL																														
Restriction	To enable this command, EXTC Command Set Enable Register (FFh) must be set first.																																
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes																				
Status	Availability																																
Normal Mode On, Idle Mode Off, Sleep Out	Yes																																
Normal Mode On, Idle Mode On, Sleep Out	Yes																																
Partial Mode On, Idle Mode Off, Sleep Out	Yes																																
Partial Mode On, Idle Mode On, Sleep Out	Yes																																
Sleep In	Yes																																
Default	<table><tr><th rowspan="2">Status</th><th colspan="3">Default Value</th></tr><tr><th>VD[2:0]</th><th>VE[2:0]</th><th>BL [1:0]</th></tr><tr><td>Power ON Sequence</td><td>3'b000</td><td>3'b000</td><td>2'b10</td></tr><tr><td>S/W Reset</td><td>3'b000</td><td>3'b000</td><td>2'b10</td></tr><tr><td>H/W Reset</td><td>3'b000</td><td>3'b000</td><td>2'b10</td></tr></table>	Status	Default Value			VD[2:0]	VE[2:0]	BL [1:0]	Power ON Sequence	3'b000	3'b000	2'b10	S/W Reset	3'b000	3'b000	2'b10	H/W Reset	3'b000	3'b000	2'b10													
Status	Default Value																																
	VD[2:0]	VE[2:0]	BL [1:0]																														
Power ON Sequence	3'b000	3'b000	2'b10																														
S/W Reset	3'b000	3'b000	2'b10																														
H/W Reset	3'b000	3'b000	2'b10																														

4.3.13. Power Control 2 (C1h)

C1h	PWCTRL 2 (Power Control 2)																																						
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HE X																										
Command	0	1	↑	XX	1	1	0	0	0	0	0	1	C1h																										
1 st parameter	1	1	↑	XX	0	0	BG_ISC [1:0]		0	1	1	1	17																										
2 nd parameter	1	1	↑	XX	VRH1 [7:0]								90																										
3 rd parameter	1	1	↑	XX	VRH2 [7:0]								90																										
4 th parameter	1	1	↑	XX	0	0	EXT_CPCK_SEL[5:4]		0	0	0	0	20																										
Description	BG_ISC [1:0]: Source OP Amp bias control.																																						
	<table><tr><th colspan="2">BG_ISC [1:0]</th><th>Source bias</th></tr><tr><td>0</td><td>0</td><td>0.5 x I</td></tr><tr><td>0</td><td>1</td><td>1.0 x I</td></tr><tr><td>1</td><td>0</td><td>1.5 x I</td></tr><tr><td>1</td><td>1</td><td>2.0 x I</td></tr></table>													BG_ISC [1:0]		Source bias	0	0	0.5 x I	0	1	1.0 x I	1	0	1.5 x I	1	1	2.0 x I											
	BG_ISC [1:0]		Source bias																																				
	0	0	0.5 x I																																				
	0	1	1.0 x I																																				
	1	0	1.5 x I																																				
	1	1	2.0 x I																																				
	VRH1 [7:0]: Sets the VGMP voltage for positive Gamma																																						
	<table><tr><th>VRH1 [7:0]</th><th>VGMP</th></tr><tr><td>8'h00</td><td>3.0000</td></tr><tr><td>8'h01</td><td>3.0125</td></tr><tr><td>8'h02</td><td>3.0250</td></tr><tr><td>:</td><td>:</td></tr><tr><td>8'h7F</td><td>4.5875</td></tr><tr><td>8'h80</td><td>4.6000</td></tr><tr><td>:</td><td>:</td></tr><tr><td>8'h8F</td><td>4.7875</td></tr><tr><td>8'h90</td><td>4.8000</td></tr><tr><td>:</td><td>:</td></tr><tr><td>8'hFE</td><td>6.1750</td></tr><tr><td>8'hFF</td><td>6.1875</td></tr></table>													VRH1 [7:0]	VGMP	8'h00	3.0000	8'h01	3.0125	8'h02	3.0250	:	:	8'h7F	4.5875	8'h80	4.6000	:	:	8'h8F	4.7875	8'h90	4.8000	:	:	8'hFE	6.1750	8'hFF	6.1875
	VRH1 [7:0]	VGMP																																					
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	8'h8F	4.7875																																					
	8'h90	4.8000																																					
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	8'hFE	6.1750																																					
	8'hFF	6.1875																																					
	Note: VGMP ≤ AVDD – 0.5V																																						
	VRH2 [7:0]: Sets the VGMP voltage for negative Gamma																																						
	<table><tr><th>VRH2 [7:0]</th><th>VGMP</th></tr><tr><td>8'h00</td><td>- 3.0000</td></tr><tr><td>8'h01</td><td>- 3.0125</td></tr><tr><td>8'h02</td><td>- 3.0250</td></tr><tr><td>:</td><td>:</td></tr><tr><td>8'h7F</td><td>- 4.5875</td></tr><tr><td>8'h80</td><td>- 4.6000</td></tr><tr><td>:</td><td>:</td></tr><tr><td>8'h8F</td><td>- 4.7875</td></tr><tr><td>8'h90</td><td>- 4.8000</td></tr><tr><td>:</td><td>:</td></tr><tr><td>8'hFE</td><td>- 6.1750</td></tr><tr><td>8'hFF</td><td>- 6.1875</td></tr></table>													VRH2 [7:0]	VGMP	8'h00	- 3.0000	8'h01	- 3.0125	8'h02	- 3.0250	:	:	8'h7F	- 4.5875	8'h80	- 4.6000	:	:	8'h8F	- 4.7875	8'h90	- 4.8000	:	:	8'hFE	- 6.1750	8'hFF	- 6.1875
VRH2 [7:0]	VGMP																																						
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8'h01	- 3.0125																																						
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:	:																																						
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Note: VGMP																																							

The information contained herein is the exclusive property of ILI Technology Corp. and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of ILI Technology Corp.

	<p>EXT_CPCK_SEL [5:4]: Sets the ILI4002 AVDD / AVEE pumping ratio.</p> <table> <tr> <th colspan="2">EXT_CPCK_SEL [5:4]</th> <th>Pumping Ratio</th> </tr> <tr> <td>0</td> <td>0</td> <td>1.5 X</td> </tr> <tr> <td>0</td> <td>1</td> <td>2.0 X</td> </tr> <tr> <td>1</td> <td>0</td> <td>3.0 X</td> </tr> <tr> <td>1</td> <td>1</td> <td>OFF</td> </tr> </table> <p>Note : If VCI>3V, ILI4002 AVDD/AVEE pumping ratio=3.0X setting is prohibited.</p>	EXT_CPCK_SEL [5:4]		Pumping Ratio	0	0	1.5 X	0	1	2.0 X	1	0	3.0 X	1	1	OFF									
EXT_CPCK_SEL [5:4]		Pumping Ratio																							
0	0	1.5 X																							
0	1	2.0 X																							
1	0	3.0 X																							
1	1	OFF																							
Restriction	To enable this command, EXTC Command Set Enable Register (FFh) must be set first.																								
Register Availability	<table> <tr> <th>Status</th> <th>Availability</th> </tr> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes												
Status	Availability																								
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Default	<table> <tr> <th rowspan="2">Status</th> <th colspan="4">Default Value</th> </tr> <tr> <th>BG_ISC [1:0]</th> <th>VRH1 [7:0]</th> <th>VRH2 [7:0]</th> <th>EXT_CPCK_SEL [1:0]</th> </tr> <tr> <td>Power ON Sequence</td> <td>2'b01</td> <td>8'h90</td> <td>8'h90</td> <td>2'b10</td> </tr> <tr> <td>S/W Reset</td> <td>2'b01</td> <td>No Change</td> <td>No Change</td> <td>2'b10</td> </tr> <tr> <td>H/W Reset</td> <td>2'b01</td> <td>8'h90</td> <td>8'h90</td> <td>2'b10</td> </tr> </table>	Status	Default Value				BG_ISC [1:0]	VRH1 [7:0]	VRH2 [7:0]	EXT_CPCK_SEL [1:0]	Power ON Sequence	2'b01	8'h90	8'h90	2'b10	S/W Reset	2'b01	No Change	No Change	2'b10	H/W Reset	2'b01	8'h90	8'h90	2'b10
Status	Default Value																								
	BG_ISC [1:0]	VRH1 [7:0]	VRH2 [7:0]	EXT_CPCK_SEL [1:0]																					
Power ON Sequence	2'b01	8'h90	8'h90	2'b10																					
S/W Reset	2'b01	No Change	No Change	2'b10																					
H/W Reset	2'b01	8'h90	8'h90	2'b10																					

4.3.14. Power Control 3 (C2h)

C2h	PWCTRL 3 (Power Control 3)																																																
	DCX	SCL	Parameter								HEX																																						
			D7	D6	D5	D4	D3	D2	D1	D0																																							
Command	0	↑	1	1	0	0	0	0	1	0	C2h																																						
1 st parameter	1	↑	0	1	0	0	0	0	0	1	41h																																						
2 nd parameter	1	↑	0	1	0	0	0	1	0	0	44h																																						
3 rd parameter	1	↑	0	0	0	0	0	1	0	0	04h																																						
4 th parameter	1	↑	VGSP[7:0]								00h																																						
5 th parameter	1	↑	VGSN[7:0]								00h																																						
Description	VGSP [7:0]: Selects positive gamma low voltage.																																																
	<table><tr><th>VGSP[7:0]</th><th>Spec (V)</th></tr><tr><td>8'h00</td><td>0</td></tr><tr><td>8'h01</td><td>0.3</td></tr><tr><td>8'h02</td><td>0.3125</td></tr><tr><td>8'h03</td><td>0.325</td></tr><tr><td>8'h04</td><td>0.3375</td></tr><tr><td>8'h05</td><td>0.35</td></tr><tr><td>8'h06</td><td>0.3625</td></tr><tr><td>8'h07</td><td>0.375</td></tr><tr><td>8'h08</td><td>0.3875</td></tr><tr><td colspan="2">...</td></tr><tr><td>8'hFA</td><td>3.4125</td></tr><tr><td>8'hFB</td><td>3.425</td></tr><tr><td>8'hFC</td><td>3.4375</td></tr><tr><td>8'hFD</td><td>3.45</td></tr><tr><td>8'hFE</td><td>3.4625</td></tr><tr><td>8'hFF</td><td>3.475</td></tr></table>											VGSP[7:0]	Spec (V)	8'h00	0	8'h01	0.3	8'h02	0.3125	8'h03	0.325	8'h04	0.3375	8'h05	0.35	8'h06	0.3625	8'h07	0.375	8'h08	0.3875	...		8'hFA	3.4125	8'hFB	3.425	8'hFC	3.4375	8'hFD	3.45	8'hFE	3.4625	8'hFF	3.475				
	VGSP[7:0]	Spec (V)																																															
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	8'hFF	3.475																																															
	VGSN [7:0]: Selects negative gamma high voltage.																																																
	<table><tr><th>VGSN[7:0]</th><th>Spec(V)</th></tr><tr><td>8'h00</td><td>0</td></tr><tr><td>8'h01</td><td>-0.3</td></tr><tr><td>8'h02</td><td>-0.3125</td></tr><tr><td>8'h03</td><td>-0.325</td></tr><tr><td>8'h04</td><td>-0.3375</td></tr><tr><td>8'h05</td><td>-0.35</td></tr><tr><td>8'h06</td><td>-0.3625</td></tr><tr><td>8'h07</td><td>-0.375</td></tr><tr><td>8'h08</td><td>-0.3875</td></tr><tr><td>8'h09</td><td>-0.4</td></tr><tr><td>8'h0A</td><td>-0.4125</td></tr><tr><td>8'h0B</td><td>-0.425</td></tr><tr><td colspan="2">...</td></tr><tr><td>8'hFB</td><td>-3.425</td></tr><tr><td>8'hFC</td><td>-3.4375</td></tr><tr><td>8'hFD</td><td>-3.45</td></tr><tr><td>8'hFE</td><td>-3.4625</td></tr><tr><td>8'hFF</td><td>-3.475</td></tr></table>											VGSN[7:0]	Spec(V)	8'h00	0	8'h01	-0.3	8'h02	-0.3125	8'h03	-0.325	8'h04	-0.3375	8'h05	-0.35	8'h06	-0.3625	8'h07	-0.375	8'h08	-0.3875	8'h09	-0.4	8'h0A	-0.4125	8'h0B	-0.425	...		8'hFB	-3.425	8'hFC	-3.4375	8'hFD	-3.45	8'hFE	-3.4625	8'hFF	-3.475
	VGSN[7:0]	Spec(V)																																															
	8'h00	0																																															
	8'h01	-0.3																																															
	8'h02	-0.3125																																															
8'h03	-0.325																																																
8'h04	-0.3375																																																
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8'h07	-0.375																																																
8'h08	-0.3875																																																
8'h09	-0.4																																																
8'h0A	-0.4125																																																
8'h0B	-0.425																																																
...																																																	
8'hFB	-3.425																																																
8'hFC	-3.4375																																																
8'hFD	-3.45																																																
8'hFE	-3.4625																																																
8'hFF	-3.475																																																
Restriction	To enable this command, “EXTC Command Set enable register (FFh) ” must set first.																																																

Register Availability	<table><tr><th>Status</th><th colspan="2">Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td colspan="2">Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td colspan="2">Yes</td></tr><tr><td>Idle Mode Off, Sleep Out</td><td colspan="2">Yes</td></tr><tr><td>Idle Mode On, Sleep Out</td><td colspan="2">Yes</td></tr><tr><td>Sleep In</td><td colspan="2">Yes</td></tr></table>			Status	Availability		Normal Mode On, Idle Mode Off, Sleep Out	Yes		Normal Mode On, Idle Mode On, Sleep Out	Yes		Idle Mode Off, Sleep Out	Yes		Idle Mode On, Sleep Out	Yes		Sleep In	Yes	
	Status	Availability																			
	Normal Mode On, Idle Mode Off, Sleep Out	Yes																			
	Normal Mode On, Idle Mode On, Sleep Out	Yes																			
	Idle Mode Off, Sleep Out	Yes																			
	Idle Mode On, Sleep Out	Yes																			
Sleep In	Yes																				
Default	<table><tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr><tr><th>VGSP[7:0]</th><th>VGSN[7:0]</th></tr><tr><td>Power ON Sequence</td><td>8'h00</td><td>8'h00</td></tr><tr><td>S/W Reset</td><td>8'h00</td><td>8'h00</td></tr><tr><td>H/W Reset</td><td>8'h00</td><td>8'h00</td></tr></table>			Status	Default Value		VGSP[7:0]	VGSN[7:0]	Power ON Sequence	8'h00	8'h00	S/W Reset	8'h00	8'h00	H/W Reset	8'h00	8'h00				
	Status	Default Value																			
		VGSP[7:0]	VGSN[7:0]																		
	Power ON Sequence	8'h00	8'h00																		
	S/W Reset	8'h00	8'h00																		
H/W Reset	8'h00	8'h00																			

4.3.15. VCOM Control 1 (C7h)

C7h	VMCTRL1 (VCOM Control 1)																																						
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX																										
Command	0	1	↑	XX	1	1	0	0	0	1	1	1	C7h																										
1 st Parameter	1	1	↑	XX	VCM [7:0]								8F																										
2 nd Parameter	1	1	↑	XX	nVM	0	0	0	0	0	0	0	80																										
Description	nVM: The source of selection of Vcom voltage setting either RC7h VCM[7:0] setting by user or NV memory programmed by user. 0 : Selection from NV memory. 1 : Selection from RC7h VCM[7:0]. If NV memory programmed before, the nVM bit set to “0” automatically, user sets nVM bit to “1”, that can enable RC7 VCM[7:0] setting again.																																						
	VCM [7:0] is used to set factors to generate the VCOM voltage.																																						
	<table><tr><th>VCM [7:0]</th><th>VCOM</th></tr><tr><td>8'h00</td><td>0.0000</td></tr><tr><td>8'h01</td><td>- 0.0125</td></tr><tr><td>8'h02</td><td>- 0.0250</td></tr><tr><td>:</td><td>:</td></tr><tr><td>8'h7F</td><td>- 1.5875</td></tr><tr><td>8'h80</td><td>- 1.6000</td></tr><tr><td>:</td><td>:</td></tr><tr><td>8'h8F</td><td>- 1.7875</td></tr><tr><td>8'h90</td><td>- 1.8000</td></tr><tr><td>:</td><td>:</td></tr><tr><td>8'hFE</td><td>- 3.1750</td></tr><tr><td>8'hFF</td><td>- 3.1875</td></tr></table>													VCM [7:0]	VCOM	8'h00	0.0000	8'h01	- 0.0125	8'h02	- 0.0250	:	:	8'h7F	- 1.5875	8'h80	- 1.6000	:	:	8'h8F	- 1.7875	8'h90	- 1.8000	:	:	8'hFE	- 3.1750	8'hFF	- 3.1875
	VCM [7:0]	VCOM																																					
	8'h00	0.0000																																					
	8'h01	- 0.0125																																					
	8'h02	- 0.0250																																					
	:	:																																					
	8'h7F	- 1.5875																																					
	8'h80	- 1.6000																																					
	:	:																																					
	8'h8F	- 1.7875																																					
	8'h90	- 1.8000																																					
	:	:																																					
	8'hFE	- 3.1750																																					
8'hFF	- 3.1875																																						
Note: VCOM ≧ VCL + 0.3V																																							
Restriction	To enable this command, EXTC Command Set Enable Register (FFh) must be set first.																																						
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes														
Status	Availability																																						
Normal Mode On, Idle Mode Off, Sleep Out	Yes																																						
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Partial Mode On, Idle Mode Off, Sleep Out	Yes																																						
Partial Mode On, Idle Mode On, Sleep Out	Yes																																						
Sleep In	Yes																																						
Default	<table><tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr><tr><th>VCM [7:0]</th><th>nVM</th></tr><tr><td>Power ON Sequence</td><td>8'h8F</td><td>1'b1</td></tr><tr><td>S/W Reset</td><td>No Change</td><td>1'b1</td></tr><tr><td>H/W Reset</td><td>8'h8F</td><td>1'b1</td></tr></table>													Status	Default Value		VCM [7:0]	nVM	Power ON Sequence	8'h8F	1'b1	S/W Reset	No Change	1'b1	H/W Reset	8'h8F	1'b1												
Status	Default Value																																						
	VCM [7:0]	nVM																																					
Power ON Sequence	8'h8F	1'b1																																					
S/W Reset	No Change	1'b1																																					
H/W Reset	8'h8F	1'b1																																					

4.3.16. Backlight Control 1 (C8h)

C8h	BLCTRL1 (Backlight Control 1)																																																																																																																																									
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																																																																																													
Command	0	1	↑	XX	1	1	0	0	1	0	0	0	C8h																																																																																																																													
1 st Parameter	1	1	↑	XX	PWM_DIV [7:0]								XX																																																																																																																													
Description	PWM_DIV [7:0]: PWM_OUT output period control. This command is used to adjust the PWM waveform period of PWM_OUT. The PWM period is calculated by the following equation.																																																																																																																																									
	<div>$f_{pwm_out} = \frac{18\text{ MHz}}{(\text{PWM_DIV}[7:0] + 1) \times 255}$</div>																																																																																																																																									
	<table><thead><tr><th colspan="8">PWM_DIV [7:0]</th><th rowspan="2">f_{PWM_OUT}</th></tr><tr><th>D7</th><th>D6</th><th>D</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr></thead><tbody><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>70.58 KHz</td></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>35.29 KHz</td></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>23.53 KHz</td></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>17.65 KHz</td></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>14.12 KHz</td></tr><tr><td colspan="8">:</td><td>:</td></tr><tr><td colspan="8">:</td><td>:</td></tr><tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>280.1 Hz</td></tr><tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>279.0 Hz</td></tr><tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>277.9 Hz</td></tr><tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>276.8 Hz</td></tr><tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>275.7 Hz</td></tr></tbody></table>													PWM_DIV [7:0]								f _{PWM_OUT}	D7	D6	D	D4	D3	D2	D1	D0	0	0	0	0	0	0	0	0	70.58 KHz	0	0	0	0	0	0	0	1	35.29 KHz	0	0	0	0	0	0	1	0	23.53 KHz	0	0	0	0	0	0	1	1	17.65 KHz	0	0	0	0	0	1	0	0	14.12 KHz	:								:	:								:	1	1	1	1	1	0	1	1	280.1 Hz	1	1	1	1	1	1	0	0	279.0 Hz	1	1	1	1	1	1	0	1	277.9 Hz	1	1	1	1	1	1	1	0	276.8 Hz	1	1	1	1	1	1	1	1	275.7 Hz
	PWM_DIV [7:0]								f _{PWM_OUT}																																																																																																																																	
	D7	D6	D	D4	D3	D2	D1	D0																																																																																																																																		
	0	0	0	0	0	0	0	0	70.58 KHz																																																																																																																																	
	0	0	0	0	0	0	0	1	35.29 KHz																																																																																																																																	
	0	0	0	0	0	0	1	0	23.53 KHz																																																																																																																																	
	0	0	0	0	0	0	1	1	17.65 KHz																																																																																																																																	
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:								:																																																																																																																																		
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1	1	1	1	1	0	1	1	280.1 Hz																																																																																																																																		
1	1	1	1	1	1	0	0	279.0 Hz																																																																																																																																		
1	1	1	1	1	1	0	1	277.9 Hz																																																																																																																																		
1	1	1	1	1	1	1	0	276.8 Hz																																																																																																																																		
1	1	1	1	1	1	1	1	275.7 Hz																																																																																																																																		
<div><p>PWM_OUT</p></div>																																																																																																																																										
<i>Note: The output frequency tolerance of internal frequency divider in the CABC is ±10%</i>																																																																																																																																										
Restriction	To enable this command, EXTC Command Set Enable Register (FFh) must be set first.																																																																																																																																									
Register Availability	<table><thead><tr><th>Status</th><th>Availability</th></tr></thead><tbody><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></tbody></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes																																																																																																																	
Status	Availability																																																																																																																																									
Normal Mode On, Idle Mode Off, Sleep Out	Yes																																																																																																																																									
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Partial Mode On, Idle Mode On, Sleep Out	Yes																																																																																																																																									
Sleep In	Yes																																																																																																																																									

Default			
		Status	Default Value
		Power ON Sequence	8'hE8
		S/W Reset	No Change
		H/W Reset	8'hE8

4.3.17. Backlight Control 2 (C9h)

C9h	BLCTRL2 (Backlight Control 2)																																																																																																											
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																																																															
Command	0	1	↑	XX	1	1	0	0	1	0	0	1	C9h																																																																																															
1 st Parameter	1	1	↑	XX	THRES_MOV [3:0]				THRES_STILL [3:0]				XX																																																																																															
Description	THRES_MOV [3:0]: This parameter is used to set the ratio (percentage) of the maximum number of pixels that makes display image white (data = 63) in the total pixels by image process in the Moving Image mode. After this parameter sets the number of pixels that makes display image white, then the threshold grayscale value (DTH) that makes display image white is set so that the number of the pixels set by this parameter will not be changed.																																																																																																											
	<table><thead><tr><th colspan="4">THRES_MOV [3:0]</th><th rowspan="2">Description</th></tr><tr><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr></thead><tbody><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>99 %</td></tr><tr><td>0</td><td>0</td><td>0</td><td>1</td><td>98 %</td></tr><tr><td>0</td><td>0</td><td>1</td><td>0</td><td>96 %</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1</td><td>94 %</td></tr><tr><td>0</td><td>1</td><td>0</td><td>0</td><td>92 %</td></tr><tr><td>0</td><td>1</td><td>0</td><td>1</td><td>90 %</td></tr><tr><td>0</td><td>1</td><td>1</td><td>0</td><td>88 %</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1</td><td>86 %</td></tr></tbody></table>					THRES_MOV [3:0]				Description	D3	D2	D1	D0	0	0	0	0	99 %	0	0	0	1	98 %	0	0	1	0	96 %	0	0	1	1	94 %	0	1	0	0	92 %	0	1	0	1	90 %	0	1	1	0	88 %	0	1	1	1	86 %	<table><thead><tr><th colspan="4">THRES_MOV [3:0]</th><th rowspan="2">Description</th></tr><tr><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr></thead><tbody><tr><td>1</td><td>0</td><td>0</td><td>0</td><td>84 %</td></tr><tr><td>1</td><td>0</td><td>0</td><td>1</td><td>82 %</td></tr><tr><td>1</td><td>0</td><td>1</td><td>0</td><td>80 %</td></tr><tr><td>1</td><td>0</td><td>1</td><td>1</td><td>78 %</td></tr><tr><td>1</td><td>1</td><td>0</td><td>0</td><td>76 %</td></tr><tr><td>1</td><td>1</td><td>0</td><td>1</td><td>74 %</td></tr><tr><td>1</td><td>1</td><td>1</td><td>0</td><td>72 %</td></tr><tr><td>1</td><td>1</td><td>1</td><td>1</td><td>70 %</td></tr></tbody></table>					THRES_MOV [3:0]				Description	D3	D2	D1	D0	1	0	0	0	84 %	1	0	0	1	82 %	1	0	1	0	80 %	1	0	1	1	78 %	1	1	0	0	76 %	1	1	0	1	74 %	1	1	1	0	72 %	1	1	1	1	70 %
	THRES_MOV [3:0]				Description																																																																																																							
	D3	D2	D1	D0																																																																																																								
	0	0	0	0	99 %																																																																																																							
	0	0	0	1	98 %																																																																																																							
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	1	1	0	1	74 %																																																																																																							
	1	1	1	0	72 %																																																																																																							
	1	1	1	1	70 %																																																																																																							
	THRES_STILL [3:0]: This parameter is used to set the ratio (percentage) of the maximum number of pixels that makes display image white (data = 63) in the total pixels by image process in the Still Picture mode. After this parameter sets the number of pixels that makes display image white, then the threshold grayscale value (DTH) that makes display image white is set so that the number of the pixels set by this parameter will not be changed.																																																																																																											
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Restriction	To enable this command, EXTC Command Set Enable Register (FFh) must be set first.														
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Sleep In	Yes														
Default	<table><tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr><tr><th>THRES_MOV [3:0]</th><th>THRES_STILL [3:0]</th></tr><tr><td>Power ON Sequence</td><td>4'b1011</td><td>4'b1011</td></tr><tr><td>S/W Reset</td><td>4'b1011</td><td>4'b1011</td></tr><tr><td>H/W Reset</td><td>4'b1011</td><td>4'b1011</td></tr></table>	Status	Default Value		THRES_MOV [3:0]	THRES_STILL [3:0]	Power ON Sequence	4'b1011	4'b1011	S/W Reset	4'b1011	4'b1011	H/W Reset	4'b1011	4'b1011
Status	Default Value														
	THRES_MOV [3:0]	THRES_STILL [3:0]													
Power ON Sequence	4'b1011	4'b1011													
S/W Reset	4'b1011	4'b1011													
H/W Reset	4'b1011	4'b1011													

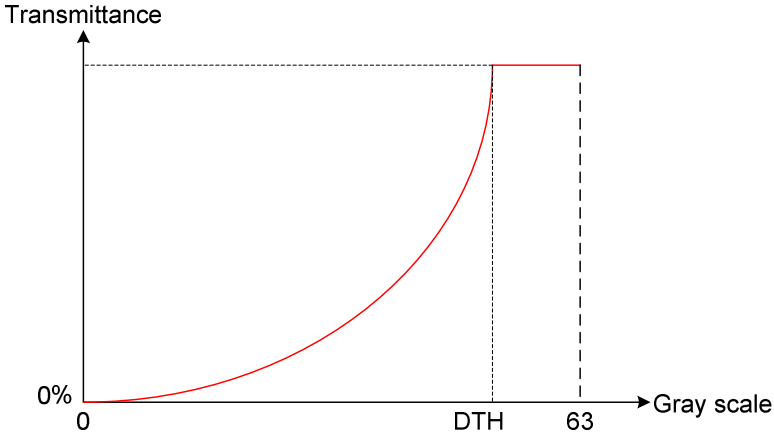
4.3.18. Backlight Control 3 (CAh)

CAh	BLCTRL3 (Backlight Control 3)																																																																																																											
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																																																															
Command	0	1	↑	XX	1	1	0	0	1	0	1	0	CAh																																																																																															
1 st Parameter	1	1	↑	XX	0	0	0	0	THRES_UI [3:0]				XX																																																																																															
Description	<p>THRES_UI [3:0]: This parameter is used to set the ratio (percentage) of the maximum number of pixels that makes display image white (data = 63) in the total pixels by image process in the UI (User Interface Image mode). After this parameter sets the number of pixels that makes display image white, then the threshold grayscale value (DTH) that makes display image white is set so that the number of the pixels set by this parameter will not be changed.</p>																																																																																																											
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<div><div>Histogram</div><div><div>100%</div><div>THRES_UI[3:0]</div><div>0%</div></div><div><div>0</div><div>DTH</div><div>63</div></div><div>Gray scale</div></div>																																																																																																												
Restriction	To enable this command, EXTC Command Set Enable Register (FFh) must be set first.																																																																																																											

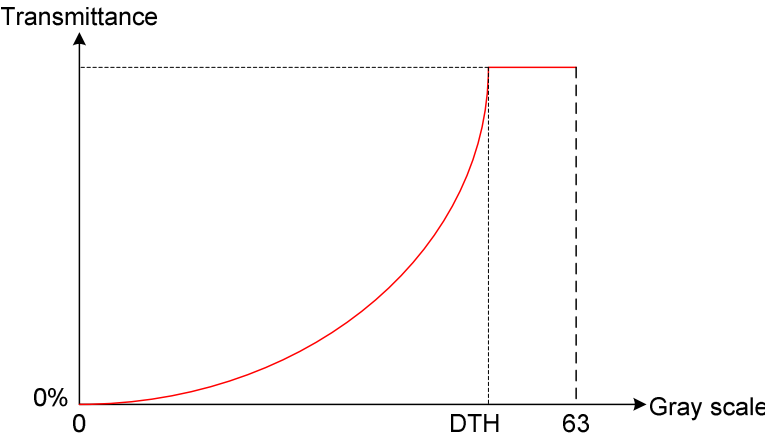
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
	Status	Availability												
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	Normal Mode On, Idle Mode On, Sleep Out	Yes												
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Sleep In	Yes													
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power ON Sequence</td><td>4'b1011</td></tr><tr><td>S/W Reset</td><td>4'b1011</td></tr><tr><td>H/W Reset</td><td>4'b1011</td></tr></table>		Status	Default Value	Power ON Sequence	4'b1011	S/W Reset	4'b1011	H/W Reset	4'b1011				
	Status	Default Value												
	Power ON Sequence	4'b1011												
	S/W Reset	4'b1011												
H/W Reset	4'b1011													

4.3.19. Backlight Control 4 (CBh)

CBh	BLCTRL4 (Backlight Control 4)																																																																																																										
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																																																														
Command	0	1	↑	XX	1	1	0	0	1	0	1	1	CBh																																																																																														
1 st Parameter	1	1	↑	XX	DTH_MOV [3:0]				DTH_STILL [3:0]				XX																																																																																														
Description	DTH_MOV [3:0]: This parameter is used to set the minimum limitation of the grayscale threshold value in the Moving Image mode.																																																																																																										
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	<div></div>														
Restriction	To enable this command, EXTC Command Set Enable Register (FFh) must be set first.														
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes		
Status	Availability														
Normal Mode On, Idle Mode Off, Sleep Out	Yes														
Normal Mode On, Idle Mode On, Sleep Out	Yes														
Partial Mode On, Idle Mode Off, Sleep Out	Yes														
Partial Mode On, Idle Mode On, Sleep Out	Yes														
Sleep In	Yes														
Default	<table><tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr><tr><th>DTH_MOV [3:0]</th><th>DTH_STILL [3:0]</th></tr><tr><td>Power ON Sequence</td><td>4'b1010</td><td>4'b1000</td></tr><tr><td>S/W Reset</td><td>4'b1010</td><td>4'b1000</td></tr><tr><td>H/W Reset</td><td>4'b1010</td><td>4'b1000</td></tr></table>	Status	Default Value		DTH_MOV [3:0]	DTH_STILL [3:0]	Power ON Sequence	4'b1010	4'b1000	S/W Reset	4'b1010	4'b1000	H/W Reset	4'b1010	4'b1000
Status	Default Value														
	DTH_MOV [3:0]	DTH_STILL [3:0]													
Power ON Sequence	4'b1010	4'b1000													
S/W Reset	4'b1010	4'b1000													
H/W Reset	4'b1010	4'b1000													

4.3.20. Backlight Control 5 (CCh)

CCh	BLCTRL5 (Backlight Control 5)													
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
Command	0	1	↑	XX	1	1	0	0	1	1	0	0	CCh	
1 st Parameter	1	1	↑	XX	0	0	0	0	DTH_UI [3:0]				XX	
Description	DTH_UI [3:0]: This parameter is used to set the minimum limitation of the grayscale threshold value in the UI (User Interface Image mode).													
	DTH_UI [3:0]				Description	DTH_UI [3:0]				Description				
	D3	D	D1	D0		D3	D2	D1	D0					
	0	0	0	0	252	1	0	0	0	220				
	0	0	0	1	248	1	0	0	1	216				
	0	0	1	0	244	1	0	1	0	212				
	0	0	1	1	240	1	0	1	1	208				
	0	1	0	0	236	1	1	0	0	204				
	0	1	0	1	232	1	1	0	1	200				
	0	1	1	0	228	1	1	1	0	196				
	0	1	1	1	224	1	1	1	1	192				
														
	Restriction	To enable this command, EXTC Command Set Enable Register (FFh) must be set first.												

Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
	Status	Availability												
	Normal Mode On, Idle Mode Off, Sleep Out	Yes												
	Normal Mode On, Idle Mode On, Sleep Out	Yes												
	Partial Mode On, Idle Mode Off, Sleep Out	Yes												
	Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes													
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power ON Sequence</td><td>4'b0100</td></tr><tr><td>S/W Reset</td><td>4'b0100</td></tr><tr><td>H/W Reset</td><td>4'b0100</td></tr></table>		Status	Default Value	Power ON Sequence	4'b0100	S/W Reset	4'b0100	H/W Reset	4'b0100				
	Status	Default Value												
	Power ON Sequence	4'b0100												
	S/W Reset	4'b0100												
H/W Reset	4'b0100													

4.3.21. Backlight Control 6 (CDh)

CDh	BLCTRL6 (Backlight Control 6)																																																			
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																							
Command	0	1	↑	XX	1	1	0	0	1	1	0	1	CDh																																							
1 st Parameter	1	1	↑	XX	0	DIM_MOV [2:0]			0	DIM_STILL [2:0]			XX																																							
Description	DIM_STILL [2:0]: This parameter is used to set the transition time of the brightness level change to avoid the sharp brightness change in the Still Picture mode.																																																			
	DIM_MOV [2:0]: This parameter is used to set the transition time of the brightness level change to avoid the sharp brightness change in the Moving Image mode.																																																			
	<table><tr><th colspan="3">DIM_MOV [2:0]/DIM_STILL [2:0]</th><th rowspan="2">Description</th></tr><tr><th>D2</th><th>D1</th><th>D0</th></tr><tr><td>0</td><td>0</td><td>0</td><td>1 frame</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1 frame</td></tr><tr><td>0</td><td>1</td><td>0</td><td>2 frames</td></tr><tr><td>0</td><td>1</td><td>1</td><td>4 frames</td></tr><tr><td>1</td><td>0</td><td>0</td><td>8 frames</td></tr><tr><td>1</td><td>0</td><td>1</td><td>16 frames</td></tr><tr><td>1</td><td>1</td><td>0</td><td>32 frames</td></tr><tr><td>1</td><td>1</td><td>1</td><td>64 frames</td></tr></table>													DIM_MOV [2:0]/DIM_STILL [2:0]			Description	D2	D1	D0	0	0	0	1 frame	0	0	1	1 frame	0	1	0	2 frames	0	1	1	4 frames	1	0	0	8 frames	1	0	1	16 frames	1	1	0	32 frames	1	1	1	64 frames
	DIM_MOV [2:0]/DIM_STILL [2:0]			Description																																																
	D2	D1	D0																																																	
	0	0	0	1 frame																																																
	0	0	1	1 frame																																																
	0	1	0	2 frames																																																
	0	1	1	4 frames																																																
	1	0	0	8 frames																																																
1	0	1	16 frames																																																	
1	1	0	32 frames																																																	
1	1	1	64 frames																																																	
<i>Note:</i> In the above picture, DIM1 [2:0] means DIM_MOV [2:0] , DIM_STILL [2:0] , and DIM_UI [2:0] are in different modes.																																																				

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Restriction	To enable this command, EXTC Command Set Enable Register (FFh) must be set first.		
Register Availability			
	Status		Availability
	Normal Mode On, Idle Mode Off, Sleep Out		Yes
	Normal Mode On, Idle Mode On, Sleep Out		Yes
	Partial Mode On, Idle Mode Off, Sleep Out		Yes
	Partial Mode On, Idle Mode On, Sleep Out		Yes
	Sleep In		Yes
Default			
	Status	Default Value	
		DIM_MOV [2:0]	DIM_STILL [2:0]
	Power ON Sequence	3'b100	3'b011
	S/W Reset	3'b100	3'b011
	H/W Reset	3'b100	3'b011

4.3.22. Backlight Control 7(CEh)

CEh	BLCTRL7 (Backlight Control 7)																																																			
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																							
Command	0	1	↑	XX	1	1	0	0	1	1	1	0	CEh																																							
1 st Parameter	1	1	↑	XX	DIM_MIN [3:0]				0	DIM_UI [2:0]		XX																																								
Description	DIM_UI [2:0]: This parameter is used to set the transition time of the brightness level change to avoid the sharp brightness change in the UI mode (User Interface Image mode).																																																			
	<table><tr><th colspan="3">DIM_UI [2:0]</th><th rowspan="2">Description</th></tr><tr><th>D2</th><th>D1</th><th>D0</th></tr><tr><td>0</td><td>0</td><td>0</td><td>1 frame</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1 frame</td></tr><tr><td>0</td><td>1</td><td>0</td><td>2 frames</td></tr><tr><td>0</td><td>1</td><td>1</td><td>4 frames</td></tr><tr><td>1</td><td>0</td><td>0</td><td>8 frames</td></tr><tr><td>1</td><td>0</td><td>1</td><td>16 frames</td></tr><tr><td>1</td><td>1</td><td>0</td><td>32 frames</td></tr><tr><td>1</td><td>1</td><td>1</td><td>64 frames</td></tr></table>													DIM_UI [2:0]			Description	D2	D1	D0	0	0	0	1 frame	0	0	1	1 frame	0	1	0	2 frames	0	1	1	4 frames	1	0	0	8 frames	1	0	1	16 frames	1	1	0	32 frames	1	1	1	64 frames
	DIM_UI [2:0]			Description																																																
	D2	D1	D0																																																	
	0	0	0	1 frame																																																
	0	0	1	1 frame																																																
	0	1	0	2 frames																																																
	0	1	1	4 frames																																																
	1	0	0	8 frames																																																
	1	0	1	16 frames																																																
1	1	0	32 frames																																																	
1	1	1	64 frames																																																	
<p>Note1: In the above picture, DIM1 [2:0] means DIM_MOV [2:0], DIM_STILL [2:0], and DIM_UI [2:0] are in different modes.</p> <p>Note2: In the above picture, DIM2 [3:0] means DIM_MIN [3:0].</p> <p>DIM_MIN [3:0]: This parameter is used to set the imitation of the minimum brightness change. If this parameter is larger than the difference between target brightness and current brightness, then the brightness will not change.</p>																																																				

Restriction	To enable this command, EXTC Command Set Enable Register (FFh) must be set first.																				
Register Availability	<table><tr><th>Status</th><th colspan="2">Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td colspan="2">Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td colspan="2">Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td colspan="2">Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td colspan="2">Yes</td></tr><tr><td>Sleep In</td><td colspan="2">Yes</td></tr></table>			Status	Availability		Normal Mode On, Idle Mode Off, Sleep Out	Yes		Normal Mode On, Idle Mode On, Sleep Out	Yes		Partial Mode On, Idle Mode Off, Sleep Out	Yes		Partial Mode On, Idle Mode On, Sleep Out	Yes		Sleep In	Yes	
	Status	Availability																			
	Normal Mode On, Idle Mode Off, Sleep Out	Yes																			
	Normal Mode On, Idle Mode On, Sleep Out	Yes																			
	Partial Mode On, Idle Mode Off, Sleep Out	Yes																			
	Partial Mode On, Idle Mode On, Sleep Out	Yes																			
Sleep In	Yes																				
Default	<table><tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr><tr><th>DIM_MIN [3:0]</th><th>DIM_UI [2:0]</th></tr><tr><td>Power ON Sequence</td><td>4'b0000</td><td>3'b010</td></tr><tr><td>S/W Reset</td><td>4'b0000</td><td>3'b010</td></tr><tr><td>H/W Reset</td><td>4'b0000</td><td>3'b010</td></tr></table>			Status	Default Value		DIM_MIN [3:0]	DIM_UI [2:0]	Power ON Sequence	4'b0000	3'b010	S/W Reset	4'b0000	3'b010	H/W Reset	4'b0000	3'b010				
	Status	Default Value																			
		DIM_MIN [3:0]	DIM_UI [2:0]																		
	Power ON Sequence	4'b0000	3'b010																		
	S/W Reset	4'b0000	3'b010																		
H/W Reset	4'b0000	3'b010																			

4.3.23. Backlight Control 8 (CFh)

CFh	BLCTRL8 (Backlight Control 8)																											
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX															
Command	0	1	↑	XX	1	1	0	0	1	1	1	1	CFh															
1 st Parameter	1	1	↑	XX	0	0	0	0	0	LEDONR	LEDONPOL	PWMPOL	XX															
Description	PWMPOL: The bit is used to define the polarity of the LEDPWM signal.																											
	<table><tr><th>BL</th><th>LEDPWMPOL</th><th>LEDPWM pin</th></tr><tr><td>0</td><td>0</td><td>Always low</td></tr><tr><td>0</td><td>1</td><td>Always high</td></tr><tr><td>1</td><td>0</td><td>Original polarity of PWM signal</td></tr><tr><td>1</td><td>1</td><td>Inversed polarity of PWM signal</td></tr></table>													BL	LEDPWMPOL	LEDPWM pin	0	0	Always low	0	1	Always high	1	0	Original polarity of PWM signal	1	1	Inversed polarity of PWM signal
	BL	LEDPWMPOL	LEDPWM pin																									
	0	0	Always low																									
	0	1	Always high																									
1	0	Original polarity of PWM signal																										
1	1	Inversed polarity of PWM signal																										
LEDONPOL: This bit is used to control the LEDON pin.																												
<table><tr><th>BL</th><th>LEDONPOL</th><th>LEDON pin</th></tr><tr><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>1</td></tr><tr><td>1</td><td>0</td><td>LEDONR</td></tr><tr><td>1</td><td>1</td><td>Inversed LEDONR</td></tr></table>													BL	LEDONPOL	LEDON pin	0	0	0	0	1	1	1	0	LEDONR	1	1	Inversed LEDONR	
BL	LEDONPOL	LEDON pin																										
0	0	0																										
0	1	1																										
1	0	LEDONR																										
1	1	Inversed LEDONR																										
LEDONR: This bit is used to control the LEDON pin.																												
<table><tr><th>LEDONR</th><th>Description</th></tr><tr><td>0</td><td>Low</td></tr><tr><td>1</td><td>High</td></tr></table>													LEDONR	Description	0	Low	1	High										
LEDONR	Description																											
0	Low																											
1	High																											
Restriction	To enable this command, EXTC Command Set Enable Register (FFh) must be set first.																											
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes			
Status	Availability																											
Normal Mode On, Idle Mode Off, Sleep Out	Yes																											
Normal Mode On, Idle Mode On, Sleep Out	Yes																											
Partial Mode On, Idle Mode Off, Sleep Out	Yes																											
Partial Mode On, Idle Mode On, Sleep Out	Yes																											
Sleep In	Yes																											

Default																
	<table><tr><th rowspan="2">Status</th><th colspan="3">Default Value</th></tr><tr><th>LEDONR</th><th>LEDONPOL</th><th>PWMPOL</th></tr><tr><td>Power On Sequence</td><td>1'b0</td><td>1'b0</td><td>1'b0</td></tr><tr><td>H/W Reset</td><td>1'b0</td><td>1'b0</td><td>1'b0</td></tr></table>	Status	Default Value			LEDONR	LEDONPOL	PWMPOL	Power On Sequence	1'b0	1'b0	1'b0	H/W Reset	1'b0	1'b0	1'b0
Status	Default Value															
	LEDONR	LEDONPOL	PWMPOL													
Power On Sequence	1'b0	1'b0	1'b0													
H/W Reset	1'b0	1'b0	1'b0													

4.3.24. NV Memory Write (D0h)

D0h				NVMWR (NV Memory Write)									
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	1	0	0	0	0	D0h
1 st Parameter	1	1	↑	XX	PGM_DATA [7:0]								XX
2 nd Parameter	1	1	↑	XX	PGM_ADR [7:0]								XX
Description	This command is used to program or read the NV memory data.												
	After a successful OTP operation, the information of PGM_DATA [7:0] will be programmed to the NV memory.												
	PGM_DATA [7:0]: The programmed data.												
	PGM_ADR [7:0]: Set the address of the NV memory for programming data. See “NV Memory Programming flow”.												
	PGM_ADR [7:0]		Programming data										
	8'h00		ID1										
	8'h 01		ID2										
8'h 02		ID3											
8'h 03		VCM											
8'h 3B		RB9h parameter 1											
8'h 3C		RB9h parameter 2											
Restriction	To enable this command, EXTC Command Set Enable Register (FFh) must be set first.												
Register Availability													
	Status						Availability						
	Normal Mode On, Idle Mode Off, Sleep Out						Yes						
	Normal Mode On, Idle Mode On, Sleep Out						Yes						
	Partial Mode On, Idle Mode Off, Sleep Out						Yes						
	Partial Mode On, Idle Mode On, Sleep Out						Yes						
Sleep In						Yes							
Default													
	Status		Default Value										
			PGM_ADR [7:0]/NVM_Read_ADR [7:0]							PGM_DATA [7:0]			
	Power ON Sequence		8'h00							8'h00			
	S/W Reset		No change							No change			
H/W Reset		8'h00							8'h00				

4.3.25. NV Memory Protection Key (D1h)

D1h	NVMPKEY (NV Memory Protection Key)																								
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	1	1	0	1	0	0	0	1	D1h												
1 st Parameter	1	1	↑	XX	KEY [23:16]								XX												
2 nd Parameter	1	1	↑	XX	KEY [15:8]								XX												
3 rd Parameter	1	1	↑	XX	KEY [7:0]								XX												
Description	<p>KEY [23:0]: NV memory programming protection key.</p> <p>Write an OTP data to D0h, this KEY [23:0] must set to 0x55AA66h to enable the OTP programming. If the KEY [23:0] is not 0 x 55AA66h, the NV Memory program will be aborted.</p>																								
Restriction	To enable this command, EXTC Command Set Enable Register (FFh) must be set first.																								
Register Availability	<table><thead><tr><th>Status</th><th>Availability</th></tr></thead><tbody><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></tbody></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><thead><tr><th>Status</th><th>Default Value</th></tr></thead><tbody><tr><td>Power ON Sequence</td><td>24'h000000h</td></tr><tr><td>S/W Reset</td><td>24'h000000h</td></tr></tbody></table>													Status	Default Value	Power ON Sequence	24'h000000h	S/W Reset	24'h000000h						
Status	Default Value																								
Power ON Sequence	24'h000000h																								
S/W Reset	24'h000000h																								

4.3.26. NV Memory Status Read (D2h)

D2h	RDNVM (NV Memory Status Read)												
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	1	0	0	1	0	D2h
1 st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
2 nd Parameter	1	↑	1	XX	0	ID2_Mk [2:0]			0	ID1_Mk [2:0]			XX
3 rd Parameter	1	↑	1	XX	OTP Busy	VCM_Mk [2:0]			0	ID3_Mk [2:0]			XX
4 th Parameter	1	↑	1	XX	0	0	0	0	RB9_P2_Mk		RB9_P1_Mk		XX
Description	The register uses a mark to record the NV memory programmed time. The bits are increase “+1” automatically after writing the PGM_DATA [7:0] to the NV memory.												
	ID1_Mk [2:0]/ID2_Mk [2:0]/ID3_Mk [2:0]/VCM_Mk [2:0]:												
	ID1_MK [2:0]/ID2_MK [2:0]/ID3_MK [2:0]/VCM_MK [2:0]								Description				
	0				0		0		No Programmed				
	0				0		1		Programmed 1 time already				
	0				1		1		Programmed 2 times already				
	1				1		1		Programmed 3 times already				
	RB9_P1_Mk: Include MY_Panel, MX_Panel, MV_Panel, ML_Panel, BGR_Panel, MH_Panel,SS_Panel, GS_Panel bits												
	RB9_P2_Mk: Include REV_Panel, SM_Panel bits												
	RB9_P1_Mk [2:0]/RB9_P1_Mk [2:0]								Description				
0				0		No Programmed							
0				1		Programmed 1 time already							
1				1		Programmed 2 times already							
OTP Busy: The status bit of the NV memory programming.													
BUSY						The Status of NV Memory							
0						Idle							
1						Busy							
Restriction	To enable this command, EXTC Command Set Enable Register (FFh) must be set first.												

Register Availability	Status		Availability	
	Normal Mode On, Idle Mode Off, Sleep Out		Yes	
	Normal Mode On, Idle Mode On, Sleep Out		Yes	
	Partial Mode On, Idle Mode Off, Sleep Out		Yes	
	Partial Mode On, Idle Mode On, Sleep Out		Yes	
	Sleep In		Yes	

Default	Status	Default Value						
		ID3_ Mk [2:0]	ID2_ Mk [2:0]	ID1_ Mk [2:0]	VCM_ Mk [2:0]	OTP Busy	RB9_P1_MK	RB9_P2_MK
	Power ON Sequence	3'b000	3'b000	3'b000	3'b000	0	2'b00	2'b00
	S/W Reset	3'b000	3'b000	3'b000	3'b000	0	2'b00	2'b00

4.3.27. Engineering Setting (DFh)

DFh	Engineering Setting																								
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	1	1	0	1	1	1	1	1	DFh												
1 st Parameter	1	1	↑	XX	0	0	0	0	0	0	0	0	00												
2 nd Parameter	1	1	↑	XX	0	0	0	0	0	0	0	0	00												
3 rd Parameter	1	1	↑	XX	0	0	0	0	0	0	0	0	00												
4 th Parameter	1	1	↑	XX	0	0	0	0	0	0	0	0	00												
5 th Parameter	1	1	↑	XX	0	0	0	0	0	0	0	0	00												
6 th Parameter	1	1	↑	XX	0	0	dsi_pclk_div	0	0	0	0	0	00												
Description	MIPI internal PCLK setting.																								
	When dsi_pclk_div set 0 → Freq. = MIPI PCLK / 2																								
	When dsi_pclk_div set 1 → Freq. = MIPI PCLK																								
Restriction	To enable this command, EXTC Command Set Enable Register (FFh) must be set first.																								
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
														Status	Availability										
														Normal Mode On, Idle Mode Off, Sleep Out	Yes										
														Normal Mode On, Idle Mode On, Sleep Out	Yes										
														Partial Mode On, Idle Mode Off, Sleep Out	Yes										
														Partial Mode On, Idle Mode On, Sleep Out	Yes										
Sleep In	Yes																								
Default	<table><tr><th rowspan="2">Status</th><th>Default Value</th></tr><tr><th>dsi_pclk_div</th></tr><tr><td>Power ON Sequence</td><td>1'b0</td></tr><tr><td>S/W Reset</td><td>No Change</td></tr><tr><td>H/W Reset</td><td>1'b0</td></tr></table>													Status	Default Value	dsi_pclk_div	Power ON Sequence	1'b0	S/W Reset	No Change	H/W Reset	1'b0			
															Status	Default Value									
														dsi_pclk_div											
														Power ON Sequence	1'b0										
														S/W Reset	No Change										
H/W Reset	1'b0																								

4.3.28. Positive Gamma Control (E0h)

E0h	PGAMCTRL (Positive Gamma Control)																								
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	1	1	1	0	0	0	0	0	E0h												
1 st Parameter	1	1	↑	XX	0	0	VP0 [5:0]						XX												
2 nd Parameter	1	1	↑	XX	0	0	VP4 [5:0]						XX												
3 rd Parameter	1	1	↑	XX	0	0	VP8 [5:0]						XX												
4 th Parameter	1	1	↑	XX	0	0	0	VP16 [4:0]					XX												
5 th Parameter	1	1	↑	XX	0	0	0	VP32 [4:0]					XX												
6 th Parameter	1	1	↑	XX	0	0	0	VP52 [4:0]					XX												
7 th Parameter	1	1	↑	XX	0	0	0	0	VP80 [3:0]				XX												
8 th Parameter	1	1	↑	XX	0	0	0	0	VP108 [3:0]				XX												
9 th Parameter	1	1	↑	XX	0	0	0	0	VP147 [3:0]				XX												
10 th Parameter	1	1	↑	XX	0	0	0	0	VP175 [3:0]				XX												
11 th Parameter	1	1	↑	XX	0	0	0	VP203 [4:0]					XX												
12 th Parameter	1	1	↑	XX	0	0	0	VP223 [4:0]					XX												
13 th Parameter	1	1	↑	XX	0	0	0	VP239 [4:0]					XX												
14 th Parameter	1	1	↑	XX	0	0	VP247 [5:0]						XX												
15 th Parameter	1	1	↑	XX	0	0	VP251 [5:0]						XX												
16 th Parameter	1	1	↑	XX	0	0	VP255 [5:0]						XX												
Description	Set the gray scale voltage to adjust the Gamma characteristics of the TFT panel.																								
Restriction	To enable this command, EXTC Command Set Enable Register (FFh) must be set first.																								
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								

4.3.29. Negative Gamma Correction (E1h)

E1h	NGAMCTRL (Negative Gamma Correction)																								
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	1	1	1	0	0	0	0	1	E1h												
1 st Parameter	1	1	↑	XX	0	0	VN0 [5:0]						XX												
2 nd Parameter	1	1	↑	XX	0	0	VN4 [5:0]						XX												
3 rd Parameter	1	1	↑	XX	0	0	VN8 [5:0]						XX												
4 th Parameter	1	1	↑	XX	0	0	0	VN16 [4:0]					XX												
5 th Parameter	1	1	↑	XX	0	0	0	VN32 [4:0]					XX												
6 th Parameter	1	1	↑	XX	0	0	0	VN52 [4:0]					XX												
7 th Parameter	1	1	↑	XX	0	0	0	0	VN80 [3:0]				XX												
8 th Parameter	1	1	↑	XX	0	0	0	0	VN108 [3:0]				XX												
9 th Parameter	1	1	↑	XX	0	0	0	0	VN147 [3:0]				XX												
10 th Parameter	1	1	↑	XX	0	0	0	0	VN175 [3:0]				XX												
11 th Parameter	1	1	↑	XX	0	0	0	VN203 [4:0]					XX												
12 th Parameter	1	1	↑	XX	0	0	0	VN223 [4:0]					XX												
13 th Parameter	1	1	↑	XX	0	0	0	VN239 [4:0]					XX												
14 th Parameter	1	1	↑	XX	0	0	VN247 [5:0]						XX												
15 th Parameter	1	1	↑	XX	0	0	VN251 [5:0]						XX												
16 th Parameter	1	1	↑	XX	0	0	VN255 [5:0]						XX												
Description	Set the gray scale voltage to adjust the Gamma characteristics of the TFT panel.																								
Restriction	To enable this command, EXTC Command Set Enable Register (FFh) must be set first.																								
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode OFF, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode OFF, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode OFF, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								

4.3.30. Digital Gamma Control 1 (E2h)

E2h	DGAMCTRL (Digital Gamma Control 1)																								
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	1	1	1	0	0	0	1	0	E2h												
1 st Parameter	1	1	↑	XX	RCA0 [3:0]				BCA0 [3:0]				XX												
:	1	1	↑	XX	RCAx [3:0]				BCAx [3:0]				XX												
64 th Parameter	1	1	↑	XX	RCA63 [3:0]				BCA63 [3:0]				XX												
Description	RCAx [3:0]: Gamma Macro-adjustment registers for red Gamma curve. BCAx [3:0]: Gamma Macro-adjustment registers for blue Gamma curve. See the 3 Gamma setting flow in the chapter 16. Note : 3 Gamma setting only support MIPI Low Power mode operation.																								
Restriction	To enable this command, EXTC Command Set Enable Register (FFh) must be set first.																								
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								

4.3.31. Digital Gamma Control 2 (E3h)

E3h	DGAMCTRL (Digital Gamma Control 2)																								
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	1	1	1	0	0	0	1	1	E3h												
1 st Parameter	1	1	↑	XX	RFA0 [3:0]				BFA0 [3:0]				XX												
:					:				:				XX												
x th Parameter	1	1	↑	XX	RFAx [3:0]				BFAx [3:0]				XX												
:					:				:				XX												
256 th Parameter	1	1	↑	XX	RFA256 [3:0]				BFA256 [3:0]				XX												
257 th Parameter	1	1	↑	XX	0	0	0	0	0	0	0	0	00												
Description	RFAx [3:0]: Gamma Micro-adjustment registers for red Gamma curve. BFAx [3:0]: Gamma Micro-adjustment registers for blue Gamma curve. 257 th Parameter enables the register E3h setting value. See the 3 Gamma setting flow in the chapter 16. Note : 3 Gamma setting only support MIPI Low Power mode operation.																								
Restriction	To enable this command, EXTC Command Set Enable Register (FFh) must be set first.																								
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								

4.3.32. Digital 3 Gamma Enable (EAh)

EAh	D3GE (Digital 3 Gamma Enable)																								
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	1	1	1	0	1	0	1	0	EAh												
1 st Parameter	1	1	↑	XX	0	0	0	0	0	0	En_3G	Dith_en	00												
Description	En_3G:																								
	1: digital 3 gamma enable																								
	0: digital 3 gamma disable																								
	Dith_en:																								
	1: dithering function enable																								
	0: dithering function disable																								
Restriction	To enable this command, EXTC Command Set Enable Register (FFh) must be set first.																								
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power ON Sequence</td><td>8'h00</td></tr><tr><td>S/W Reset</td><td>No Change</td></tr><tr><td>H/W Reset</td><td>8'h00</td></tr></table>													Status	Default Value	Power ON Sequence	8'h00	S/W Reset	No Change	H/W Reset	8'h00				
Status	Default Value																								
Power ON Sequence	8'h00																								
S/W Reset	No Change																								
H/W Reset	8'h00																								

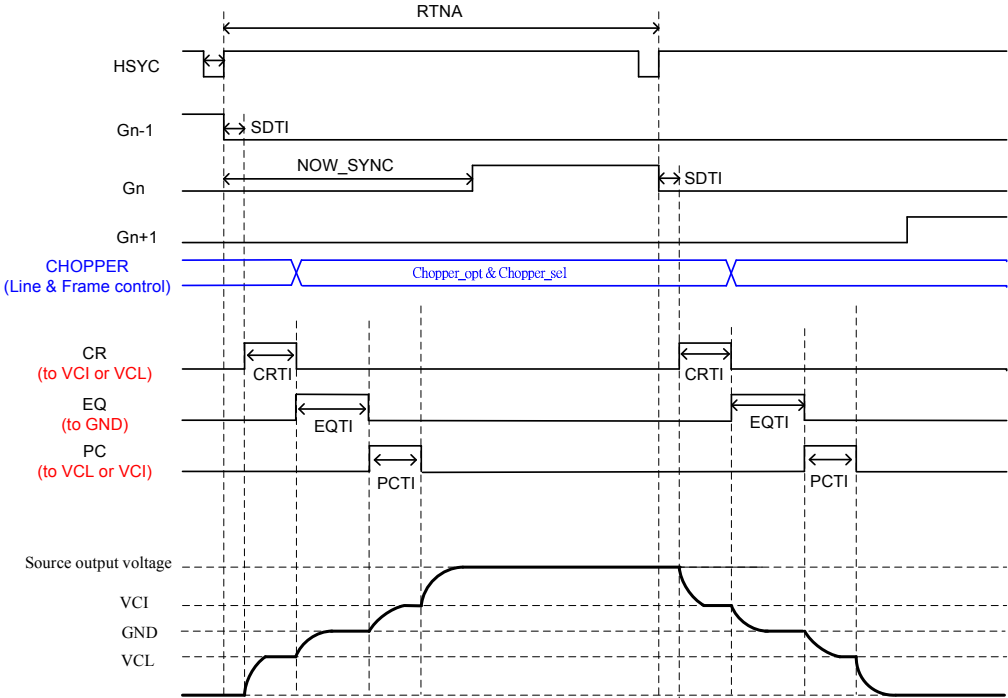
4.3.33. VGMP / VGMN / VGSP / VGSN Voltage Measurement Set (EDh)

EDh	VGMP / VGMN / VGSP / VGSN Voltage Measurement Set																								
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	1	1	1	0	1	1	0	1	EDh												
1 st parameter	1	1	↑	XX	0	1	1	1	1	1	1	1	7F												
2 nd parameter	1	1	↑	XX	0	0	0	0	en_volt_reg	1	1	1	07												
Description	en_volt_reg: 1: Enable VGMP / VGMN /VGSP / VGSN voltage to output 0: disable VGMP / VGMN /VGSP / VGSN voltage to output																								
Restriction	To enable this command, EXTC Command Set Enable Register (FFh) must be set first.																								
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td></td><td>en_volt_reg</td></tr><tr><td>Power ON Sequence</td><td>1'b0</td></tr><tr><td>S/W Reset</td><td>No Change</td></tr><tr><td>H/W Reset</td><td>1'b0</td></tr></table>													Status	Default Value		en_volt_reg	Power ON Sequence	1'b0	S/W Reset	No Change	H/W Reset	1'b0		
Status	Default Value																								
	en_volt_reg																								
Power ON Sequence	1'b0																								
S/W Reset	No Change																								
H/W Reset	1'b0																								

4.3.34. Panel Timing Control 1 (F1h)

F1h	PTCTRL1 (Panel Timing Control 1)																																																
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HE X																																				
Command	0	1	↑	XX	1	1	1	1	0	0	0	1	F1h																																				
1 st Parameter	1	1	↑	XX	0	0	1	0	1	0	0	1	29																																				
2 nd Parameter	1	1	↑	XX	Chopper_opt	Chopper_sel [1:0]		0	1	0	1	0	CA																																				
3 rd Parameter	1	1	↑	XX	0	0	Outsre	0	0	1	1	1	07																																				
Description	Chopper_opt: Source Op-amp chopper function option																																																
	Chopper_sel [1:0]: Source Op-amp chopper function option																																																
	<table><tr><th>Chopper_opt</th><th>Chopper_sel [1]</th><th>Chopper_sel [0]</th><th>Description</th></tr><tr><td>0</td><td>0</td><td>0</td><td>chopper disable</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1 frame chopper</td></tr><tr><td>0</td><td>1</td><td>0</td><td>2 frame chopper</td></tr><tr><td>0</td><td>1</td><td>1</td><td>3 frame chopper</td></tr><tr><td>1</td><td>0</td><td>0</td><td>1 line chopper (1 frame chopper polarity change)</td></tr><tr><td>1</td><td>0</td><td>1</td><td>2 line chopper (1 frame chopper polarity change)</td></tr><tr><td>1</td><td>1</td><td>0</td><td>1 line chopper (2 frame chopper polarity change)</td></tr><tr><td>1</td><td>1</td><td>1</td><td>2 line chopper (2 frame chopper polarity change)</td></tr></table>													Chopper_opt	Chopper_sel [1]	Chopper_sel [0]	Description	0	0	0	chopper disable	0	0	1	1 frame chopper	0	1	0	2 frame chopper	0	1	1	3 frame chopper	1	0	0	1 line chopper (1 frame chopper polarity change)	1	0	1	2 line chopper (1 frame chopper polarity change)	1	1	0	1 line chopper (2 frame chopper polarity change)	1	1	1	2 line chopper (2 frame chopper polarity change)
	Chopper_opt	Chopper_sel [1]	Chopper_sel [0]	Description																																													
	0	0	0	chopper disable																																													
	0	0	1	1 frame chopper																																													
	0	1	0	2 frame chopper																																													
	0	1	1	3 frame chopper																																													
	1	0	0	1 line chopper (1 frame chopper polarity change)																																													
	1	0	1	2 line chopper (1 frame chopper polarity change)																																													
1	1	0	1 line chopper (2 frame chopper polarity change)																																														
1	1	1	2 line chopper (2 frame chopper polarity change)																																														
Outsre: Increase SRC Opamp output driving ability. 0:normal driving, 1:double driving																																																	
Restriction	To enable this command, EXTC Command Set Enable Register (FFh) must be set first.																																																
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes																								
Status	Availability																																																
Normal Mode On, Idle Mode Off, Sleep Out	Yes																																																
Normal Mode On, Idle Mode On, Sleep Out	Yes																																																
Partial Mode On, Idle Mode Off, Sleep Out	Yes																																																
Partial Mode On, Idle Mode On, Sleep Out	Yes																																																
Sleep In	Yes																																																
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td rowspan="3">Power ON Sequence</td><td>1st Parameter = 8'h29</td></tr><tr><td>2nd Parameter = 8'hCA</td></tr><tr><td>3rd Parameter = 8'h07</td></tr><tr><td>S/W Reset</td><td>No Change</td></tr><tr><td rowspan="3">H/W Reset</td><td>1st Parameter = 8'h29</td></tr><tr><td>2nd Parameter = 8'hCA</td></tr><tr><td>3rd Parameter = 8'h07</td></tr></table>													Status	Default Value	Power ON Sequence	1 st Parameter = 8'h29	2 nd Parameter = 8'hCA	3 rd Parameter = 8'h07	S/W Reset	No Change	H/W Reset	1 st Parameter = 8'h29	2 nd Parameter = 8'hCA	3 rd Parameter = 8'h07																								
Status	Default Value																																																
Power ON Sequence	1 st Parameter = 8'h29																																																
	2 nd Parameter = 8'hCA																																																
	3 rd Parameter = 8'h07																																																
S/W Reset	No Change																																																
H/W Reset	1 st Parameter = 8'h29																																																
	2 nd Parameter = 8'hCA																																																
	3 rd Parameter = 8'h07																																																

4.3.35. Panel Timing Control 2 (F2h)

F2h	PTCTRL2 (Panel Timing Control 2)													
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
Command	0	1	↑	XX	1	1	1	1	0	0	1	0	F2h	
1 st Parameter	1	1	↑	XX	SDTI [1:0]		0	0	0	CRTI [2:0]			40	
2 nd Parameter	1	1	↑	XX	1	1	0	1	0	EQTI [2:0]			D2	
3 rd Parameter	1	1	↑	XX	0	creqpc		0	1	0	PCTI [2:0]		52	
4 th Parameter	1	1	↑	XX	0	0	1	0	1	0	SDTI [2]	0	2A	
Description	<p>SDTI [2:0]: Source SDT timing adjustment (time scale: internal op_clk).</p> <p>The timing can be adjusted 0 to 7 time scales.</p> <p>CRTI [2:0]: Source CR timing adjustment (time scale: internal op_clk).</p> <p>The timing can be adjusted 0 to 7 time scales.</p> <p>EQTI [2:0]: Source EQ timing adjustment (time scale: internal op_clk).</p> <p>The timing can be adjusted 1 to 8 time scales.</p> <p>PCTI [2:0]: Source PC timing adjustment (time scale: internal op_clk).</p> <p>The timing can be adjusted 0 to 7 time scales.</p> <p>creqpc: CR/EQ/PC function enable signal</p> 													
	Restriction													
	To enable this command, EXTC Command Set Enable Register (FFh) must be set first.													
	Register Availability													

Default		Status	Default Value
		Power ON Sequence	1 st Parameter = 8'h40 2 nd Parameter = 8'hD2 3 rd Parameter = 8'h52 4 th Parameter = 8'h2A
		S/W Reset	No Change
		H/W Reset	1 st Parameter = 8'h40 2 nd Parameter = 8'hD2 3 rd Parameter = 8'h52 4 th Parameter = 8'h2A

4.3.36. DVDD Voltage Setting (F3h)

F3h	DVDD Voltage Setting																														
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX																		
Command	0	1	↑	XX	1	1	1	1	0	0	1	1	F3h																		
1 st parameter	1	1	↑	XX	0	1	1	reg_vd[2:0]			0	0	70																		
Description	reg_vd [2:0]: Select DVDD regulator voltage level																														
	<table><tr><th>reg_vd[2:0]</th><th>DVDD Voltage(V)</th></tr><tr><td>3'h00</td><td>1.5 V</td></tr><tr><td>3'h01</td><td>setting prohibited</td></tr><tr><td>3'h02</td><td>setting prohibited</td></tr><tr><td>3'h03</td><td>setting prohibited</td></tr><tr><td>3'h04</td><td>1.6 V</td></tr><tr><td>3'h05</td><td>1.6 V</td></tr><tr><td>3'h06</td><td>1.7 V</td></tr><tr><td>3'h07</td><td>1.7 V</td></tr></table>													reg_vd[2:0]	DVDD Voltage(V)	3'h00	1.5 V	3'h01	setting prohibited	3'h02	setting prohibited	3'h03	setting prohibited	3'h04	1.6 V	3'h05	1.6 V	3'h06	1.7 V	3'h07	1.7 V
	reg_vd[2:0]	DVDD Voltage(V)																													
	3'h00	1.5 V																													
	3'h01	setting prohibited																													
	3'h02	setting prohibited																													
	3'h03	setting prohibited																													
	3'h04	1.6 V																													
	3'h05	1.6 V																													
	3'h06	1.7 V																													
3'h07	1.7 V																														
Restriction	To enable this command, EXTC Command Set Enable Register (FFh) must be set first.																														
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Idle Mode Off, Sleep Out	Yes	Idle Mode On, Sleep Out	Yes	Sleep In	Yes						
Status	Availability																														
Normal Mode On, Idle Mode Off, Sleep Out	Yes																														
Normal Mode On, Idle Mode On, Sleep Out	Yes																														
Idle Mode Off, Sleep Out	Yes																														
Idle Mode On, Sleep Out	Yes																														
Sleep In	Yes																														
Default	<table><tr><th rowspan="2">Status</th><th>Default Value</th></tr><tr><th>reg_vd[2:0]</th></tr><tr><td>Power ON Sequence</td><td>3'b100</td></tr><tr><td>S/W Reset</td><td>No Change</td></tr><tr><td>H/W Reset</td><td>3'b100</td></tr></table>													Status	Default Value	reg_vd[2:0]	Power ON Sequence	3'b100	S/W Reset	No Change	H/W Reset	3'b100									
Status	Default Value																														
	reg_vd[2:0]																														
Power ON Sequence	3'b100																														
S/W Reset	No Change																														
H/W Reset	3'b100																														

4.3.37. Power Control 5 (F5h)

F5h	PWCTRL 5 (Power Control 5)																																																
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																				
Command	0	1	↑	XX	1	1	1	1	0	1	0	1	F5h																																				
1 st parameter	1	1	↑	XX	0	1	0	0	0	0	1	0	42h																																				
2 nd parameter	1	1	↑	XX	0	0	0	0	0	1	0	0	04h																																				
3 rd parameter	1	1	↑	XX	1	0	VRGH[5:0]						80h																																				
Description	VRGH [5:0]: Select AVDD regulator voltage level																																																
	<table><tr><th>VRGH[5:0]</th><th>Spec(V)</th></tr><tr><td>8'h00</td><td>1</td></tr><tr><td>8'h01</td><td>1.1</td></tr><tr><td>8'h02</td><td>1.2</td></tr><tr><td>8'h03</td><td>1.3</td></tr><tr><td>8'h04</td><td>1.4</td></tr><tr><td>8'h05</td><td>1.5</td></tr><tr><td>8'h06</td><td>1.6</td></tr><tr><td>8'h07</td><td>1.7</td></tr><tr><td>8'h08</td><td>1.8</td></tr><tr><td>8'h09</td><td>1.9</td></tr><tr><td>8'h0A</td><td>2</td></tr><tr><td colspan="2">...</td></tr><tr><td>8'h2F</td><td>5.7</td></tr><tr><td>8'h30</td><td>5.8</td></tr><tr><td>8'h31</td><td>5.9</td></tr><tr><td>8'h32</td><td>6</td></tr><tr><td>8'h33 → 8'h3F</td><td>6</td></tr></table>													VRGH[5:0]	Spec(V)	8'h00	1	8'h01	1.1	8'h02	1.2	8'h03	1.3	8'h04	1.4	8'h05	1.5	8'h06	1.6	8'h07	1.7	8'h08	1.8	8'h09	1.9	8'h0A	2	...		8'h2F	5.7	8'h30	5.8	8'h31	5.9	8'h32	6	8'h33 → 8'h3F	6
	VRGH[5:0]	Spec(V)																																															
	8'h00	1																																															
	8'h01	1.1																																															
	8'h02	1.2																																															
	8'h03	1.3																																															
	8'h04	1.4																																															
	8'h05	1.5																																															
	8'h06	1.6																																															
	8'h07	1.7																																															
	8'h08	1.8																																															
	8'h09	1.9																																															
	8'h0A	2																																															
	...																																																
	8'h2F	5.7																																															
	8'h30	5.8																																															
	8'h31	5.9																																															
	8'h32	6																																															
	8'h33 → 8'h3F	6																																															
Restriction	To enable this command, EXTC Command Set Enable Register (FFh) must be set first.																																																
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Idle Mode Off, Sleep Out	Yes	Idle Mode On, Sleep Out	Yes	Sleep In	Yes																								
Status	Availability																																																
Normal Mode On, Idle Mode Off, Sleep Out	Yes																																																
Normal Mode On, Idle Mode On, Sleep Out	Yes																																																
Idle Mode Off, Sleep Out	Yes																																																
Idle Mode On, Sleep Out	Yes																																																
Sleep In	Yes																																																
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power ON Sequence</td><td>3rd parameter = 8'h80</td></tr><tr><td>S/W Reset</td><td>No Change</td></tr><tr><td>H/W Reset</td><td>3rd parameter = 8'h80</td></tr></table>													Status	Default Value	Power ON Sequence	3 rd parameter = 8'h80	S/W Reset	No Change	H/W Reset	3 rd parameter = 8'h80																												
Status	Default Value																																																
Power ON Sequence	3 rd parameter = 8'h80																																																
S/W Reset	No Change																																																
H/W Reset	3 rd parameter = 8'h80																																																

4.3.38. Panel Resolution Selection Set (F7h)

F7h	Panel Resolution Selection Set																								
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	1	1	1	1	0	1	1	1	F7h												
1 st parameter	1	1	↑	XX	1	0	0	0	0	rso_in_test_mode[2:0]			80												
Description	Rso_in_test_mode[2:0] : 000 : 480x864 resolution 001 : 480x854 resolution 010 : 480x800 resolution 011 : 480x640 resolution 100 : 480x720 resolution																								
Restriction	To enable this command, EXTC Command Set Enable Register (FFh) must be set first.																								
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>1st Parameter = 8'h80</td></tr><tr><td>S/W Reset</td><td>No Change</td></tr><tr><td>H/W Reset</td><td>1st Parameter = 8'h80</td></tr></table>													Status	Default Value	Power On Sequence	1 st Parameter = 8'h80	S/W Reset	No Change	H/W Reset	1 st Parameter = 8'h80				
Status	Default Value																								
Power On Sequence	1 st Parameter = 8'h80																								
S/W Reset	No Change																								
H/W Reset	1 st Parameter = 8'h80																								

4.3.39. Read EXTC Command In SPI Mode (FBh)

FBh	RDEXTCSPI(Read EXTC command In SPI)																								
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	1	1	1	1	1	0	1	1	FBh												
1 st Parameter	1	1	↑	XX	ext_spi_read_en	ext_spi_cnt [6:0]							XX												
2 nd Parameter	1	1	↑	XX	0	0	0	0	0	0	ext_spi_cnt [8:7]		XX												
Description	<div>ext_spi_read_en: enable the read function of the EXTC Command in the SPI operation mode</div> <div>ext_spi_cnt [8:0]: the Nth parameter which wants to be read out</div> <div><div><div>START</div><div>Read the EXTC command in SPI operation mode (Example: read Register XXh, Nth parameter)</div><div>EXTC Command Set enable register (FFh) 1st Parameter : FFh 2nd Parameter : 98h 3rd Parameter : 06h</div><div>Set Register FBh 1. enable SPI read (ext_spi_read_en=1) 2. Nth parameter to be read out (ext_spi_cnt[8:0])</div><div>Set Register XXh command And read out the Nth Parameter</div><div>END SPI read</div><div>Set Register FBh Disable SPI read (ext_spi_read_en=0) (Enable SPI write)</div></div><div>Read others command / Parameter</div></div>																								
Restriction																									
Register Availability	<table><thead><tr><th>Status</th><th>Availability</th></tr></thead><tbody><tr><td>Normal Mode On, Idle Mode Off Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></tbody></table>													Status	Availability	Normal Mode On, Idle Mode Off Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><thead><tr><th>Status</th><th>Default Value</th></tr></thead><tbody><tr><td>Power ON Sequence</td><td>1st Parameter = 8'h00 2nd Parameter = 8'h00</td></tr><tr><td>S/W Reset</td><td>1st Parameter = 8'h00 2nd Parameter = 8'h00</td></tr><tr><td>H/W Reset</td><td>1st Parameter = 8'h00 2nd Parameter = 8'h00</td></tr></tbody></table>													Status	Default Value	Power ON Sequence	1 st Parameter = 8'h00 2 nd Parameter = 8'h00	S/W Reset	1 st Parameter = 8'h00 2 nd Parameter = 8'h00	H/W Reset	1 st Parameter = 8'h00 2 nd Parameter = 8'h00				
Status	Default Value																								
Power ON Sequence	1 st Parameter = 8'h00 2 nd Parameter = 8'h00																								
S/W Reset	1 st Parameter = 8'h00 2 nd Parameter = 8'h00																								
H/W Reset	1 st Parameter = 8'h00 2 nd Parameter = 8'h00																								

4.3.40. LVGL Voltage Setting (FCh)

FCh	LVGL Voltage Setting																																														
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																		
Command	0	1	↑	XX	1	1	1	1	1	1	0	0	FCh																																		
1 st parameter	1	1	↑	XX	0	0	0	EXB1T_IN	LVGL_SEL[3:0]				04																																		
Description	EXB1T_IN : Select the AVDD / AVEE power source. EXB1T_IN bit = 0 , AVDD / AVEE generated by internal pumping. EXB1T_IN bit = 1 , AVDD / AVEE generated by external pumping source(ex. ILI4002). LVGL_SEL[3:0]: Select VGL regulator voltage level.																																														
	<table><tr><th>LVGL_SEL[3:0]</th><th>Spec (V)</th></tr><tr><td>4'h0</td><td>N/A</td></tr><tr><td>4'h1</td><td>N/A</td></tr><tr><td>4'h2</td><td>N/A</td></tr><tr><td>4'h3</td><td>N/A</td></tr><tr><td>4'h4</td><td>-6</td></tr><tr><td>4'h5</td><td>-7</td></tr><tr><td>4'h6</td><td>-8</td></tr><tr><td>4'h7</td><td>-9</td></tr><tr><td>4'h8</td><td>-10</td></tr><tr><td>4'h9</td><td>-11</td></tr><tr><td>4'hA</td><td>-12</td></tr><tr><td>4'hB</td><td>-13</td></tr><tr><td>4'hC</td><td>-14</td></tr><tr><td>4'hD</td><td>-15</td></tr><tr><td>4'hE</td><td>-16</td></tr><tr><td>4'hF</td><td>-17</td></tr></table>													LVGL_SEL[3:0]	Spec (V)	4'h0	N/A	4'h1	N/A	4'h2	N/A	4'h3	N/A	4'h4	-6	4'h5	-7	4'h6	-8	4'h7	-9	4'h8	-10	4'h9	-11	4'hA	-12	4'hB	-13	4'hC	-14	4'hD	-15	4'hE	-16	4'hF	-17
	LVGL_SEL[3:0]	Spec (V)																																													
	4'h0	N/A																																													
	4'h1	N/A																																													
	4'h2	N/A																																													
	4'h3	N/A																																													
	4'h4	-6																																													
	4'h5	-7																																													
	4'h6	-8																																													
4'h7	-9																																														
4'h8	-10																																														
4'h9	-11																																														
4'hA	-12																																														
4'hB	-13																																														
4'hC	-14																																														
4'hD	-15																																														
4'hE	-16																																														
4'hF	-17																																														
LVGL>VGL+2V																																															
Restriction	To enable this command, EXTC Command Set Enable Register (FFh) must be set first.																																														
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes																						
Status	Availability																																														
Normal Mode On, Idle Mode Off, Sleep Out	Yes																																														
Normal Mode On, Idle Mode On, Sleep Out	Yes																																														
Partial Mode On, Idle Mode Off, Sleep Out	Yes																																														
Partial Mode On, Idle Mode On, Sleep Out	Yes																																														
Sleep In	Yes																																														
Default	<table><tr><th rowspan="2">Status</th><th>Default Value</th><th>Default Value</th></tr><tr><th>EXB1T_IN</th><th>LVGL_SEL[3:0]</th></tr><tr><td>Power On Sequence</td><td>1'b0</td><td>4'b0100</td></tr><tr><td>S/W Reset</td><td>No Change</td><td>No Change</td></tr><tr><td>H/W Reset</td><td>1'b0</td><td>4'b0100</td></tr></table>													Status	Default Value	Default Value	EXB1T_IN	LVGL_SEL[3:0]	Power On Sequence	1'b0	4'b0100	S/W Reset	No Change	No Change	H/W Reset	1'b0	4'b0100																				
Status	Default Value	Default Value																																													
	EXB1T_IN	LVGL_SEL[3:0]																																													
Power On Sequence	1'b0	4'b0100																																													
S/W Reset	No Change	No Change																																													
H/W Reset	1'b0	4'b0100																																													

4.3.41. External Power Selection Set (FDh)

FCh	External Power Selection Set																											
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX															
Command	0	1	↑	XX	1	1	1	1	1	1	0	1	FDh															
1 st parameter	1	1	↑	XX	0	0	0	0	1	0	1	0	0A															
2 nd parameter	1	1	↑	XX	0	0	pccs_reg[1:0]		0	0	0	0	00															
Description	pccs_reg[1:0]: Select external driving mode.																											
	<table><tr><th>pccs_reg[1]</th><th>pccs_reg[0]</th><th>Driving mode</th></tr><tr><td>0</td><td>0</td><td>Default</td></tr><tr><td>0</td><td>1</td><td>Prohibit</td></tr><tr><td>1</td><td>0</td><td>ILI4002</td></tr><tr><td>1</td><td>1</td><td>Prohibit</td></tr></table>													pccs_reg[1]	pccs_reg[0]	Driving mode	0	0	Default	0	1	Prohibit	1	0	ILI4002	1	1	Prohibit
	pccs_reg[1]	pccs_reg[0]	Driving mode																									
	0	0	Default																									
	0	1	Prohibit																									
	1	0	ILI4002																									
1	1	Prohibit																										
Restriction	To enable this command, EXTC Command Set Enable Register (FFh) must be set first.																											
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes			
	Status	Availability																										
	Normal Mode On, Idle Mode Off, Sleep Out	Yes																										
	Normal Mode On, Idle Mode On, Sleep Out	Yes																										
	Partial Mode On, Idle Mode Off, Sleep Out	Yes																										
	Partial Mode On, Idle Mode On, Sleep Out	Yes																										
Sleep In	Yes																											
Default	<table><tr><th rowspan="2">Status</th><th>Default Value</th></tr><tr><th>pccs_reg[1:0]</th></tr><tr><td>Power On Sequence</td><td>2'b00</td></tr><tr><td>S/W Reset</td><td>No Change</td></tr><tr><td>H/W Reset</td><td>2'b00</td></tr></table>													Status	Default Value	pccs_reg[1:0]	Power On Sequence	2'b00	S/W Reset	No Change	H/W Reset	2'b00						
	Status	Default Value																										
		pccs_reg[1:0]																										
	Power On Sequence	2'b00																										
	S/W Reset	No Change																										
	H/W Reset	2'b00																										

4.3.42. EXTC Command Set enable register (FFh)

FFh	ENEXTC (EXTC command set enable register)																								
	DCX	RDX	WRX	D [23:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	1	1	1	1	1	1	1	1	FFh												
1 st Parameter	1	1	↑	XX	1	1	1	1	1	1	1	1	FFh												
2 nd Parameter	1	1	↑	XX	1	0	0	1	1	0	0	0	98h												
3 rd Parameter	1	1	↑	XX	0	0	0	0	0	1	1	0	06h												
Description	Set the register, 1 st Parameter = FFh, 2 nd Parameter = 98h, 3 rd Parameter = 06h to enable “EXTC command set”. Set the register, 1 st Parameter = FFh, 2 nd Parameter = 98h, 3 rd Parameter = any value except 06h to disable “EXTC command set”.																								
Restriction																									
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power ON Sequence</td><td>1st Parameter = 8'h00 2nd Parameter = 8'h00 3rd Parameter = 8'h00</td></tr><tr><td>S/W Reset</td><td>1st Parameter = 8'h00 2nd Parameter = 8'h00 3rd Parameter = 8'h00</td></tr><tr><td>H/W Reset</td><td>1st Parameter = 8'h00 2nd Parameter = 8'h00 3rd Parameter = 8'h00</td></tr></table>													Status	Default Value	Power ON Sequence	1 st Parameter = 8'h00 2 nd Parameter = 8'h00 3 rd Parameter = 8'h00	S/W Reset	1 st Parameter = 8'h00 2 nd Parameter = 8'h00 3 rd Parameter = 8'h00	H/W Reset	1 st Parameter = 8'h00 2 nd Parameter = 8'h00 3 rd Parameter = 8'h00				
Status	Default Value																								
Power ON Sequence	1 st Parameter = 8'h00 2 nd Parameter = 8'h00 3 rd Parameter = 8'h00																								
S/W Reset	1 st Parameter = 8'h00 2 nd Parameter = 8'h00 3 rd Parameter = 8'h00																								
H/W Reset	1 st Parameter = 8'h00 2 nd Parameter = 8'h00 3 rd Parameter = 8'h00																								

5. Source, Gate and Memory Map

5.1. Memory Map of the 480 (RGB) x 864 Resolution

For example: R36h MV bit (D5) = 0

Source Out		S1	S2	S3	S4	S5	S6	...	S1435	S1436	S1437	S1438	S1439	S1440		
RA														SA		
MY=0	MY=1	R0	G0	B0	R1	G1	B1	...	R478	G478	B478	R479	G479	B479	ML=0	ML=1
0	863							...							0	863
1	862							...							1	862
2	861							...							2	861
3	860							...							3	860
4	859							...							4	859
5	858							...							5	858
6	857							...							6	857
7	856							...							7	856
8	855							...							8	855
9	854							...							9	854
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
856	7							...							856	7
857	6							...							857	6
858	5							...							858	5
859	4							...							859	4
860	3							...							860	3
861	2							...							861	2
862	1							...							862	1
863	0							...							863	0
CA	MX=0	0			1			...	478			479				
	MX=1	479			478			...	1			0				

Figure 159: Memory Map of the 480 (RGB) x 864 Resolution, R36h MV bit D5 = 0

RA = Row Address

CA = Column Address

SA = Scan Address

MX = Colum Address direction parameter

MY = Row Address direction parameter

ML = Scan direction parameter

RGB = Red, Green and Blue pixel position change

5.2. Memory Map of the 480 (RGB) x 854 Resolution

For example: R36h MV bit (D5) = 0

Source Out		S1	S2	S3	S4	S5	S6	...	S1435	S1436	S1437	S1438	S1439	S1440		
RA		RGB Order							RGB Order						SA	
MY=0	MY=1														ML=0	ML=1
0	853	R0	G0	B0	R1	G1	B1	...	R478	G478	B478	R479	G479	B479	0	853
1	852							...							1	852
2	851							...							2	851
3	850							...							3	850
4	849							...							4	849
5	848							...							5	848
6	847							...							6	847
7	846							...							7	846
8	845							...							8	845
9	844							...							9	844
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
846	7							...							846	7
847	6							...							847	6
848	5							...							848	5
849	4							...							849	4
850	3							...							850	3
851	2							...							851	2
852	1							...							852	1
853	0							...							853	0
CA	MX=0	0			1			...	478			479				
	MX=1	479			478			...	1			0				

Figure 160: Memory Map of the 480 (RGB) x 854 Resolution, R36h MV bit D5 = 0

RA = Row Address

CA = Column Address

SA = Scan Address

MX = Column Address direction parameter

MY = Row Address direction parameter

ML = Scan direction parameter

RGB = Red, Green and Blue pixel position change

5.3. Memory Map of the 480 (RGB) x 800 Resolution

For example: R36h MV bit (D5) = 0

Source Out		S1	S2	S3	S4	S5	S6	...	S1435	S1436	S1437	S1438	S1439	S1440		
RA				RGB Order			SA									
MY=0	MY=1						ML=0	ML=1								
0	799	R0	G0	B0	R1	G1	B1	...	R478	G478	B478	R479	G479	B479	0	799
1	798							...							1	798
2	797							...							2	797
3	796							...							3	796
4	795							...							4	795
5	794							...							5	794
6	793							...							6	793
7	792							...							7	792
8	791							...							8	791
9	790							...							9	790
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
792	7							...							792	7
793	6							...							793	6
794	5							...							794	5
795	4							...							795	4
796	3							...							796	3
797	2							...							797	2
798	1							...							798	1
799	0							...							799	0
CA	MX=0	0			1			...	478			479				
	MX=1	479			478			...	1			0				

Figure 161: Memory Map of the 480 (RGB) x 800 resolution, R36h MV bit D5 = 0

RA = Row Address

CA = Column Address

SA = Scan Address

MX = Column Address direction parameter

MY = Row Address direction parameter

ML = Scan direction parameter

RGB = Red, Green and Blue pixel position change

5.4. Memory Map of the 480 (RGB) x 640 Resolution

For example: R36h MV bit (D5) = 0

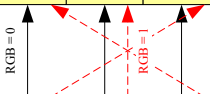
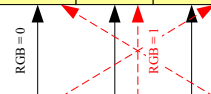
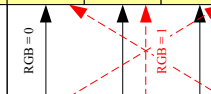
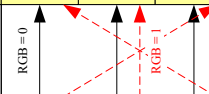
Source Out		S1	S2	S3	S4	S5	S6	...	S1435	S1436	S1437	S1438	S1439	S1440		
RA				RGB Order			SA									
MY=0	MY=1						ML=0	ML=1								
0	639	R0	G0	B0	R1	G1	B1	...	R478	G478	B478	R479	G479	B479	0	639
1	638							...							1	638
2	637							...							2	637
3	636							...							3	636
4	635							...							4	635
5	634							...							5	634
6	633							...							6	633
7	632							...							7	632
8	631							...							8	631
9	630							...							9	630
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
632	7							...							632	7
633	6							...							633	6
634	5							...							634	5
635	4							...							635	4
636	3							...							636	3
637	2							...							637	2
638	1							...							638	1
639	0							...							639	0
CA	MX=0	0			1			...	478			479				
	MX=1	479			478			...	1			0				

Figure 162: Memory Map of the 480 (RGB) x 640 Resolution, R36h MV bit D5 = 0

RA = Row Address

CA = Column Address

SA = Scan Address

MX = Column Address direction parameter

MY = Row Address direction parameter

ML = Scan direction parameter

RGB = Red, Green and Blue pixel position change

6. Source Driver

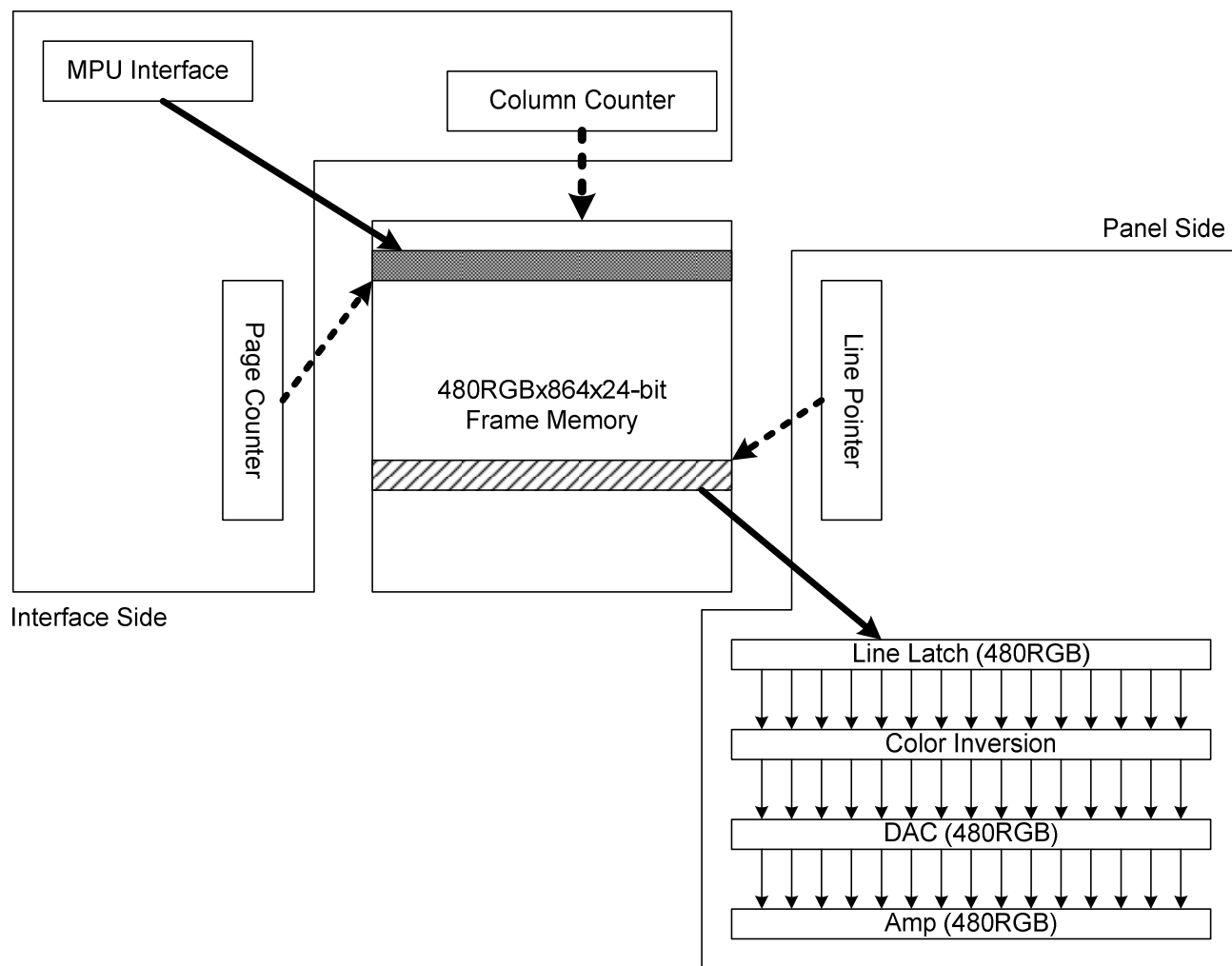
The source driver uses 1440 channels (S1~S1440) are used for driving the source line of the TFT LCD panel. The source driver converts the digital data from the GRAM into the analog voltage and generates the corresponding gray scale voltage output, enabling up to 16.7M colors to be displayed simultaneously. The output circuit of this source driver incorporates with an operational amplifier, so that a positive and a negative voltage can be alternately outputted from each channel.

7. Display Data RAM

7.1. Configuration

The 480 x 864 x 24-bit graphic type static RAM has a 1,244,160-byte memory, allowing the storage of a 480 (RGB)x 864 image with a 24-bit resolution.

Panel Read and Interface Read (or Interface Write) can occur simultaneously with the Frame Memory. This process will not cause any visible effects on the display.

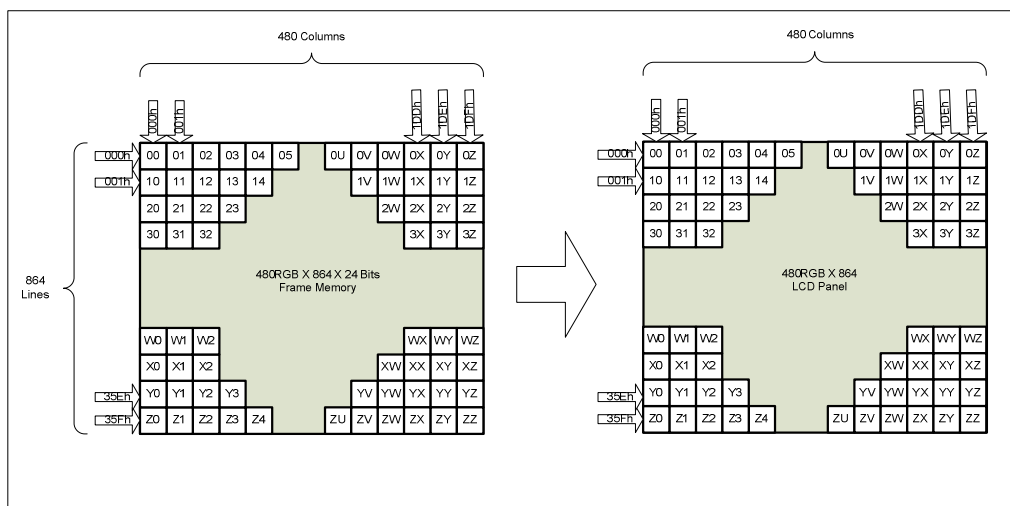


7.2. Memory to Display Address Mapping

7.2.1. Fully Display

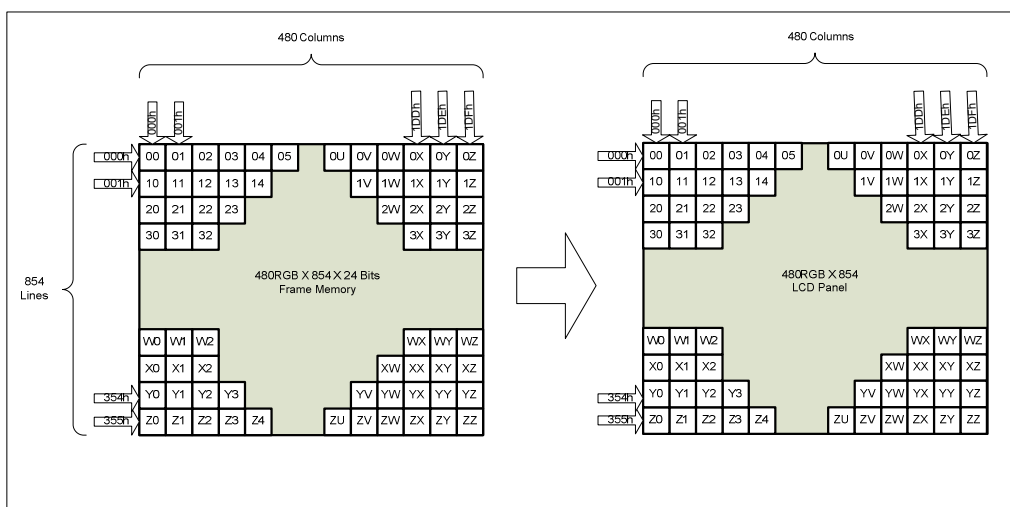
Example: 480 (RGB) x 864 dot display mode

- (1) In this mode, the content of the Frame Memory within an area where the column pointer is 0000h to 01DFh and page pointer is 0000h to 035Fh is displayed.
- (2) NORON (Normal Display Mode On) instruction (R13h)
- (3) SC = 0 x 000h, EC = 0 x 1DFh (R2Ah) and SP = 0 x 000h, EP = 0 x 35Fh (R2Bh), ML = 0



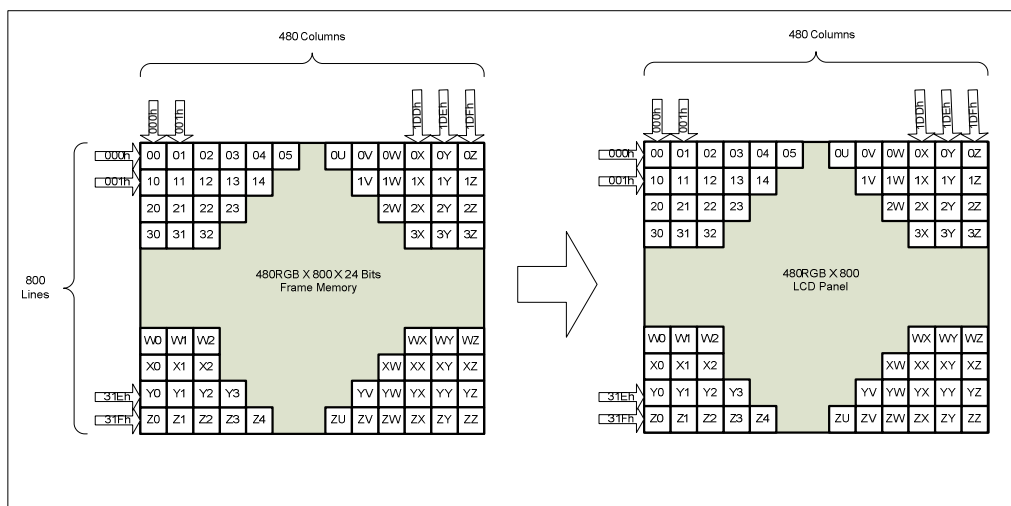
Example: 480 (RGB) x 854 dot display mode

- (1) In this mode, the content of the Frame Memory within an area where the column pointer is 0000h to 01DFh and page pointer is 0000h to 0355h is displayed.
- (2) NORON (Normal Display Mode On) instruction (R13h)
- (3) SC = 0 x 000h, EC = 0 x 1DFh (R2Ah) and SP = 0 x 000h, EP = 0 x 355h (R2Bh), ML = 0



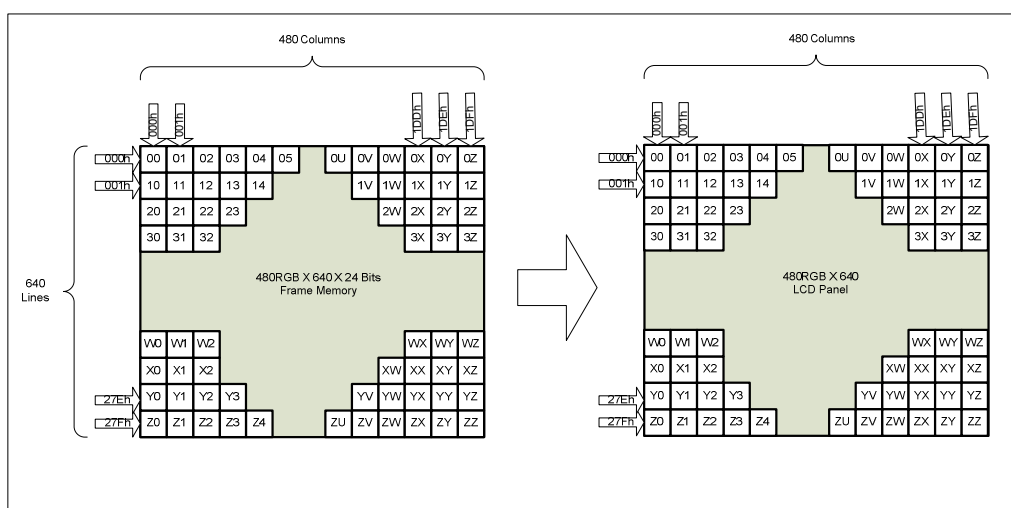
Example: 480 (RGB) x 800 dot display mode

- (1) In this mode, the content of the Frame Memory within an area where the column pointer is 0000h to 01DFh and page pointer is 0000h to 031Fh is displayed.
- (2) NORON (Normal Display Mode On) instruction (R13h)
- (3) SC = 0 x 000h, EC = 0 x 1DFh (R2Ah) and SP = 0 x 000h, EP = 0 x 31Fh (R2Bh), ML = 0



Example: 480 (RGB) x 640 dot display mode

- (1) In this mode, the content of the Frame Memory within an area where the column pointer is 0000h to 01DFh and page pointer is 0000h to 027Fh is displayed.
- (2) NORON (Normal Display Mode On) instruction (R13h)
- (3) SC = 0 x 000h, EC = 0 x 1DFh (R2Ah) and SP = 0 x 000h, EP = 0 x 27Fh (R2Bh), ML = 0



7.2.2. Vertical Scrolling Display

The vertical scrolling mode is determined by the commands “Vertical Scrolling Definition” (33h) and “Vertical Scrolling Start Address” (37h).

The Vertical Scroll Mode function is explained by the examples of $(TFA+VSA+BFA) = 864$ in Figure 163.

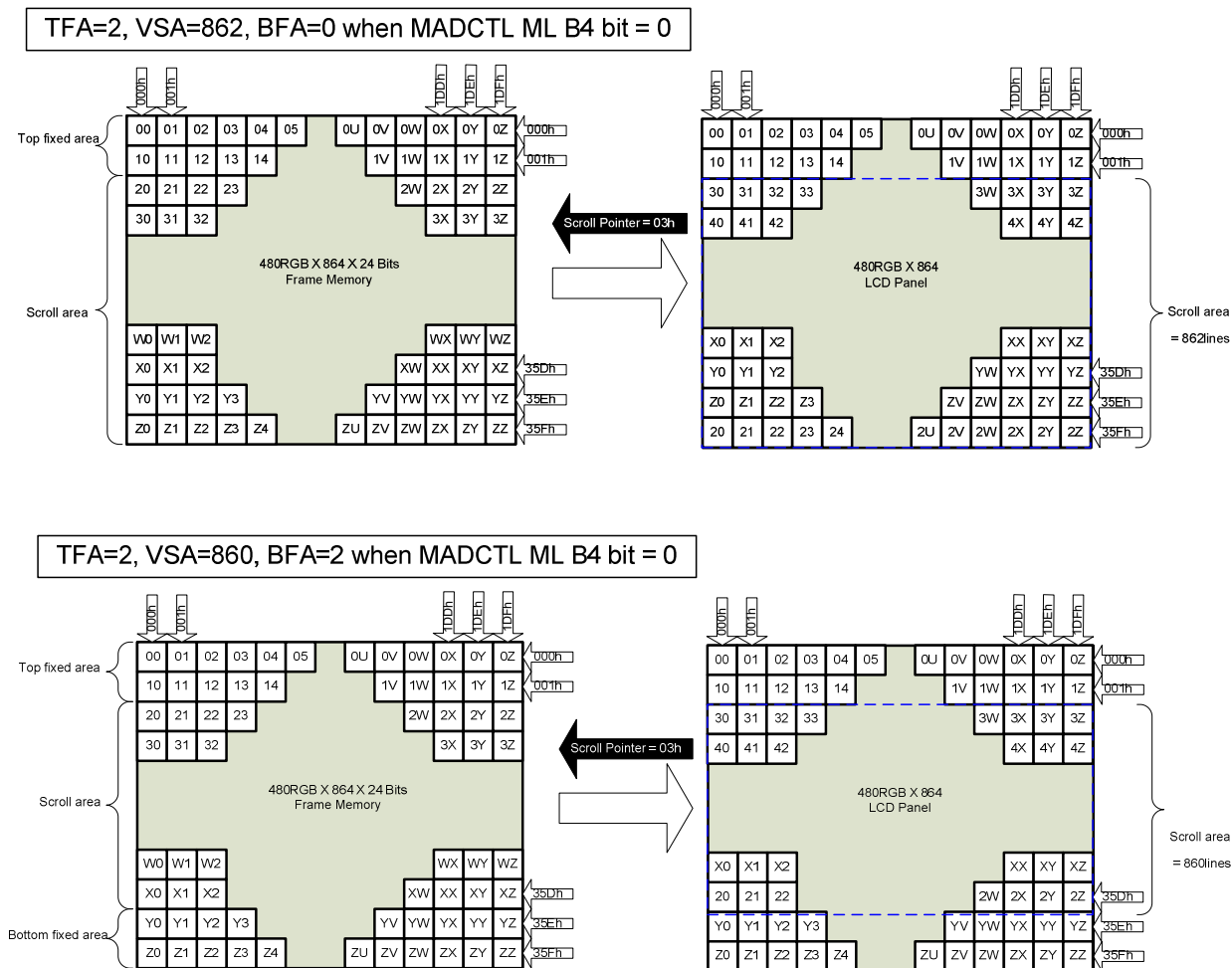


Figure 163: Vertical Scroll Mode Function

Note: When Vertical Scrolling Definition Parameters $(TFA+VSA+BFA) \neq 640$, the Scrolling Mode is undefined.

7.2.3. Vertical Scroll 480(RGB) (H) X 864 (V) Example

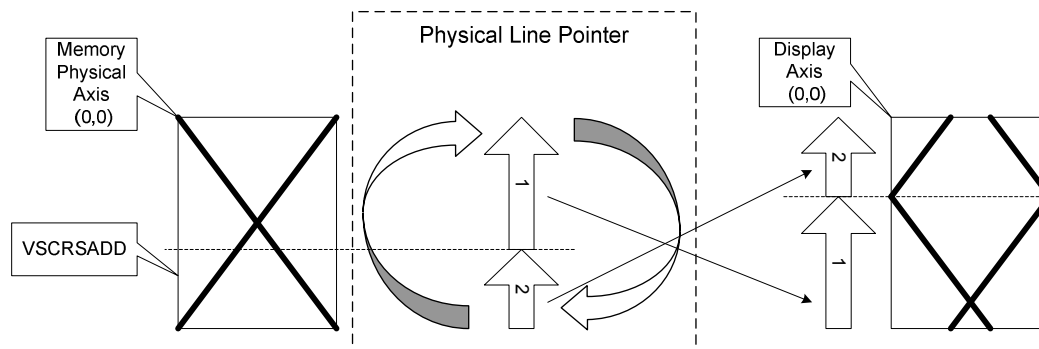
7.2.4. Case1: $TFA+VSA+BFA \neq 864$

This setting is prohibited because it will cause a display output error.

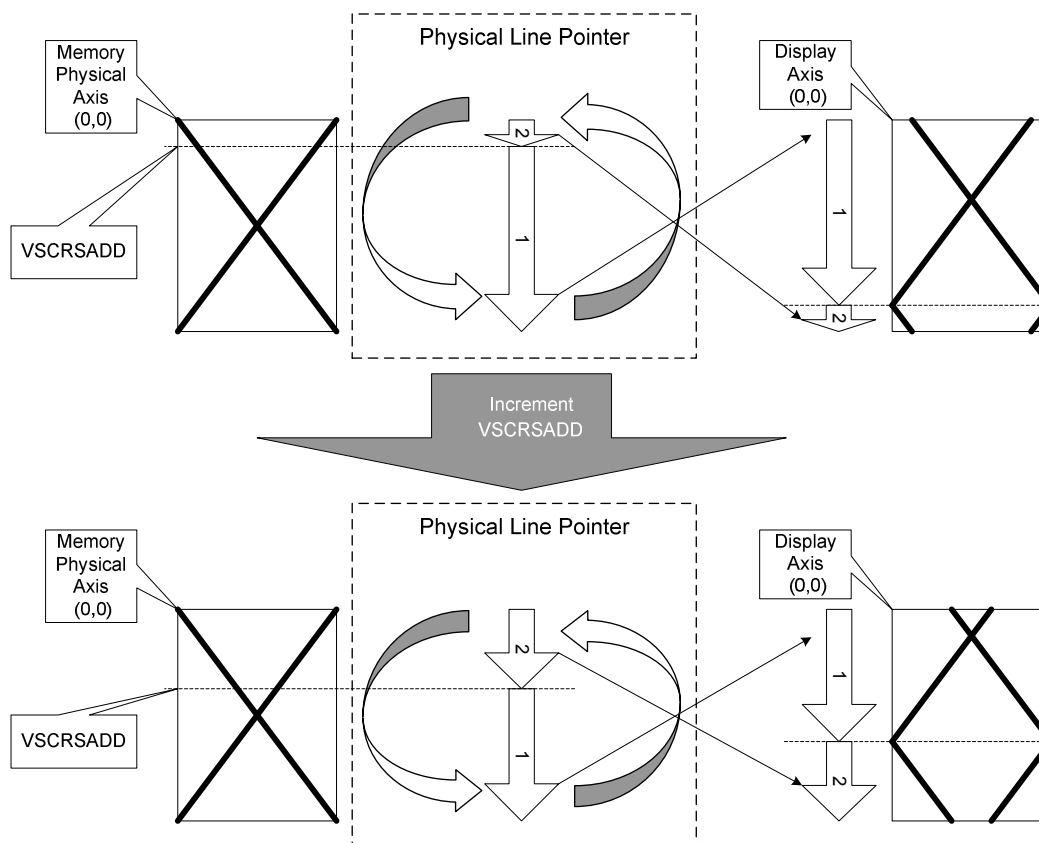
7.2.5. Case2: $TFA+VSA+BFA = 864$ (Rolling Scrolling)

The operations of the Rolling Scrolling are explained by the examples below.

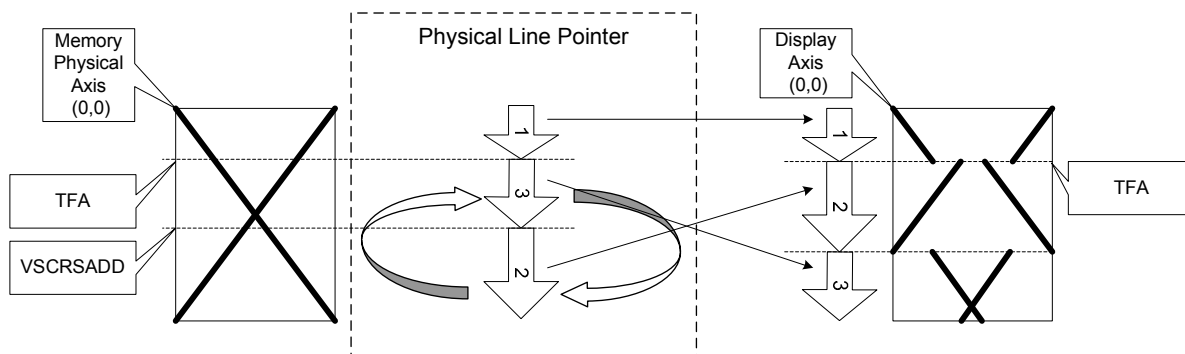
When TFA=0, VSA=864, BFA=0, VSCRSADD=40 and MADCTL ML B4 bit = 1



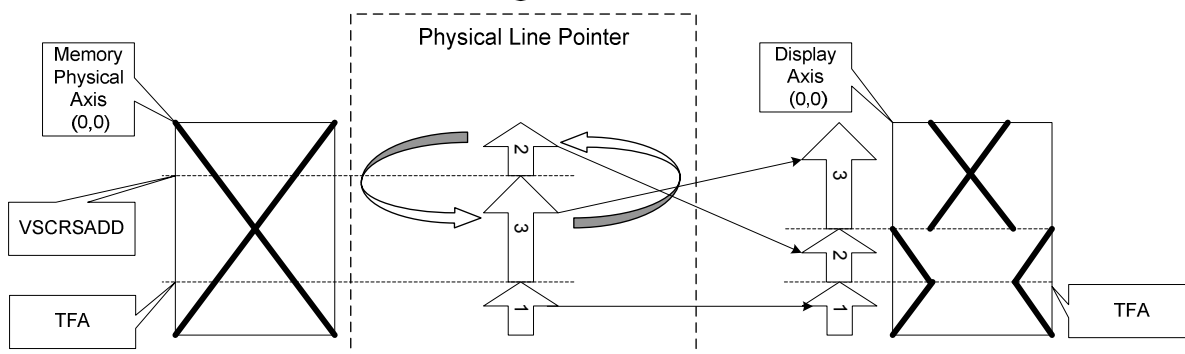
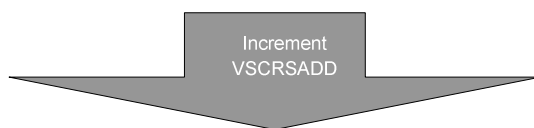
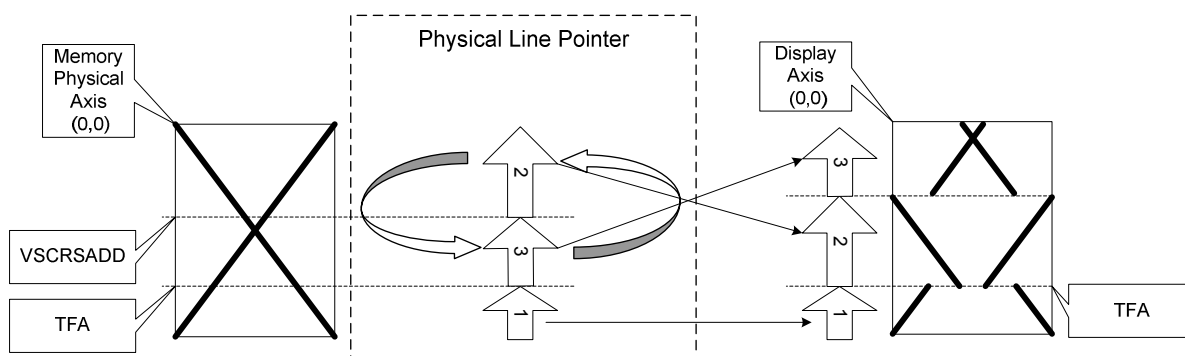
When TFA=0, VSA=864, BFA=0, VSCRSADD=40 and MADCTL ML bit = 0



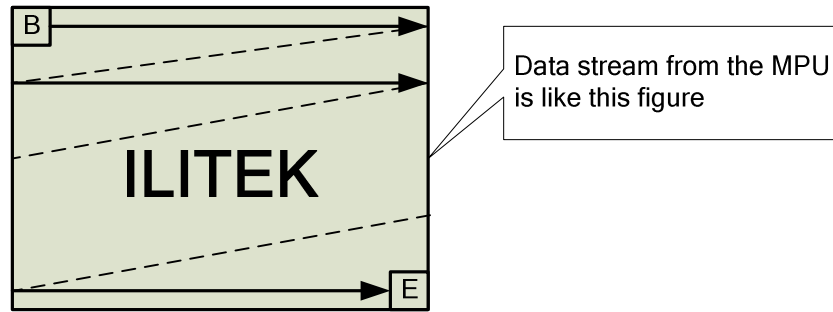
When TFA=30, VSA=834, BFA=0, VSCRSADD=80 and MADCTL ML bit = 0



When TFA=30, VSA=834, BFA=0, VSCRSADD=80 and MADCTL ML bit = 1



7.3. MPU to Memory Write/Read Direction



The data is written in the order illustrated above. Data is always written to the Frame Memory in the same order, regardless of the Memory Write Direction set by MADCTL bits D7, D6 and D5.

The write order for each pixel unit is shown below.

DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R[7]	R[6]	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[7]	G[6]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[7]	B[6]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]

The Counter dictates where the data is to be written in the physical memory and is controlled by “Memory Data Access Control” Command, Bits D5, D6, and D7, as described in Figure 164.

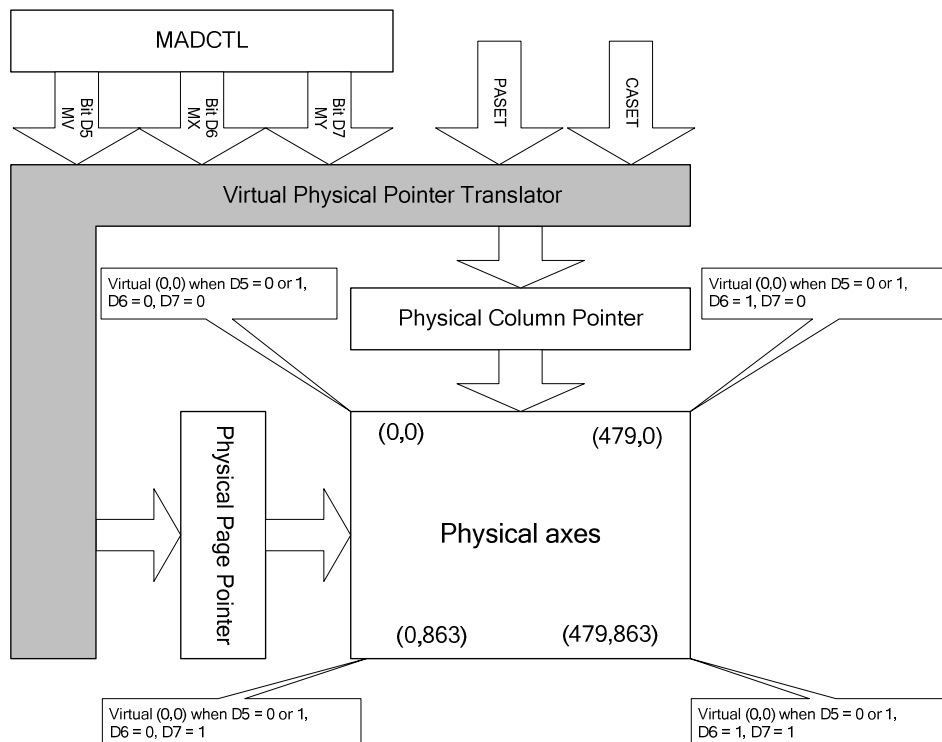


Figure 164: MV, MX, MY setting (480 (RGB) x 864)

D5 (MV)	D6 (MX)	D7 (MY)	CASET	PASET
0	0	0	Direct to Physical Column Pointer	Direct to Physical Page Pointer
0	0	1	Direct to Physical Column Pointer	Direct to (863-Physical Page Pointer)
0	1	0	Direct to (479-Physical Column Pointer)	Direct to Physical Page Pointer
0	1	1	Direct to (479-Physical Column Pointer)	Direct to (863-Physical Page Pointer)
1	0	0	Direct to Physical Page Pointer	Direct to Physical Column Pointer
1	0	1	Direct to (863-Physical Page Pointer)	Direct to Physical Column Pointer
1	1	0	Direct to Physical Page Pointer	Direct to (479-Physical Column Pointer)
1	1	1	Direct to (863-Physical Page Pointer)	Direct to (479-Physical Column Pointer)

Condition	Column Counter	Page counter
When RAMWR/RAMRD command is accepted	Return to "Start column"	Return to "Start Page"
Complete Pixel Read/Write action	Incremented by 1	No change
The Column values are larger than "End Column"	Return to "Start column"	Incremented by 1
The Page counter are larger than "End Page"	Return to "Start column"	Return to "Start Page"

One pixel unit represents 1 column and 1 page counter value on the Frame Memory.

Display Data Direction	MADCTR Parameter			Image in the Memory (MPU)	Image in the Driver (Frame Memory)
	MV	MX	MY		
Normal	0	0	0		
Y-Mirror	0	0	1		
X-Mirror	0	1	0		
X-Mirror Y-Mirror	0	1	1		
X-Y Exchange	1	0	0		
X-Y Exchange Y-Mirror	1	0	1		
X-Y Exchange X-Mirror	1	1	0		
X-Y Exchange X-Mirror Y-Mirror	1	1	1		

8. Tearing Effect Information

The Tearing Effect Line (TE) signal supplies panel synchronization information to the MPU. The TE signal determines the position for refreshing GRAM data for the display panel; the MPU can reference the TE to decide when to send image data in order to avoid abnormal visual effect on the display panel.

The TE signal is enabled or disabled with the Tearing Effect Line ON or OFF commands.

The TE Line output mode is defined by the parameter of the “Tearing Effect Line ON” command.

Tearing Effect information is sent in two different ways:

- Separated Line, which is the Tearing Effect Line (TE).
- Tearing Effect Bus Trigger (TEE), the ILI9806G sends a trigger to inform the MPU.

The TE is used in the MPU parallel interface.

The TE can also be used in the DSI case if the Tearing Effect Bus Trigger (TEE) is not possible to be used.

The Tearing Effect (TEE) Bus Trigger is only used in the DSI.

8.1. Tearing Effect Line

8.1.1. Tearing Effect Line Modes

Mode 1: illustrated in Figure 165, the Tearing Effect output signal consists of V-Sync information only:



Figure 165: Tearing Effect Line Mode 1

tvdh = The LCD display is not updated from the Frame Memory.

tvdl = The LCD display is updated from the Frame Memory (except Invisible Line – see the figure above).

Mode 2: illustrated in Figure 166, the Tearing Effect output signal consists of V-Sync and H-Sync information; there is one V-sync and “N” H-sync pulses per field.

N: If RSO [2:0] = 3'b000, the resolution is 480 (RGB) X 864 and N = 864.

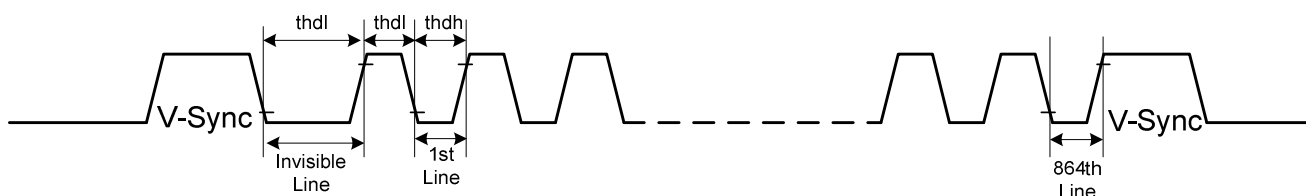
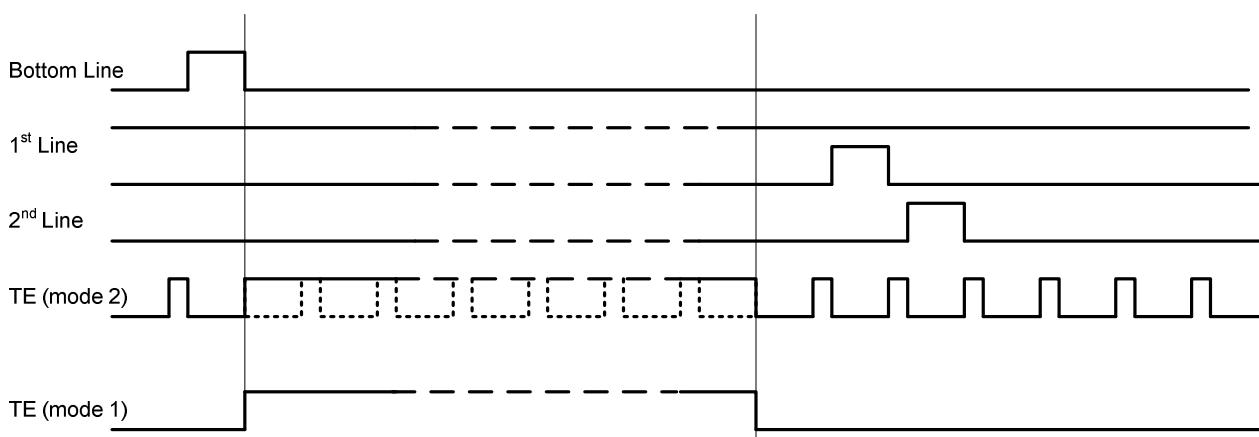


Figure 166: Tearing Effect Line Mode 2

thdh = The LCD display is not updated from the Frame Memory.

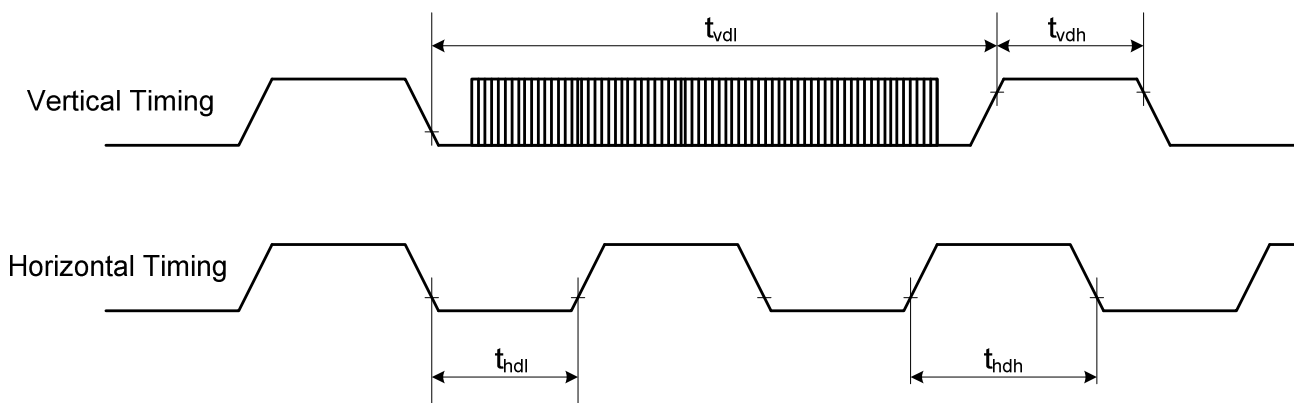
thdl = The LCD display is updated from the Frame Memory (except Invisible Line – see the figure above).



Note: During the Sleep In Mode, the Tearing Effect Output Pin is active Low.

8.1.2. Tearing Effect Line Timing

The tearing effect signal is described below:

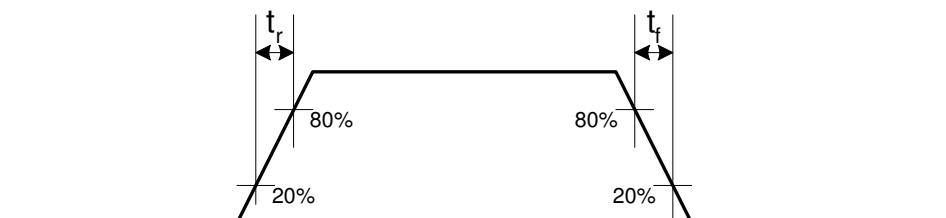


AC characteristics of the Tearing Effect Signal is: (Resolution 480(RGB)x800, Frame Rate = 60.5 Hz)

Table 44: Tearing Effect Line Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{vdl}	Vertical timing low duration	15	-		ms
t_{vdh}	Vertical timing high duration	1000	-		us
t_{hdl}	Horizontal timing low duration	18	-		us
t_{hdh}	Horizontal timing high duration	0.13	500		us

- Notes:
1. The timings in Table 44 are applied when MADCTL D4 = 0 and D4 = 1.
 2. The signal's rising and falling times (t_f , t_r) are stipulated to be equal to or less than 15ns.



The Tearing Effect Output Line is fed back to the MPU and should be used to avoid the Tearing Effect.

8.2. Tearing Effect Bus Trigger

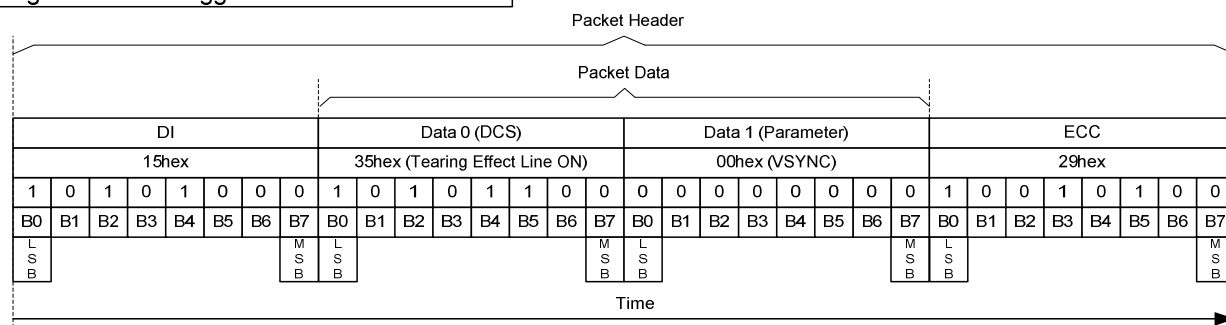
Tearing Effect Bus Trigger information supplies to the MPU a Panel synchronization trigger, and this Tearing Effect Bus Trigger information can be enabled or disabled by “Tearing Effect Line Off (34h)” and “Tearing Effect Line On (35h)” commands when the only mode of the Tearing Effect Signal is VSYNC information.

The ILI9806G sends this trigger information in the Escape Mode after the Bus Turnaround (BTA), and the Tearing Effect Bus Trigger can only be used in the DSI without the TE line.

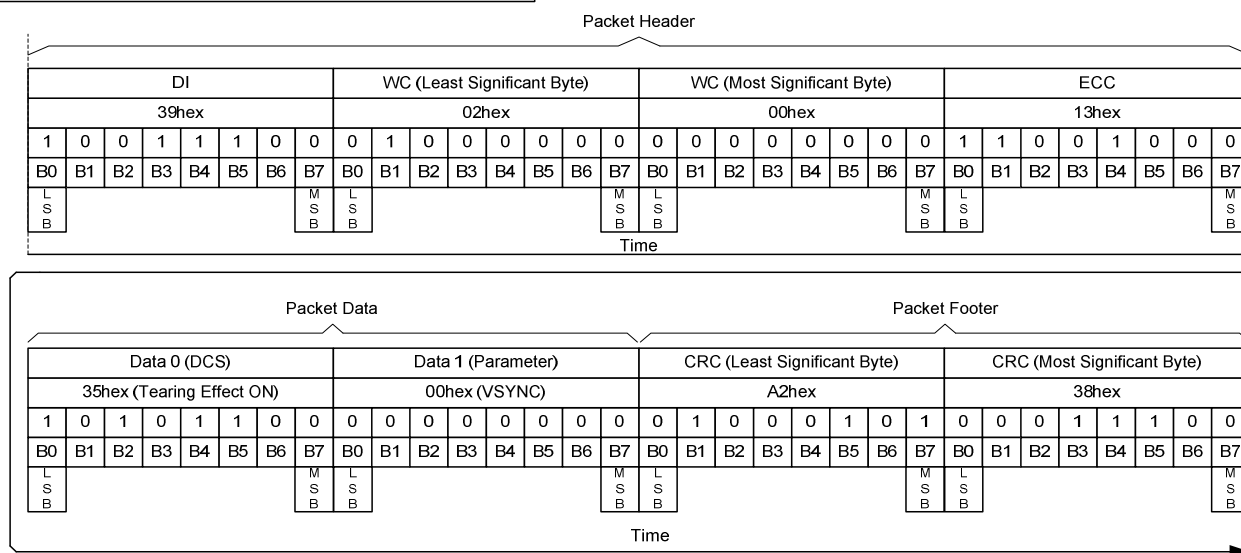
8.2.1. Tearing Effect Bus Trigger Enable

The MPU can enable the Tearing Effect Bus Trigger on the ILI9806G in 2 different ways: when a Short Packet (SPa) or a Long Packet (LPa) is used. These cases are illustrated below.

Tearing Effect Bus Trigger Enable - Short Packet



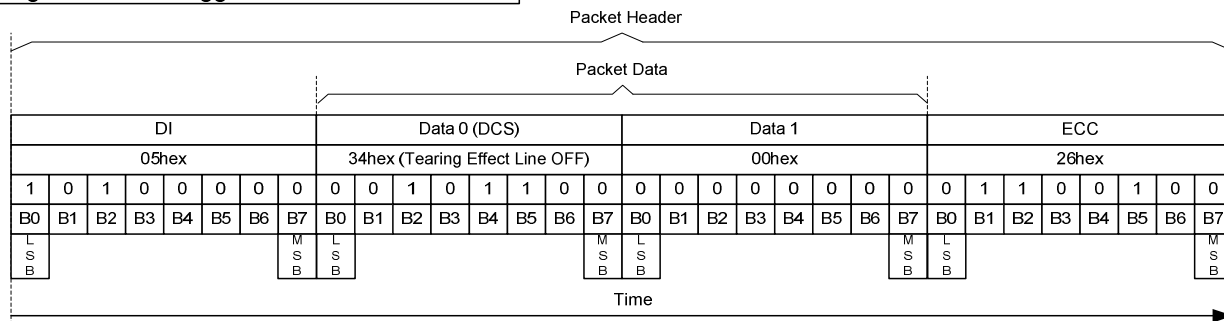
Tearing Effect Bus Trigger Enable - Long Packet



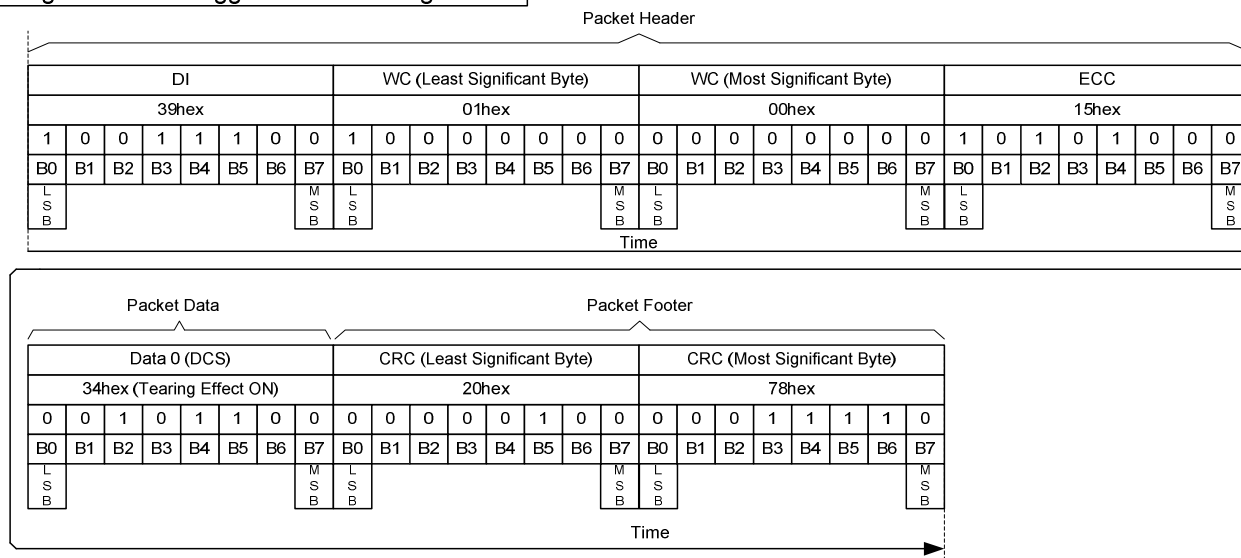
8.2.2. Tearing Effect Bus Trigger Disable

The MPU can enable the Tearing Effect Bus Trigger on the ILI9806G in 2 different ways: when a Short Packet (SPa) or a Long Packet (LPa) is used. These both possibilities are illustrated below.

Tearing Effect Bus Trigger Disable - Short Packet



Tearing Effect Bus Trigger Disable - Long Packet



8.2.3. Tearing Effect Bus Trigger Sequences

Tearing Effect Trigger Enable Sequence – DCS Write (Long Packet) and HSDT						
Line	MPU		Information Direction	Display Module (ILI9806G)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	→	-	-	Start
2	DCSW-L	HSDT	→	-	-	Tearing Effect Trigger Enable
3	EoTP	HSDT	→	-	-	End of Transmission Packet
4	-	LP-11	→	-	-	-
5	-	BTA	↔	BTA	-	Interface Control Change from the MPU to the display module
6	-	-	←	LP-11	-	If No Error => Goto Line 8 If Error is Corrected by ECC => Goto Line 19, If Error => Goto Line 30
7						
8	-	-	←	ACK	-	No Error
9	-	-	←	LP-11	-	-
10	-	BTA	↔	BTA	-	Interface Control Change from the display module to the MPU
11	-	LP-11	→	-	-	-
12	-	BTA	↔	BTA	-	Interface Control Change from the MPU to the display module
13	-	-	←	LP-11	-	-
14	-	-	←	TEE	-	TE (Escape Trigger) on the next V-Synch.
15	-	-	←	LP-11	-	-
16	-	BTA	↔	BTA	-	Interface Control Change from the display module to the MPU
17	-	LP-11	→	-	-	End
18						
19	-	-	←	LPDT	AwER	Error Report (Error is Corrected by ECC)
20	-	-	←	LP-11	-	-
21	-	BTA	↔	BTA	-	Interface Control Change from the display module to the MPU
22	-	LP-11	→	-	-	-
23	-	BTA	↔	BTA	-	Interface Control Change from the MPU to the display module
24	-	-	←	LP-11	-	-
25	-	-	←	TEE	-	TE (Escape Trigger) on the next V-Synch.
26	-	-	←	LP-11	-	-
27	-	BTA	↔	BTA	-	Interface Control Change from the display module to the MPU
28	-	LP-11	→	-	-	End
29						
30	-	-	←	LPDT	AwER	Error Report
31	-	-	←	LP-11	-	-
32	-	BTA	↔	BTA	-	Interface Control Change from the display module to the MPU
33	-	LP-11	→	-	-	If the MPU is not forcing BTA => Goto Line 34, If the MPU is forcing BTA => Goto Line 36
34	-	LP-11	→	-	-	End
35						

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36	-	BTA	↔	BTA	-	Interface Control Change from the MPU to the display module
37	-	-	←	LP-11	-	Dead-Lock (No TE information) See Note 2
38	-	LP-11	→	-	-	The MPU is forced to start to control the interface. The display module detects, Bus Connection Error (BCE)
39	-	BTA	↔	BTA	-	Interface Control Change from the MPU to the display module
40	-	-	←	LP-11	-	-
41	-	-	←	LPDT	AwER	Error Report (Bus Connection Error (BCE) is reported) See Note 2
42	-	-	←	LP-11	-	-
43	-	BTA	↔	BTA	-	Interface Control Change from the display module to the MPU
44	-	LP-11	→	-	-	End

Notes:

1. Lines 1 – 17 are needed for every frame.
2. Bits 5 and 7 of the AwER are applied.

Tearing Effect Trigger Enable Sequence – DCS Write (Long Packet) and LPDT						
Line	MPU		Information Direction	Display Module (ILI9806G)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	➔	-	-	Start
2	DCSW-L	LPDT	➔	-	-	Tearing Effect Trigger Enable
3	-	LP-11	➔	-	-	-
4	-	BTA	↔	BTA	-	Interface Control Change from the MPU to the display module
5	-	-	⬅	LP-11	-	If No Error => Goto Line 7 If Error is Corrected by ECC => Goto Line 18 , If Error => Goto Line 29
6						
7	-	-	⬅	ACK	-	No Error
8	-	-	⬅	LP-11	-	-
9	-	BTA	↔	BTA	-	Interface Control Change from the display module to the MPU
10	-	LP-11	➔	-	-	-
11	-	BTA	↔	BTA	-	Interface Control Change from the MPU to the display module
12	-	-	⬅	LP-11	-	-
13	-	-	⬅	TEE	-	TE (Escape Trigger) on the next V-Synch.
14	-	-	⬅	LP-11	-	-
15	-	BTA	↔	BTA	-	Interface Control Change from the display module to the MPU
16	-	LP-11	➔	-	-	End
17						
18	-	-	⬅	LPDT	AwER	Error Report (Error is Corrected by ECC)
19	-	-	⬅	LP-11	-	-
20	-	BTA	↔	BTA	-	Interface Control Change from the display module to the MPU
21	-	LP-11	➔	-	-	-
22	-	BTA	↔	BTA	-	Interface Control Change from the MPU to the display module
23	-	-	⬅	LP-11	-	-
24	-	-	⬅	TEE	-	TE (Escape Trigger) on the next V-Synch.
25	-	-	⬅	LP-11	-	-
26	-	BTA	↔	BTA	-	Interface Control Change from the display module to the MPU
27	-	LP-11	➔	-	-	End
28						
29	-	-	⬅	LPDT	AwER	Error Report
30	-	-	⬅	LP-11	-	-
31	-	BTA	↔	BTA	-	Interface Control Change from the display module to the MPU
32	-	LP-11	➔	-	-	If the MPU is not forcing BTA => Goto Line 33 , If the MPU is forcing BTA => Goto Line 35
33	-	LP-11	➔	-	-	End
34						
35	-	BTA	↔	BTA	-	Interface Control Change from the MPU to the display module

36	-	-	←	LP-11	-	Dead-Lock (No TE information) See Note 2
37	-	LP-11	→	-	-	The MPU is forced to start to control the interface. The display module detects Bus Connection Error (BCE)
38	-	BTA	↔	BTA	-	Interface Control Change from the MPU to the display module
39	-	-	←	LP-11	-	-
40	-	-	←	LPDT	AwER	Error Report (Bus Connection Error (BCE) is reported) See Note 2
41	-	-	←	LP-11	-	-
42	-	BTA	↔	BTA	-	Interface Control Change from the display module to the MPU
43	-	LP-11	→	-	-	End

Notes:

1. Lines 1 – 16 are needed for every frame.
2. Bits 5 and 7 of the AwER are applied.

Tearing Effect Trigger Enable Sequence – DCS Write, 1 Parameter (Short Packet) and HSDT						
Line	MPU		Information Direction	Display Module (ILI9806G)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	➔	-	-	Start
2	DCSW1-S	HSDT	➔	-	-	Tearing Effect Trigger Enable
3	EoTP	HSDT	➔	-	-	End of Transmission Packet
4	-	LP-11	➔	-	-	-
5	-	BTA	↔	BTA	-	Interface Control Change from the MPU to the display module
6	-	-	⬅	LP-11	-	If No Error => Goto Line 8 If Error is Corrected by ECC => Goto Line 19 , If Error => Goto Line 30
7						
8	-	-	⬅	ACK	-	No Error
9	-	-	⬅	LP-11	-	-
10	-	BTA	↔	BTA	-	Interface Control Change from the display module to the MPU
11	-	LP-11	➔	-	-	-
12	-	BTA	↔	BTA	-	Interface Control Change from the MPU to the display module
13	-	-	⬅	LP-11	-	-
14	-	-	⬅	TEE	-	TE (Escape Trigger) on the next V-Synch.
15	-	-	⬅	LP-11	-	-
16	-	BTA	↔	BTA	-	Interface Control Change from the display module to the MPU
17	-	LP-11	➔	-	-	End
18						
19	-	-	⬅	LPDT	AwER	Error Report (Error is Corrected by ECC)
20	-	-	⬅	LP-11	-	-
21	-	BTA	↔	BTA	-	Interface Control Change from the display module to the MPU
22	-	LP-11	➔	-	-	-
23	-	BTA	↔	BTA	-	Interface Control Change from the MPU to the display module
24	-	-	⬅	LP-11	-	-
25	-	-	⬅	TEE	-	TE (Escape Trigger) on the next V-Synch.
26	-	-	⬅	LP-11	-	-
27	-	BTA	↔	BTA	-	Interface Control Change from the display module to the MPU
28	-	LP-11	➔	-	-	End
29						
30	-	-	⬅	LPDT	AwER	Error Report
31	-	-	⬅	LP-11	-	-
32	-	BTA	↔	BTA	-	Interface Control Change from the display module to the MPU
33	-	LP-11	➔	-	-	If the MPU is not forcing BTA => Goto Line 34 , If the MPU is forcing BTA => Goto Line 36
34	-	LP-11	➔	-	-	End
35						
36	-	BTA	↔	BTA	-	Interface Control Change from the

						MPU to the display module
37	-	-	←	LP-11	-	Dead-Lock (No TE information) See Note 2
38	-	LP-11	→	-	-	The MPU is forced to start to control the interface. The display module detects Bus Connection Error (BCE)
39	-	BTA	↔	BTA	-	Interface Control Change from the MPU to the display module
40	-	-	←	LP-11	-	-
41	-	-	←	LPDT	AwER	Error Report (Bus Connection Error (BCE) is reported) See Note 2
42	-	-	←	LP-11	-	-
43	-	BTA	↔	BTA	-	Interface Control Change from the display module to the MPU
44	-	LP-11	→	-	-	End

Notes:

1. Lines 1 – 17 are needed for every frame.
2. Bits 5 and 7 of the AwER are applied.

Tearing Effect Trigger Enable Sequence – DCS Write, 1 Parameter (Short Packet) and LPDT						
Line	MPU		Information Direction	Display Module (ILI9806G)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	➔	-	-	Start
2	DCSW1-S	LPDT	➔	-	-	Tearing Effect Trigger Enable
3	-	LP-11	➔	-	-	-
4	-	BTA	↔	BTA	-	Interface Control Change from the MPU to the display module
5	-	-	⬅	LP-11	-	If No Error => Goto Line 7 If Error is Corrected by ECC => Goto Line 18 , If Error => Goto Line 29
6						
7	-	-	⬅	ACK	-	No Error
8	-	-	⬅	LP-11	-	-
9	-	BTA	↔	BTA	-	Interface Control Change from the display module to the MPU
10	-	LP-11	➔	-	-	-
11	-	BTA	↔	BTA	-	Interface Control Change from the MPU to the display module
12	-	-	⬅	LP-11	-	-
13	-	-	⬅	TEE	-	TE (Escape Trigger) on the next V-Synch.
14	-	-	⬅	LP-11	-	-
15	-	BTA	↔	BTA	-	Interface Control Change from the display module to the MPU
16	-	LP-11	➔	-	-	End
17						
18	-	-	⬅	LPDT	AwER	Error Report (Error is Corrected by ECC)
19	-	-	⬅	LP-11	-	-
20	-	BTA	↔	BTA	-	Interface Control Change from the display module to the MPU
21	-	LP-11	➔	-	-	-
22	-	BTA	↔	BTA	-	Interface Control Change from the MPU to the display module
23	-	-	⬅	LP-11	-	-
24	-	-	⬅	TEE	-	TE (Escape Trigger) on the next V-Synch.
25	-	-	⬅	LP-11	-	-
26	-	BTA	↔	BTA	-	Interface Control Change from the display module to the MPU
27	-	LP-11	➔	-	-	End
28						
29	-	-	⬅	LPDT	AwER	Error Report
30	-	-	⬅	LP-11	-	-
31	-	BTA	↔	BTA	-	Interface Control Change from the display module to the MPU
32	-	LP-11	➔	-	-	If the MPU is not forcing BTA => Goto Line 33 , If the MPU is forcing BTA => Goto Line 35
33	-	LP-11	➔	-	-	End
34						
35	-	BTA	↔	BTA	-	Interface Control Change from the MPU to the display module

36	-	-	←	LP-11	-	Dead-Lock (No TE information) See Note 2
37	-	LP-11	→	-	-	The MPU is forced to start to control the interface. The display module detects Bus Connection Error (BCE)
38	-	BTA	↔	BTA	-	Interface Control Change from the MPU to the display module
39	-	-	←	LP-11	-	-
40	-	-	←	LPDT	AwER	Error Report (Bus Connection Error (BCE) is reported) See Note 2
41	-	-	←	LP-11	-	-
42	-	BTA	↔	BTA	-	Interface Control Change from the display module to the MPU
43	-	LP-11	→	-	-	End

Notes:

1. Lines 1 – 16 are needed for every frame.
2. Bits 5 and 7 of the AwER are applied.

Tearing Effect Bus Trigger Disable Sequence – DCS Write, No Parameter (Short Packet) and LPDT						
Line	MPU		Information Direction	Display Module (ILI9806G)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	→	-	-	Start
2	DCS Write (SPa)	LPDT	→	-	-	Tearing Effect Bus Trigger Disable
3	-	LP-11	→	-	-	End

Tearing Effect Bus Trigger Disable Sequence – DCS Write, No Parameter (Short Packet) and HSDT						
Line	MPU		Information Direction	Display Module (ILI9806G)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	→	-	-	Start
2	DCS Write (SPa)	HSDT	→	-	-	Tearing Effect Bus Trigger Disable
3	-	LP-11	→	-	-	End

9. Content Adaptive Brightness Control (CABC) Function

The CABC, a dynamic backlight control function, drastically reduces power consumption of the luminance source. The ILI9806G will refer the gray scale content of the display image to output in the PWM waveform then to the LED driver for backlight brightness control. The content of gray scale can be increased while simultaneously lowering the brightness of the backlight to achieve the same perceived brightness. The adjusted gray level scale and the power consumption reduction depend on the content of the image.

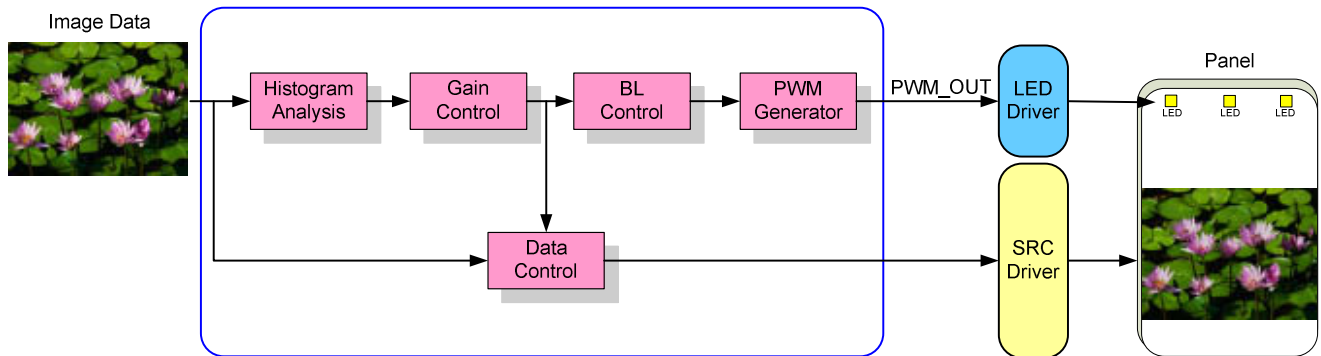


Figure 167: CABC Block Diagram

The ILI9806G can calculate the backlight brightness level and send a PWM_OUT pulse to the LED driver via PWM_OUT pin for backlight brightness control purposes. The PWM frequency can be adjusted by PWM_DIV parameters, and the calculating equation is shown below:

$$f_{\text{pwm_out}} = \frac{18 \text{ MHz}}{(\text{PWM_DIV}[7:0] + 1) \times 255}$$

Figure 168 is the basic timing diagram which is applied by the ILI9806G in order to control a LED driver.

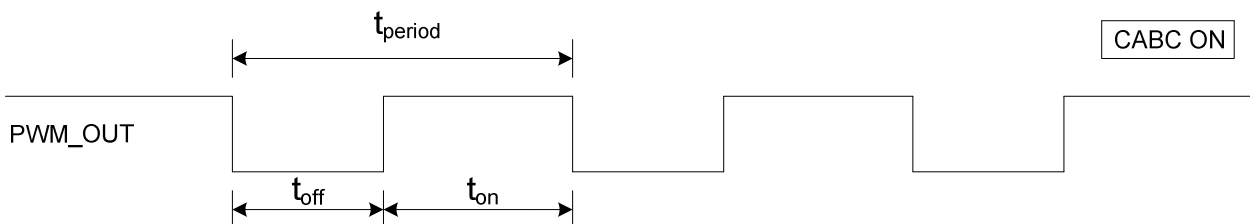


Figure 168: PWM OUT on/off period

10. Color Enhancement Function

The ILI9806G supports color enhancement. The Color Enhancement Function enhances saturation by calculating image data of the display on the liquid crystal panel. The saturation enhancement coefficients of red, yellow, green, cyan, blue, magenta, are set independently. The function enhances color and makes pixel colors more vivid.

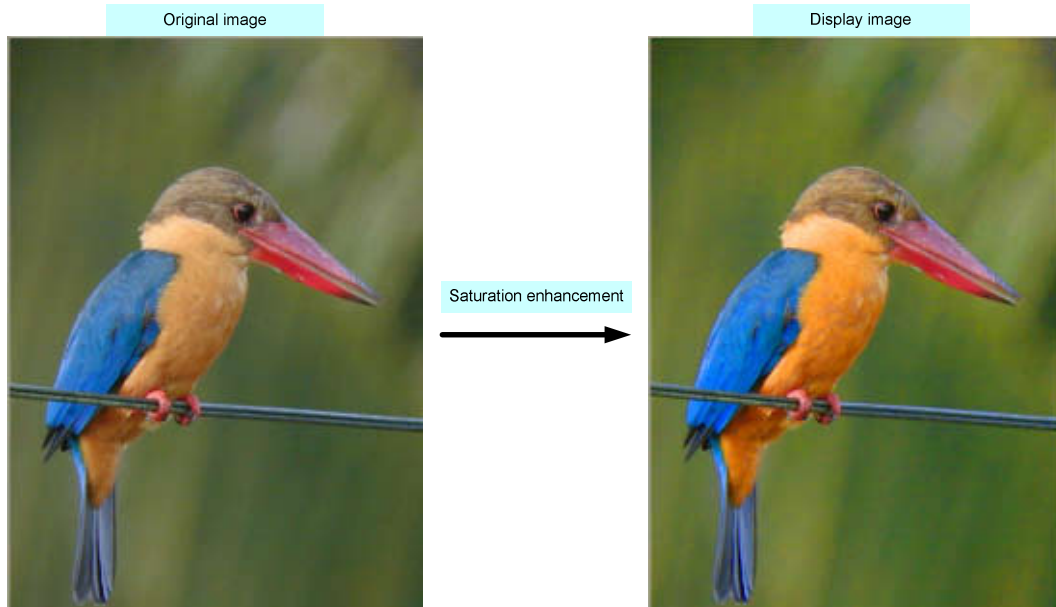


Figure 169: Saturation Enhancement Image

The display image with color enhanced is generated when the saturation enhancement coefficients of the input image are 1.0 or more. See the saturation diagram Figure 169, where the colors of the input image are enhanced. Both green and magenta colors keep the original gray value without enhanced.

11. Sleep Out Command and Self-Diagnostic Functions

11.1. Register Loading Detection

The Sleep Out command (See “Sleep Out (11h)”) is a trigger for an internal function of the display module, which indicates if the display module loading function of factory default values from the EEPROM (or similar devices) to registers of the display controller works properly.

Factory values of the EEPROM and register values of the display controller are compared by the display controller (1st step: compare register and EEPROM values, 2nd step: loads EEPROM values to the register). If those values (EEPROM and register values) are the same, a bit is inverted (= increased by 1), which is defined in the command Read Display Self-Diagnostic Result (0Fh) (= RDDSDR). The used bit of this command is D7. If both values are not the same, this bit (D7) is not inverted (not increased by 1), and the used TE-line is set to low (registers, set by the “Tearing Effect Line On (35h)” command, keep their current values) and can only be reactivated by the “Tearing Effect Line On (35h)” command.

The flow chart for this internal function is:

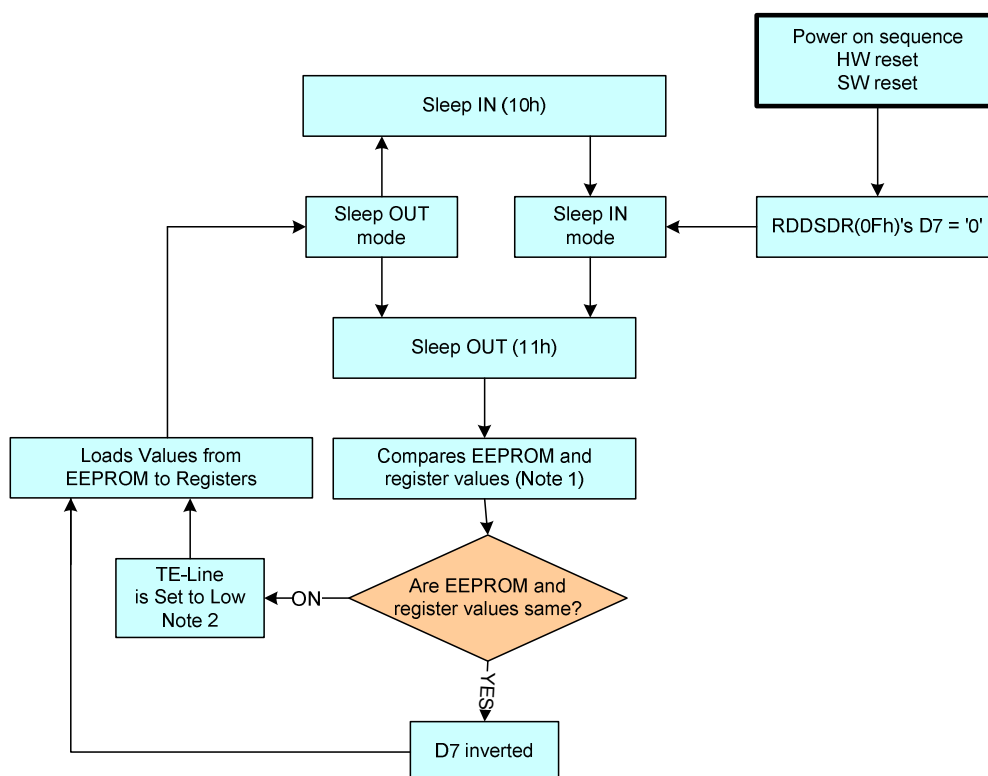


Figure 170: Register Loading Detection

Notes:

1. If the EEPROM and register values are not compared and loaded, they can be changed by commands 00h to AFh and DAh to DDh.
2. This information is only used when the TE line is used.

11.2. Functionality Detection

The Sleep Out command (See “Sleep Out (11h)”) is a trigger for an internal function of the display module. It indicates if the display module is still running and meets functionality requirements.

The internal function (the display controller) is compared when the display module meets functionality requirements (e.g. booster voltage levels, timings, etc.). If functionality requirements are met, a bit is inverted (increased by 1), defined in the command “Read Display Self-Diagnostic Result (0Fh)” (RDDSDR). The used bit of this command is D6. If functionality requirements are not the same, this bit (D6) is not inverted (not increased by 1), and the used TE-line is set to low (registers keep their current values) and can only be reactivated by “Tearing Effect Line On (35h)” command.

The flow chart for this internal function is:

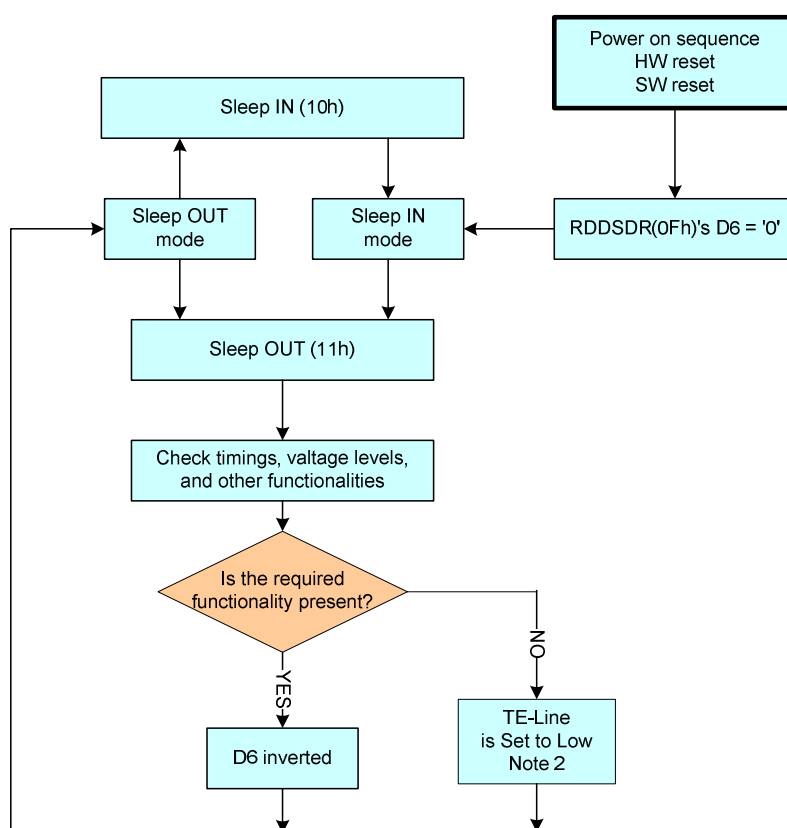


Figure 171: Functionality Detection

Notes:

1. When changing from the Sleep In mode to the Sleep Out mode, 120msec are needed after the Sleep Out command before it is able to check if functionality requirements are met and the value of RDDSDR's D6 is valid. Otherwise, there will be 5msec delay for the D6's value to be valid when the Sleep Out command is sent in the Sleep Out mode.
2. This function can only be used when the TE-line is used.

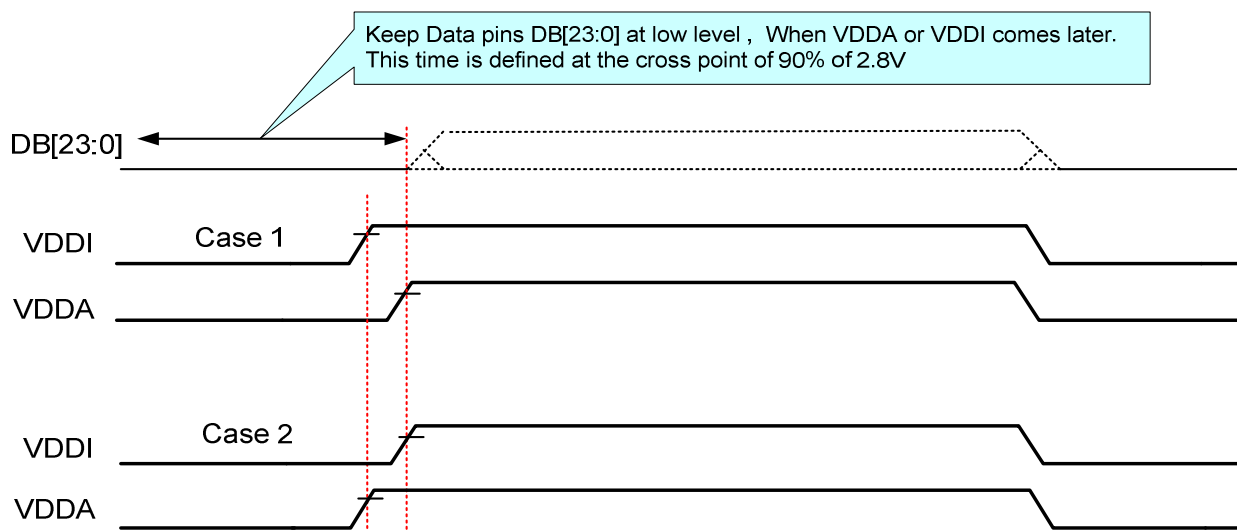
12. Power ON/OFF Sequence

VDDI and VDDA can be applied or powered down in any order. During the Power Off sequence, if the LCD is in the Sleep Out mode, VDDA and VDDI must be powered down with minimum 120msec. If the LCD is in the Sleep In mode, VDDA and VDDI can be powered down with minimum 0msec after the RESX is released.

CSX can be applied at any timing or can be permanently grounded. RESX has high priority over CSX.

Notes:

1. There will be no damage to the ILI9806G if the power sequences are not met.
2. There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.
3. There will be no abnormal visible effects on the display between the end of Power On Sequence and before receiving the Sleep Out command, and also between receiving the Sleep In command and the Power Off Sequence.
4. If the RESX line is not steadily held by the host during the Power On Sequence as defined in Sections 12.1 and 12.2, then it will be necessary to apply the Hardware Reset (RESX) after the completion of the Host Power On Sequence to ensure correct operations. Otherwise, all the functions are not guaranteed.
5. Keep data pins DB[23:0] at low level, when VDDA or VDDI comes later.



12.1. Case 1 – RESX Line is Held High or Unstable by Host at Power ON

If the RESX line is held high or unstable by the host during Power On, then the Hardware Reset must be applied after both VDDA and VDDI have been applied. Otherwise, the correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.

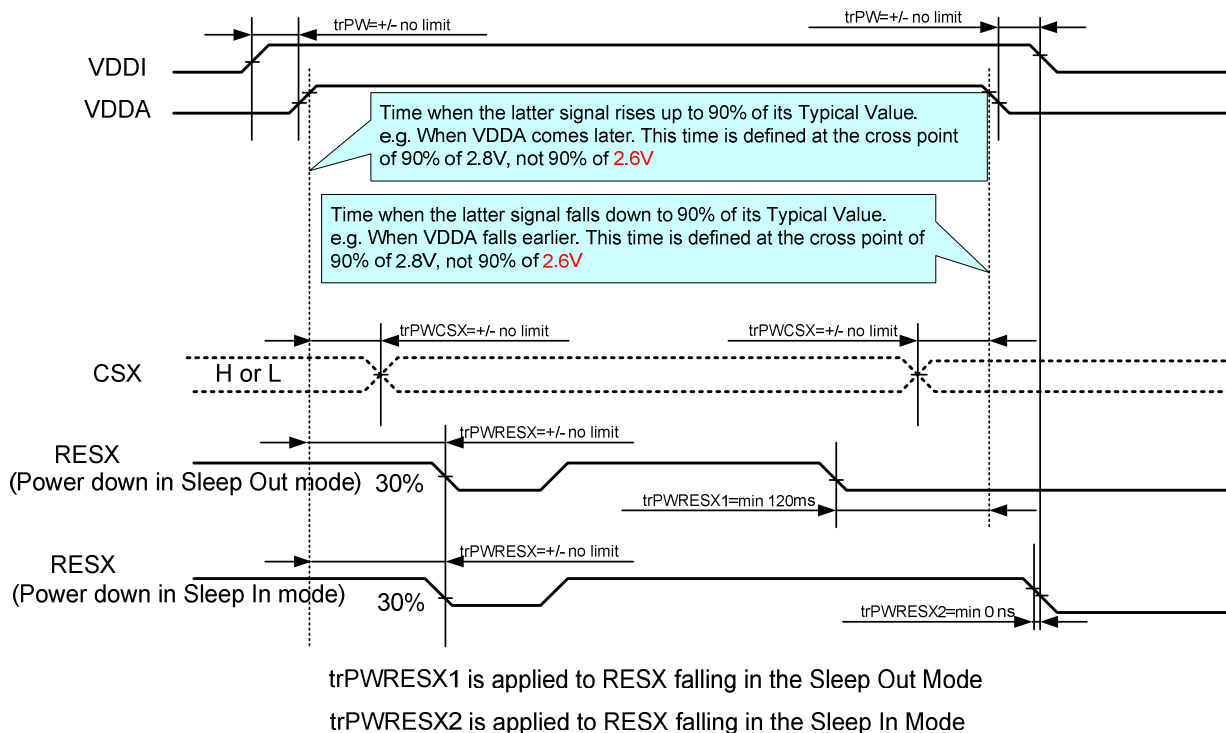


Figure 172: Case 1 – RESX Line is Held High or Unstable by Host at Power ON

Note: Unless otherwise specified, timings herein show the cross point at 50% of the signal power level.

12.2. Case 2 – RESX Line is Held Low by Host at Power ON

If the RESX line is held Low (and stable) by the host during Power On, then the RESX must be held low for a minimum of 10μsec after both VDDA and VDDI have been applied.

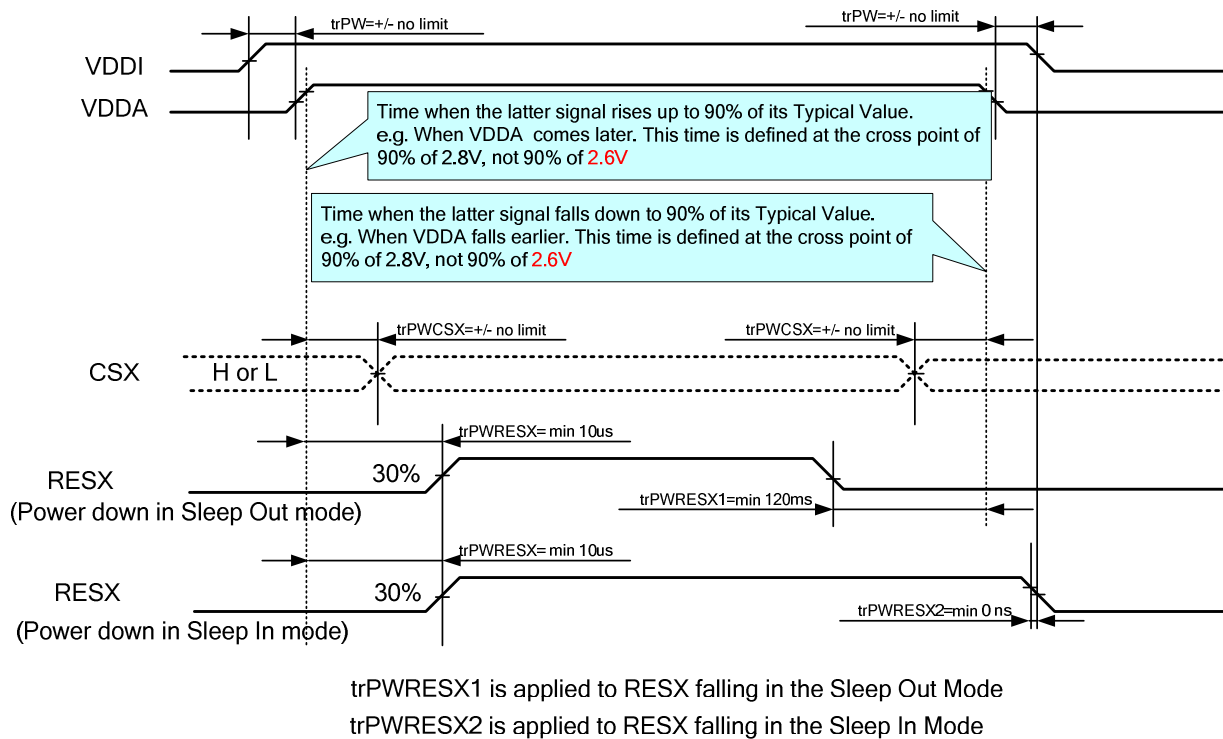


Figure 173: Case 2 – RESX Line is Held Low by Host at Power ON

Note: Unless otherwise specified, timings herein show the cross point at 50% of the signal power level.

12.3. Abnormal Power Off

The Abnormal Power Off means a situation when a battery is removed without the controlled power off sequence. There will not be any damages on the display module, or the display module will not cause any damages on the host or lines of the interface. At an uncontrolled power off event, the ILI9806G will not cause any abnormal visible effects within 1 second on the display, and will force the display to become blank until the Power On Sequence powers it up.

13. Power Level Definition

13.1. Power Levels

6 level modes are defined in order from Maximum to Minimum Power Consumption:

1. Normal Mode On (full display), Idle Mode Off, Sleep Out.

In this mode, the display is able to show a maximum of 16.7M colors.

2. Partial Mode On, Idle Mode Off, Sleep Out.

In this mode, part of the display is used with a maximum of 16.7M colors.

3. Normal Mode On (full display), Idle Mode On, Sleep Out.

In this mode, the full display area is used but with 8 colors.

4. Partial Mode On, Idle Mode On, Sleep Out.

In this mode, part of the display is used but with 8 colors.

5. Sleep In Mode.

In this mode, the DC/DC converter, internal oscillator, and panel driver circuit are stopped. Only the MPU interface and memory work with VDDI power supply. Contents of the memory are safe and cannot be changed.

6. Power Off Mode.

In this mode, both VDDA and VDDI are removed.

Transition between modes 1-5 is controllable by MPU commands. Only when both Power supplies are removed can Mode 6 be entered.

13.3. LCM Voltage Generation

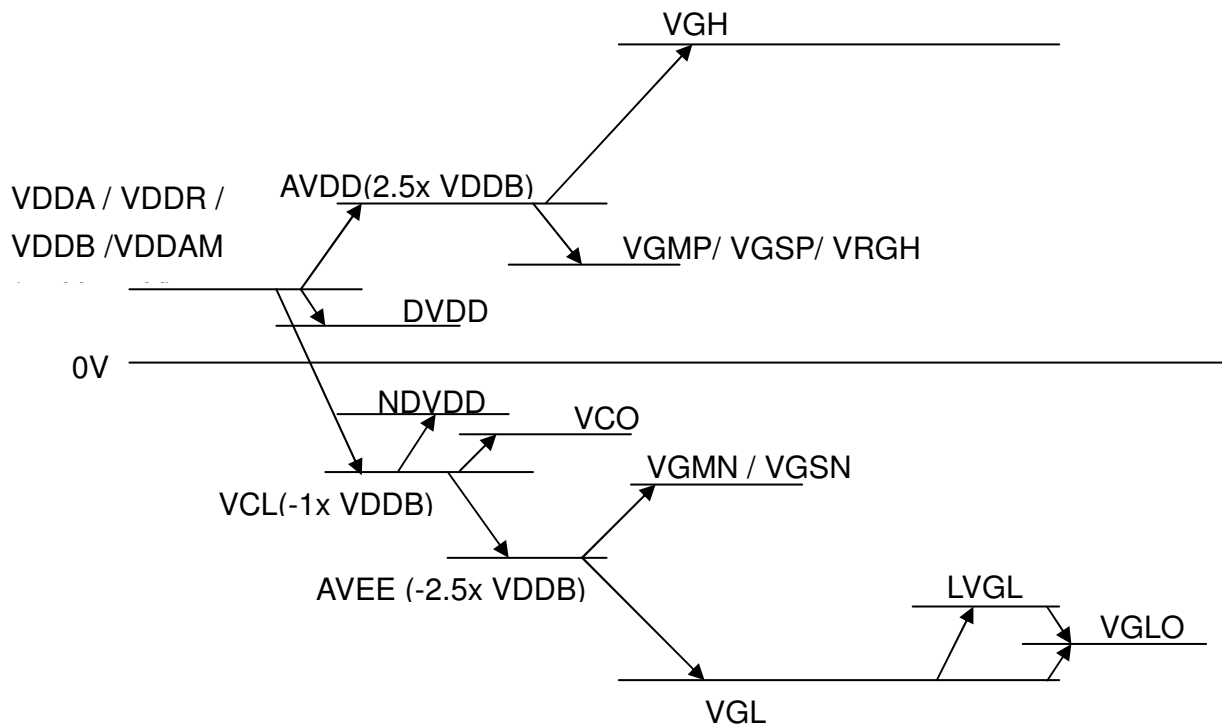


Figure 175: Power Stage Diagram

Power	VGL : BL[1:0]	
$AVDD = 2.5 \times VDDDB$	00	$AVEE - AVDD$
$AVEE = -2.5 \times VDDDB$	01	$2AVEE - VDDDB$
$VCL = -1 \times VDDDB$	10	$AVEE - AVDD + VCL$
$VGH = 2AVDD - AVEE$	11	$AVEE - VDDDB + VCL$

Note: The AVDD, AVEE, VGMP, VGMN, VCOM, VGH, VGL and VCL output voltage levels are lower than their theoretical levels (ideal voltage levels) due to the current consumption at respective outputs.

13.4. Gamma Curves

13.4.1. Gamma Curve 1 (GC0), applies the function $y = x^{2.2}$

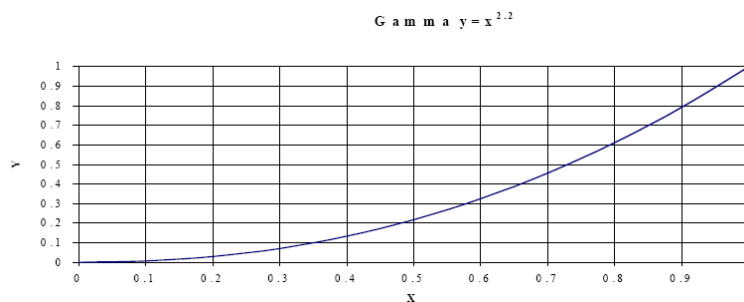


Figure 176: Gamma Curve 1 (GC0)

13.4.2. Gamma Curve 2 (GC1), applies the function $y = x^{1.8}$

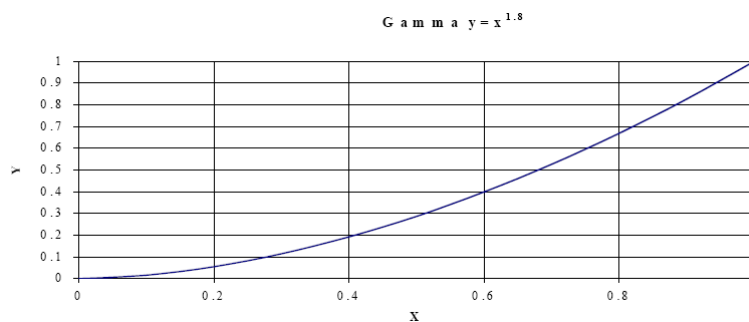


Figure 177: Gamma Curve 2 (GC1)

13.4.3. Gamma Curve 3 (GC2), applies the function $y = x^{2.5}$

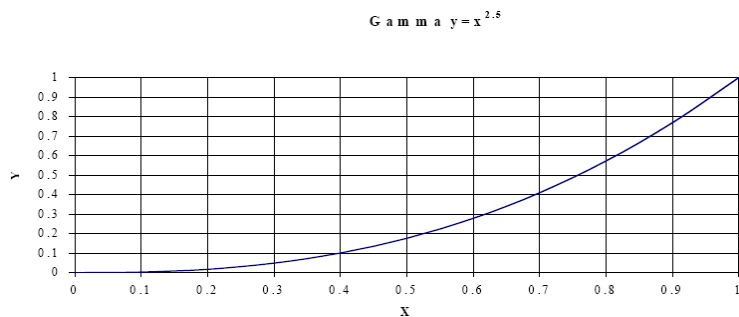


Figure 178: Gamma Curve 3 (GC2)

13.4.4. Gamma Curve 4 (GC3), applies the function $y = x^{1.0}$

$$\text{Gamma } y = x^1$$

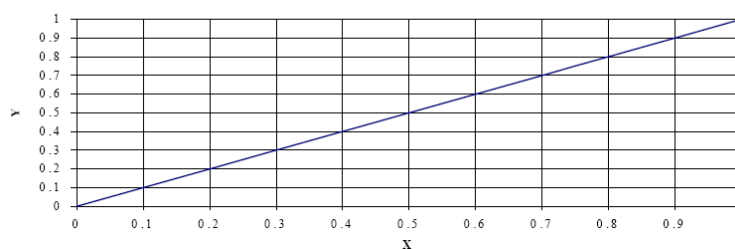


Figure 179: Gamma Curve 4 (GC3)

14. Reset

14.1. Registers

The initialized values of registers are listed in the Table 45.

Table 45: Initial Values of Registers

Register	After Powered ON	After Hardware Reset	After Software Reset
Frame Memory	Random	Random	Random
Sleep	In	In	In
Display Mode	Normal	Normal	Normal
Display Status	Display Off	Display Off	Display Off
Idle Mode	Off	Off	Off
All Pixels Off	Off	Off	Off
All Pixels On	Off	Off	Off
Column Start Address (2Ah)	0000 h	0000 h	0000 h
Column End Address (2Ah)	01DF h	01DF h	01DF h
Page Start Address (2Bh)	0000 h	0000 h	0000 h
Page End Address (2Bh)	480(RGB)x864=035Fh	480(RGB)x864=035Fh	480(RGB)x864=035 h
Gamma Setting (26h)	GC0	GC0	GC0
Partial Area Start (30h)	0000 h	0000 h	0000 h
Partial Area End (30h)	480(RGB)x864=035Fh	480(RGB)x864=035Fh	480(RGB)x864=035Fh
MADCTL (36h)	00 h	00 h	00h
RDNUMED (05h)	00 h	00 h	00h
RDDPM (0Ah)	08 h	08 h	08 h
RDDMADCTL (0Bh)	00 h	00 h	no change
RDDCOLMOD (0Ch)	07 h	07 h	07 h
RDDIM (0Dh)	00 h	00 h	00 h
RDDSM (0Eh)	00 h	00 h	00 h
RDDSDR (0Fh)	00 h	00 h	00 h
Color Pixel Format (3Ah)	24 Bit/Pixel	24 Bit/Pixel	24 Bit/Pixel
TE Output Line (35h)	Off	Off	Off
TE Line Mode (35h)	Mode 1 (Note 3)	Mode 1 (Note 3)	Mode 1 (Note 3)
RDDISBV (52h)	00 h	00 h	00 h
RDCTRLD (54h)	00 h	00 h	00 h
RDCABC (56h)	00 h	00 h	00 h
RDCABCMB (5Fh)	00 h	00 h	00 h
RDFCS (AAh)	00 h	00 h	00 h
RDCCS (AFh)	00 h	00 h	00 h
MRPS (Data Type 37h)	01 h	01 h	01 h

Notes:

1. There will be no abnormal visible effects on the display when S/W or H/W Resets are applied.
2. After the Powered-On Reset finishes within 10μs after both VDDA & VDDI are applied.
3. Mode 1 means Tearing Effect Output Line consists of V-Blanking Information only.

14.2. Driver IC Input and Output pins

14.2.1. Output Pins, I/O Pins

Table 46: Output and I/O Pins

Pin/Line	After Power ON	After Hardware Reset	After Software Reset
DB [23:0]	Hi-Z (Inactive)	Hi-Z (Inactive)	Hi-Z (Inactive)
SDA (Output direction), SDO	Hi-Z (Inactive)	Hi-Z (Inactive)	Hi-Z (Inactive)
HS_D0P	Hi-Z (Inactive)	Hi-Z (Inactive)	Hi-Z (Inactive)
HS_D0N	Hi-Z (Inactive)	Hi-Z (Inactive)	Hi-Z (Inactive)
LEDPWM	Low	Low	Low
TE_L / TE_R	Low	Low	Low

Note: There will be no output from DB [23:0], SDA, SDO, LEDPWM, TE_L / TE_R, HS_D0P, and HS_D0N, during the Power ON/OFF sequence, hardware reset and software reset.

14.2.2. Reset Timing

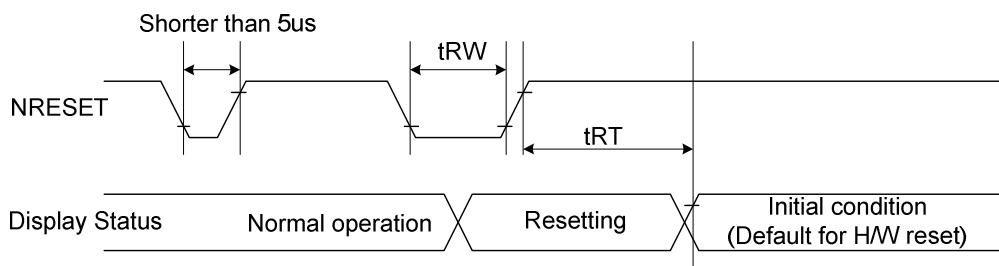


Figure 180: Reset Timing

Table 47: Reset Timing

Signal	Symbol	Parameter	Min	Max	Unit
RESX	tRW	Reset pulse duration	10		us
	tRT	Reset cancel		5 (note 1,5) 120 (note 1,6,7)	ms

Notes:

1. The reset cancel also includes the required time for loading ID bytes, VCOM setting and other settings from the EEPROM to registers. After a rising edge of RESX, this loading is done within 5 ms after the H/W reset cancel (tRT).
2. A spike due to an electrostatic discharge on the RESX line does not cause irregular system reset, according to the Table 48.

Table 48: Reset Description

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Resetting period, the display will be blanked (When Reset starts in the Sleep Out mode, the display will enter the blanking sequence in at least 120 ms. The display remains blank in the Sleep In mode.), and then return to the default condition for the Hardware Reset.
4. Spike Rejection can also be applied during a valid reset pulse as shown below:

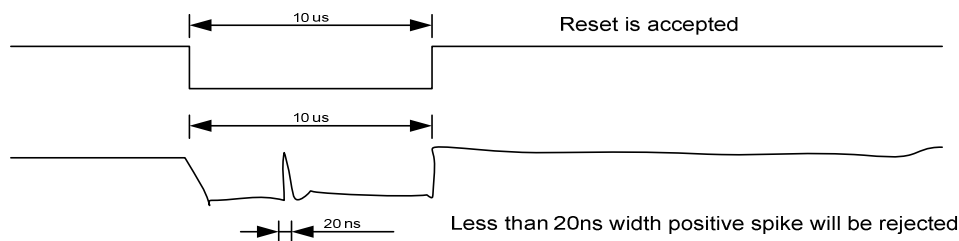


Figure 181: Positive Noise Pulse during Reset Low

5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5msec after releasing the RESX before sending commands. Moreover, the Sleep Out command cannot be sent in 120msec.

15. NV Memory Programming

15.1. NV Memory Programming Flow

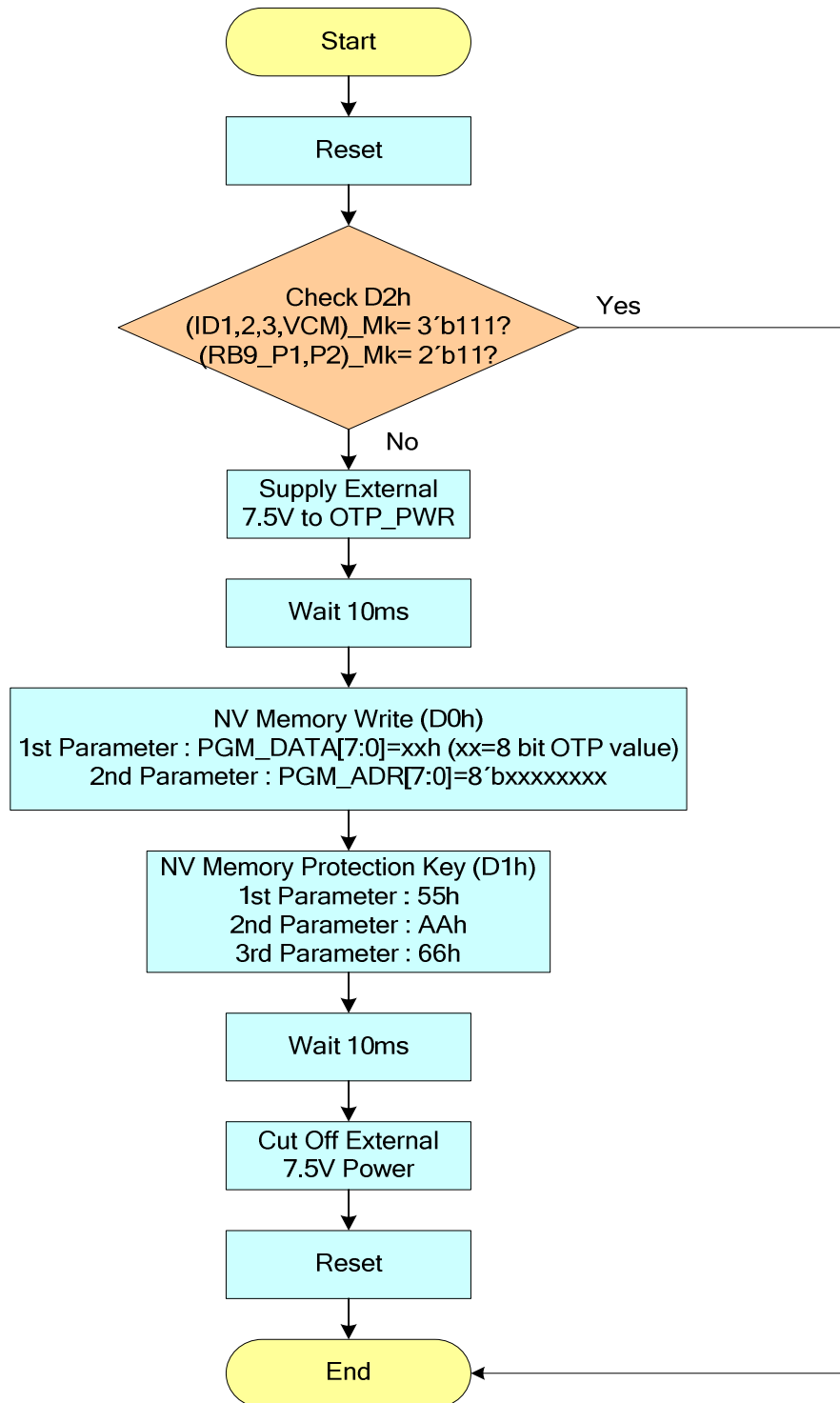
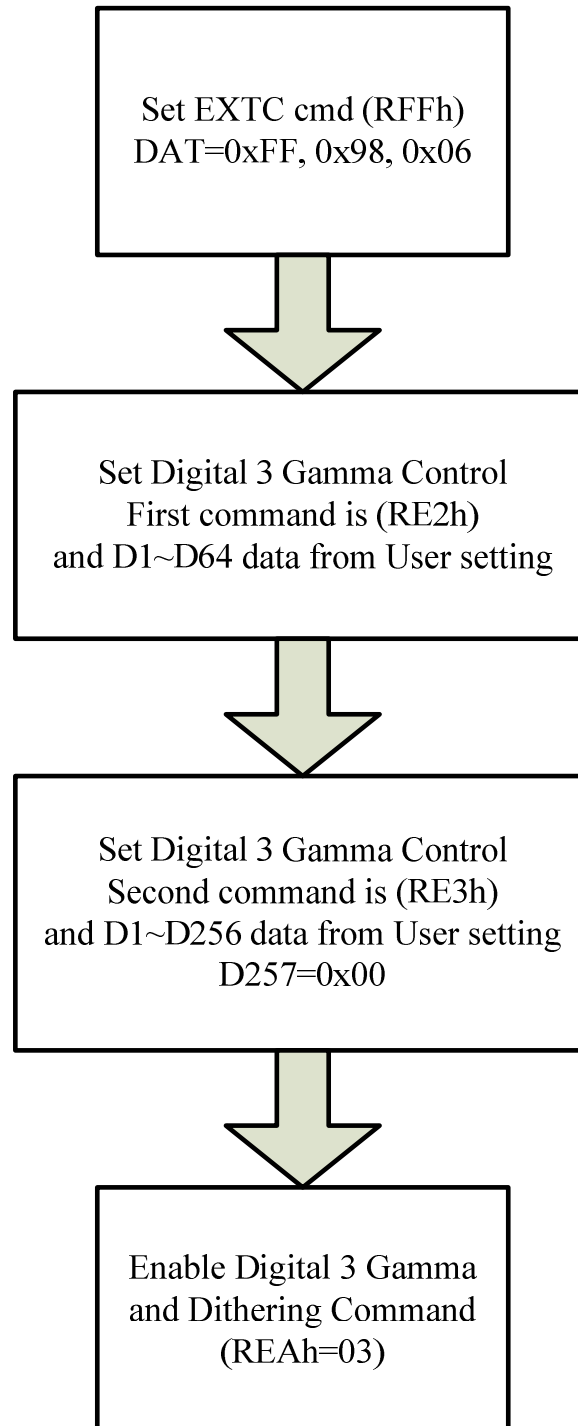


Figure 182: NV Memory Programming Flow

Note 1 : In SPI operation mode, set register FBh "ext_spi_read_en"=1 to enable the read function of extend command.

16. 3 Gamma Setting Flow

16.1. 3 Gamma Setting Flow



Negative Gamma Control (E1h)

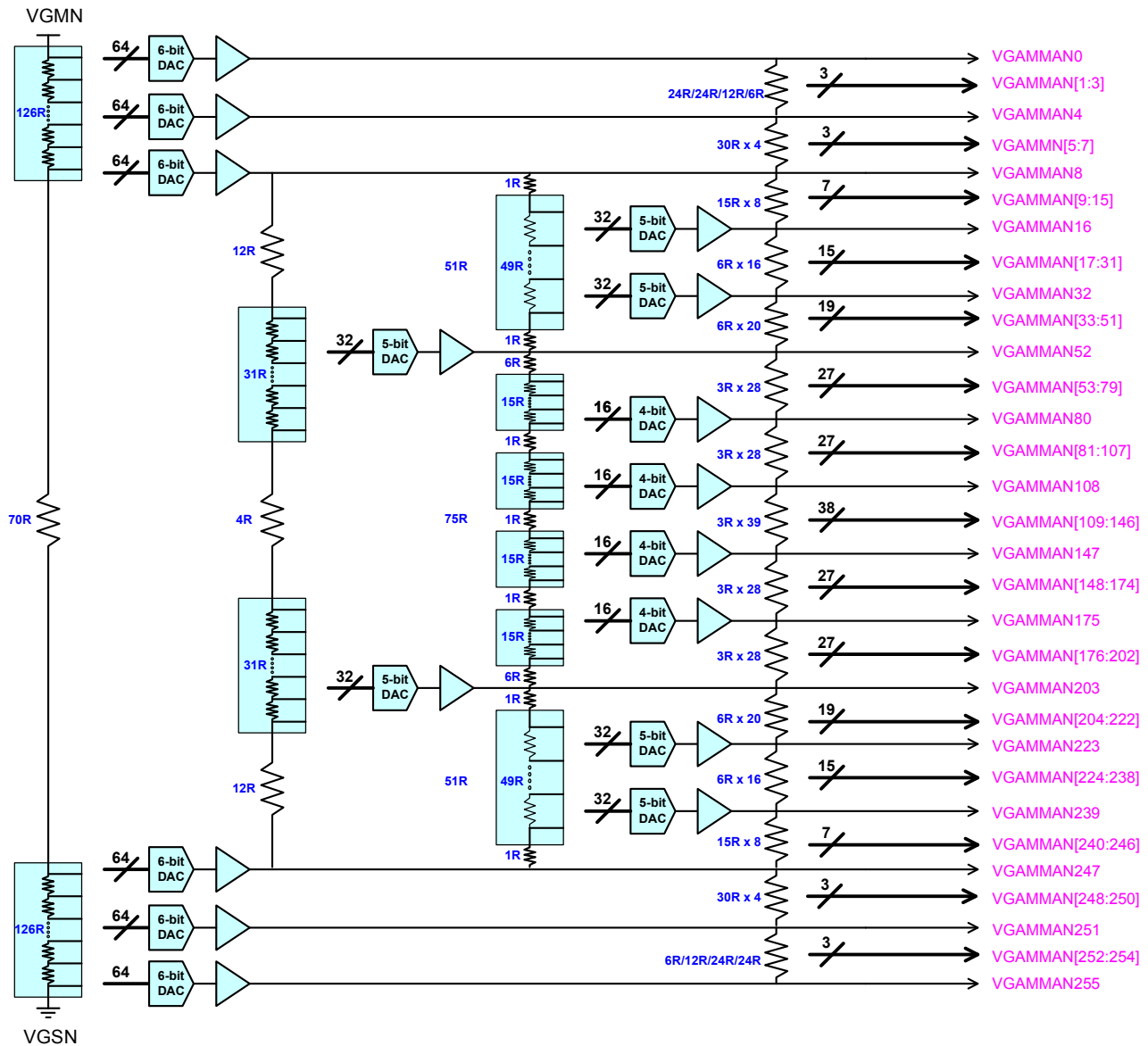


Figure 184: Negative Gamma Control (E1h)

Positive polarity	Resister stream	Gamma 256 grayscale voltage calculation formula
VGAMMAP0	24R	$VGSP + \Delta VDHP (322R - 2R \cdot VP0[5:0]) / 322R$, $\Delta VDHP = (VGMP - VGSP)$
VGAMMAP1	24R	$VGAMMAP4 + (VGAMMP0 - VGAMMAP4) \cdot (6R + 12R + 24R) / (42R + RCGPH + 24R)$
VGAMMAP2	12R	$VGAMMAP4 + (VGAMMP0 - VGAMMAP4) \cdot (6R + 12R) / (42R + RCGPH + 24R)$
VGAMMAP3	6R	$VGAMMAP4 + (VGAMMP0 - VGAMMAP4) \cdot (6R) / (42R + RCGPH + 24R)$
VGAMMAP4	30R	$VGSP + \Delta VDHP (322R - 2R \cdot VP4[5:0]) / 322R$, $\Delta VDHP = (VGMP - VGSP)$
VGAMMAP5	30R	$VGAMMAP8 + (VGAMMAP4 - VGAMMAP8) \cdot (90R / 120R)$
VGAMMAP6	30R	$VGAMMAP8 + (VGAMMAP4 - VGAMMAP8) \cdot (60R / 120R)$
VGAMMAP7	30R	$VGAMMAP8 + (VGAMMAP4 - VGAMMAP8) \cdot (30R / 120R)$

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VGAMMAP8	15R	$VGSP + \Delta VDHP(322R - 2R * VP8[5:0]) / 322R, \Delta VDHP = (VGMP - VGSP)$
VGAMMAP9	15R	$VGAMMAP16 + ((VGAMMAP8 - VGAMMAP16) * (105R / 120R))$
VGAMMAP10	15R	$VGAMMAP16 + ((VGAMMAP8 - VGAMMAP16) * (90R / 120R))$
VGAMMAP11	15R	$VGAMMAP16 + ((VGAMMAP8 - VGAMMAP16) * (75R / 120R))$
VGAMMAP12	15R	$VGAMMAP16 + ((VGAMMAP8 - VGAMMAP16) * (60R / 120R))$
VGAMMAP13	15R	$VGAMMAP16 + ((VGAMMAP8 - VGAMMAP16) * (45R / 120R))$
VGAMMAP14	15R	$VGAMMAP16 + ((VGAMMAP8 - VGAMMAP16) * (30R / 120R))$
VGAMMAP15	15R	$VGAMMAP16 + ((VGAMMAP8 - VGAMMAP16) * (15R / 120R))$
VGAMMAP16	6R	$VGAMMAP52 + (VGAMMAP8 - VGAMMAP52) * ((50R - 1R * VP16[4:0]) / 51R)$
VGAMMAP17	6R	$VGAMMAP32 + ((VGAMMAP16 - VGAMMAP32) * (90R / 96R))$
VGAMMAP18	6R	$VGAMMAP32 + ((VGAMMAP16 - VGAMMAP32) * (84R / 96R))$
VGAMMAP19	6R	$VGAMMAP32 + ((VGAMMAP16 - VGAMMAP32) * (78R / 96R))$
VGAMMAP20	6R	$VGAMMAP32 + ((VGAMMAP16 - VGAMMAP32) * (72R / 96R))$
VGAMMAP21	6R	$VGAMMAP32 + ((VGAMMAP16 - VGAMMAP32) * (66R / 96R))$
VGAMMAP22	6R	$VGAMMAP32 + ((VGAMMAP16 - VGAMMAP32) * (60R / 96R))$
VGAMMAP23	6R	$VGAMMAP32 + ((VGAMMAP16 - VGAMMAP32) * (54R / 96R))$
VGAMMAP24	6R	$VGAMMAP32 + ((VGAMMAP16 - VGAMMAP32) * (48R / 96R))$
VGAMMAP25	6R	$VGAMMAP32 + ((VGAMMAP16 - VGAMMAP32) * (42R / 96R))$
VGAMMAP26	6R	$VGAMMAP32 + ((VGAMMAP16 - VGAMMAP32) * (36R / 96R))$
VGAMMAP27	6R	$VGAMMAP32 + ((VGAMMAP16 - VGAMMAP32) * (30R / 96R))$
VGAMMAP28	6R	$VGAMMAP32 + ((VGAMMAP16 - VGAMMAP32) * (24R / 96R))$
VGAMMAP29	6R	$VGAMMAP32 + ((VGAMMAP16 - VGAMMAP32) * (18R / 96R))$
VGAMMAP30	6R	$VGAMMAP32 + ((VGAMMAP16 - VGAMMAP32) * (12R / 96R))$
VGAMMAP31	6R	$VGAMMAP32 + ((VGAMMAP16 - VGAMMAP32) * (6R / 96R))$
VGAMMAP32	6R	$VGAMMAP52 + (VGAMMAP8 - VGAMMAP52) * ((32R - 1R * VP32[4:0]) / 51R)$
VGAMMAP33	6R	$VGAMMAP52 + ((VGAMMAP32 - VGAMMAP52) * (114R / 120R))$
VGAMMAP34	6R	$VGAMMAP52 + ((VGAMMAP32 - VGAMMAP52) * (108R / 120R))$
VGAMMAP35	6R	$VGAMMAP52 + ((VGAMMAP32 - VGAMMAP52) * (102R / 120R))$
VGAMMAP36	6R	$VGAMMAP52 + ((VGAMMAP32 - VGAMMAP52) * (96R / 120R))$
VGAMMAP37	6R	$VGAMMAP52 + ((VGAMMAP32 - VGAMMAP52) * (90R / 120R))$
VGAMMAP38	6R	$VGAMMAP52 + ((VGAMMAP32 - VGAMMAP52) * (84R / 120R))$
VGAMMAP39	6R	$VGAMMAP52 + ((VGAMMAP32 - VGAMMAP52) * (78R / 120R))$
VGAMMAP40	6R	$VGAMMAP52 + ((VGAMMAP32 - VGAMMAP52) * (72R / 120R))$
VGAMMAP41	6R	$VGAMMAP52 + ((VGAMMAP32 - VGAMMAP52) * (66R / 120R))$
VGAMMAP42	6R	$VGAMMAP52 + ((VGAMMAP32 - VGAMMAP52) * (60R / 120R))$
VGAMMAP43	6R	$VGAMMAP52 + ((VGAMMAP32 - VGAMMAP52) * (54R / 120R))$
VGAMMAP44	6R	$VGAMMAP52 + ((VGAMMAP32 - VGAMMAP52) * (48R / 120R))$

VGAMMAP45	6R	$VGAMMAP52 + ((VGAMMAP32 - VGAMMAP52) * (42R/120R))$
VGAMMAP46	6R	$VGAMMAP52 + ((VGAMMAP32 - VGAMMAP52) * (36R/120R))$
VGAMMAP47	6R	$VGAMMAP52 + ((VGAMMAP32 - VGAMMAP52) * (30R/120R))$
VGAMMAP48	6R	$VGAMMAP52 + ((VGAMMAP32 - VGAMMAP52) * (24R/120R))$
VGAMMAP49	6R	$VGAMMAP52 + ((VGAMMAP32 - VGAMMAP52) * (18R/120R))$
VGAMMAP50	6R	$VGAMMAP52 + ((VGAMMAP32 - VGAMMAP52) * (12R/120R))$
VGAMMAP51	6R	$VGAMMAP52 + ((VGAMMAP32 - VGAMMAP52) * (6R/120R))$
VGAMMAP52	3R	$VGAMMAP247 + (VGAMMAP8 - VGAMMAP247) * ((77R - 0R)/90R)$, VP52[4:0] = 0(Dec) $VGAMMAP247 + (VGAMMAP8 - VGAMMAP247) * ((77R - 2R)/90R)$, VP52[4:0] = 1(Dec) $VGAMMAP247 + (VGAMMAP8 - VGAMMAP247) * ((77R - 4R)/90R)$, VP52[4:0] = 2(Dec) $VGAMMAP247 + (VGAMMAP8 - VGAMMAP247) * ((74R - 1R * VP52[4:0])/90R)$, else
VGAMMAP53	3R	$VGAMMAP80 + ((VGAMMAP52 - VGAMMAP80) * (81R/84R))$
VGAMMAP54	3R	$VGAMMAP80 + ((VGAMMAP52 - VGAMMAP80) * (78R/84R))$
VGAMMAP55	3R	$VGAMMAP80 + ((VGAMMAP52 - VGAMMAP80) * (75R/84R))$
VGAMMAP56	3R	$VGAMMAP80 + ((VGAMMAP52 - VGAMMAP80) * (72R/84R))$
VGAMMAP57	3R	$VGAMMAP80 + ((VGAMMAP52 - VGAMMAP80) * (69R/84R))$
VGAMMAP58	3R	$VGAMMAP80 + ((VGAMMAP52 - VGAMMAP80) * (66R/84R))$
VGAMMAP59	3R	$VGAMMAP80 + ((VGAMMAP52 - VGAMMAP80) * (63R/84R))$
VGAMMAP60	3R	$VGAMMAP80 + ((VGAMMAP52 - VGAMMAP80) * (60R/84R))$
VGAMMAP61	3R	$VGAMMAP80 + ((VGAMMAP52 - VGAMMAP80) * (57R/84R))$
VGAMMAP62	3R	$VGAMMAP80 + ((VGAMMAP52 - VGAMMAP80) * (54R/84R))$
VGAMMAP63	3R	$VGAMMAP80 + ((VGAMMAP52 - VGAMMAP80) * (51R/84R))$
VGAMMAP64	3R	$VGAMMAP80 + ((VGAMMAP52 - VGAMMAP80) * (48R/84R))$
VGAMMAP65	3R	$VGAMMAP80 + ((VGAMMAP52 - VGAMMAP80) * (45R/84R))$
VGAMMAP66	3R	$VGAMMAP80 + ((VGAMMAP52 - VGAMMAP80) * (42R/84R))$
VGAMMAP67	3R	$VGAMMAP80 + ((VGAMMAP52 - VGAMMAP80) * (39R/84R))$
VGAMMAP68	3R	$VGAMMAP80 + ((VGAMMAP52 - VGAMMAP80) * (36R/84R))$
VGAMMAP69	3R	$VGAMMAP80 + ((VGAMMAP52 - VGAMMAP80) * (33R/84R))$
VGAMMAP70	3R	$VGAMMAP80 + ((VGAMMAP52 - VGAMMAP80) * (30R/84R))$
VGAMMAP71	3R	$VGAMMAP80 + ((VGAMMAP52 - VGAMMAP80) * (27R/84R))$
VGAMMAP72	3R	$VGAMMAP80 + ((VGAMMAP52 - VGAMMAP80) * (24R/84R))$
VGAMMAP73	3R	$VGAMMAP80 + ((VGAMMAP52 - VGAMMAP80) * (21R/84R))$
VGAMMAP74	3R	$VGAMMAP80 + ((VGAMMAP52 - VGAMMAP80) * (18R/84R))$
VGAMMAP75	3R	$VGAMMAP80 + ((VGAMMAP52 - VGAMMAP80) * (15R/84R))$
VGAMMAP76	3R	$VGAMMAP80 + ((VGAMMAP52 - VGAMMAP80) * (12R/84R))$
VGAMMAP77	3R	$VGAMMAP80 + ((VGAMMAP52 - VGAMMAP80) * (9R/84R))$
VGAMMAP78	3R	$VGAMMAP80 + ((VGAMMAP52 - VGAMMAP80) * (6R/84R))$

VGAMMAP79	3R	$VGAMMAP80 + ((VGAMMAP52 - VGAMMAP80) * (3R/84R))$
VGAMMAP80	3R	$VGAMMAP203 + (VGAMMAP52 - VGAMMAP203) * ((68R - 0R)/75R)$, VP80[3:0] =0(Dec) $VGAMMAP203 + (VGAMMAP52 - VGAMMAP203) * ((68R - 2R)/75R)$, VP80[3:0] =1(Dec) $VGAMMAP203 + (VGAMMAP52 - VGAMMAP203) * ((68R - 4R)/75R)$, VP80[3:0] =2(Dec) $VGAMMAP203 + (VGAMMAP52 - VGAMMAP203) * ((65R - 1R * VP80[3:0])/75R)$, else
VGAMMAP81	3R	$VGAMMAP108 + ((VGAMMAP80 - VGAMMAP108) * (81R/84R))$
VGAMMAP82	3R	$VGAMMAP108 + ((VGAMMAP80 - VGAMMAP108) * (78R/84R))$
VGAMMAP83	3R	$VGAMMAP108 + ((VGAMMAP80 - VGAMMAP108) * (75R/84R))$
VGAMMAP84	3R	$VGAMMAP108 + ((VGAMMAP80 - VGAMMAP108) * (72R/84R))$
VGAMMAP85	3R	$VGAMMAP108 + ((VGAMMAP80 - VGAMMAP108) * (69R/84R))$
VGAMMAP86	3R	$VGAMMAP108 + ((VGAMMAP80 - VGAMMAP108) * (66R/84R))$
VGAMMAP87	3R	$VGAMMAP108 + ((VGAMMAP80 - VGAMMAP108) * (63R/84R))$
VGAMMAP88	3R	$VGAMMAP108 + ((VGAMMAP80 - VGAMMAP108) * (60R/84R))$
VGAMMAP89	3R	$VGAMMAP108 + ((VGAMMAP80 - VGAMMAP108) * (57R/84R))$
VGAMMAP90	3R	$VGAMMAP108 + ((VGAMMAP80 - VGAMMAP108) * (54R/84R))$
VGAMMAP91	3R	$VGAMMAP108 + ((VGAMMAP80 - VGAMMAP108) * (51R/84R))$
VGAMMAP92	3R	$VGAMMAP108 + ((VGAMMAP80 - VGAMMAP108) * (48R/84R))$
VGAMMAP93	3R	$VGAMMAP108 + ((VGAMMAP80 - VGAMMAP108) * (45R/84R))$
VGAMMAP94	3R	$VGAMMAP108 + ((VGAMMAP80 - VGAMMAP108) * (42R/84R))$
VGAMMAP95	3R	$VGAMMAP108 + ((VGAMMAP80 - VGAMMAP108) * (39R/84R))$
VGAMMAP96	3R	$VGAMMAP108 + ((VGAMMAP80 - VGAMMAP108) * (36R/84R))$
VGAMMAP97	3R	$VGAMMAP108 + ((VGAMMAP80 - VGAMMAP108) * (33R/84R))$
VGAMMAP98	3R	$VGAMMAP108 + ((VGAMMAP80 - VGAMMAP108) * (30R/84R))$
VGAMMAP99	3R	$VGAMMAP108 + ((VGAMMAP80 - VGAMMAP108) * (27R/84R))$
VGAMMAP100	3R	$VGAMMAP108 + ((VGAMMAP80 - VGAMMAP108) * (24R/84R))$
VGAMMAP101	3R	$VGAMMAP108 + ((VGAMMAP80 - VGAMMAP108) * (21R/84R))$
VGAMMAP102	3R	$VGAMMAP108 + ((VGAMMAP80 - VGAMMAP108) * (18R/84R))$
VGAMMAP103	3R	$VGAMMAP108 + ((VGAMMAP80 - VGAMMAP108) * (15R/84R))$
VGAMMAP104	3R	$VGAMMAP108 + ((VGAMMAP80 - VGAMMAP108) * (12R/84R))$
VGAMMAP105	3R	$VGAMMAP108 + ((VGAMMAP80 - VGAMMAP108) * (9R/84R))$
VGAMMAP106	3R	$VGAMMAP108 + ((VGAMMAP80 - VGAMMAP108) * (6R/84R))$
VGAMMAP107	3R	$VGAMMAP108 + ((VGAMMAP80 - VGAMMAP108) * (3R/84R))$
VGAMMAP108	3R	$VGAMMAP203 + (VGAMMAP52 - VGAMMAP203) * ((52R - 0R)/75R)$, VP108[3:0] =0(Dec) $VGAMMAP203 + (VGAMMAP52 - VGAMMAP203) * ((52R - 2R)/75R)$, VP108[3:0] =1(Dec) $VGAMMAP203 + (VGAMMAP52 - VGAMMAP203) * ((52R - 4R)/75R)$, VP108[3:0] =2(Dec) $VGAMMAP203 + (VGAMMAP52 - VGAMMAP203) * ((49R - 1R * VP108[3:0])/75R)$, else
VGAMMAP109	3R	$VGAMMAP147 + ((VGAMMAP108 - VGAMMAP147) * (114R/117R))$

VGAMMAP110	3R	VGAMMAP147+((VGAMMAP108-VGAMMAP147)*(111R/117R)
VGAMMAP111	3R	VGAMMAP147+((VGAMMAP108-VGAMMAP147)*(108R/117R)
VGAMMAP112	3R	VGAMMAP147+((VGAMMAP108-VGAMMAP147)*(105R/117R)
VGAMMAP113	3R	VGAMMAP147+((VGAMMAP108-VGAMMAP147)*(102R/117R)
VGAMMAP114	3R	VGAMMAP147+((VGAMMAP108-VGAMMAP147)*(99R/117R)
VGAMMAP115	3R	VGAMMAP147+((VGAMMAP108-VGAMMAP147)*(96R/117R)
VGAMMAP116	3R	VGAMMAP147+((VGAMMAP108-VGAMMAP147)*(93R/117R)
VGAMMAP117	3R	VGAMMAP147+((VGAMMAP108-VGAMMAP147)*(90R/117R)
VGAMMAP118	3R	VGAMMAP147+((VGAMMAP108-VGAMMAP147)*(87R/117R)
VGAMMAP119	3R	VGAMMAP147+((VGAMMAP108-VGAMMAP147)*(84R/117R)
VGAMMAP120	3R	VGAMMAP147+((VGAMMAP108-VGAMMAP147)*(81R/117R)
VGAMMAP121	3R	VGAMMAP147+((VGAMMAP108-VGAMMAP147)*(78R/117R)
VGAMMAP122	3R	VGAMMAP147+((VGAMMAP108-VGAMMAP147)*(75R/117R)
VGAMMAP123	3R	VGAMMAP147+((VGAMMAP108-VGAMMAP147)*(72R/117R)
VGAMMAP124	3R	VGAMMAP147+((VGAMMAP108-VGAMMAP147)*(69R/117R)
VGAMMAP125	3R	VGAMMAP147+((VGAMMAP108-VGAMMAP147)*(66R/117R)
VGAMMAP126	3R	VGAMMAP147+((VGAMMAP108-VGAMMAP147)*(63R/117R)
VGAMMAP127	3R	VGAMMAP147+((VGAMMAP108-VGAMMAP147)*(60R/117R)
VGAMMAP128	3R	VGAMMAP147+((VGAMMAP108-VGAMMAP147)*(57R/117R)
VGAMMAP129	3R	VGAMMAP147+((VGAMMAP108-VGAMMAP147)*(54R/117R)
VGAMMAP130	3R	VGAMMAP147+((VGAMMAP108-VGAMMAP147)*(51R/117R)
VGAMMAP131	3R	VGAMMAP147+((VGAMMAP108-VGAMMAP147)*(48R/117R)
VGAMMAP132	3R	VGAMMAP147+((VGAMMAP108-VGAMMAP147)*(45R/117R)
VGAMMAP133	3R	VGAMMAP147+((VGAMMAP108-VGAMMAP147)*(42R/117R)
VGAMMAP134	3R	VGAMMAP147+((VGAMMAP108-VGAMMAP147)*(39R/117R)
VGAMMAP135	3R	VGAMMAP147+((VGAMMAP108-VGAMMAP147)*(36R/117R)
VGAMMAP136	3R	VGAMMAP147+((VGAMMAP108-VGAMMAP147)*(33R/117R)
VGAMMAP137	3R	VGAMMAP147+((VGAMMAP108-VGAMMAP147)*(30R/117R)
VGAMMAP138	3R	VGAMMAP147+((VGAMMAP108-VGAMMAP147)*(27R/117R)
VGAMMAP139	3R	VGAMMAP147+((VGAMMAP108-VGAMMAP147)*(24R/117R)
VGAMMAP140	3R	VGAMMAP147+((VGAMMAP108-VGAMMAP147)*(21R/117R)
VGAMMAP141	3R	VGAMMAP147+((VGAMMAP108-VGAMMAP147)*(18R/117R)
VGAMMAP142	3R	VGAMMAP147+((VGAMMAP108-VGAMMAP147)*(15R/117R)
VGAMMAP143	3R	VGAMMAP147+((VGAMMAP108-VGAMMAP147)*(12R/117R)
VGAMMAP144	3R	VGAMMAP147+((VGAMMAP108-VGAMMAP147)*(9R/117R)
VGAMMAP145	3R	VGAMMAP147+((VGAMMAP108-VGAMMAP147)*(6R/117R)
VGAMMAP146	3R	VGAMMAP147+((VGAMMAP108-VGAMMAP147)*(3R/117R)

VGAMMAP147	3R	$\text{VGAMMAP203} + (\text{VGAMMAP52} - \text{VGAMMAP203}) * ((17R + 1R * VP147[3:0]) / 75R) , \text{ else}$ $\text{VGAMMAP203} + (\text{VGAMMAP52} - \text{VGAMMAP203}) * ((17R + 31R / 75R) , VP147[3:0] = 13(\text{Dec})$ $\text{VGAMMAP203} + (\text{VGAMMAP52} - \text{VGAMMAP203}) * ((17R + 33R / 75R) , VP147[3:0] = 14(\text{Dec})$ $\text{VGAMMAP203} + (\text{VGAMMAP52} - \text{VGAMMAP203}) * ((17R + 35R / 75R) , VP147[3:0] = 15(\text{Dec})$
VGAMMAP148	3R	$\text{VGAMMAP175} + ((\text{VGAMMAP147} - \text{VGAMMAP175}) * (81R / 84R))$
VGAMMAP149	3R	$\text{VGAMMAP175} + ((\text{VGAMMAP147} - \text{VGAMMAP175}) * (78R / 84R))$
VGAMMAP150	3R	$\text{VGAMMAP175} + ((\text{VGAMMAP147} - \text{VGAMMAP175}) * (75R / 84R))$
VGAMMAP151	3R	$\text{VGAMMAP175} + ((\text{VGAMMAP147} - \text{VGAMMAP175}) * (72R / 84R))$
VGAMMAP152	3R	$\text{VGAMMAP175} + ((\text{VGAMMAP147} - \text{VGAMMAP175}) * (69R / 84R))$
VGAMMAP153	3R	$\text{VGAMMAP175} + ((\text{VGAMMAP147} - \text{VGAMMAP175}) * (66R / 84R))$
VGAMMAP154	3R	$\text{VGAMMAP175} + ((\text{VGAMMAP147} - \text{VGAMMAP175}) * (63R / 84R))$
VGAMMAP155	3R	$\text{VGAMMAP175} + ((\text{VGAMMAP147} - \text{VGAMMAP175}) * (60R / 84R))$
VGAMMAP156	3R	$\text{VGAMMAP175} + ((\text{VGAMMAP147} - \text{VGAMMAP175}) * (57R / 84R))$
VGAMMAP157	3R	$\text{VGAMMAP175} + ((\text{VGAMMAP147} - \text{VGAMMAP175}) * (54R / 84R))$
VGAMMAP158	3R	$\text{VGAMMAP175} + ((\text{VGAMMAP147} - \text{VGAMMAP175}) * (51R / 84R))$
VGAMMAP159	3R	$\text{VGAMMAP175} + ((\text{VGAMMAP147} - \text{VGAMMAP175}) * (48R / 84R))$
VGAMMAP160	3R	$\text{VGAMMAP175} + ((\text{VGAMMAP147} - \text{VGAMMAP175}) * (45R / 84R))$
VGAMMAP161	3R	$\text{VGAMMAP175} + ((\text{VGAMMAP147} - \text{VGAMMAP175}) * (42R / 84R))$
VGAMMAP162	3R	$\text{VGAMMAP175} + ((\text{VGAMMAP147} - \text{VGAMMAP175}) * (39R / 84R))$
VGAMMAP163	3R	$\text{VGAMMAP175} + ((\text{VGAMMAP147} - \text{VGAMMAP175}) * (36R / 84R))$
VGAMMAP164	3R	$\text{VGAMMAP175} + ((\text{VGAMMAP147} - \text{VGAMMAP175}) * (33R / 84R))$
VGAMMAP165	3R	$\text{VGAMMAP175} + ((\text{VGAMMAP147} - \text{VGAMMAP175}) * (30R / 84R))$
VGAMMAP166	3R	$\text{VGAMMAP175} + ((\text{VGAMMAP147} - \text{VGAMMAP175}) * (27R / 84R))$
VGAMMAP167	3R	$\text{VGAMMAP175} + ((\text{VGAMMAP147} - \text{VGAMMAP175}) * (24R / 84R))$
VGAMMAP168	3R	$\text{VGAMMAP175} + ((\text{VGAMMAP147} - \text{VGAMMAP175}) * (21R / 84R))$
VGAMMAP169	3R	$\text{VGAMMAP175} + ((\text{VGAMMAP147} - \text{VGAMMAP175}) * (18R / 84R))$
VGAMMAP170	3R	$\text{VGAMMAP175} + ((\text{VGAMMAP147} - \text{VGAMMAP175}) * (15R / 84R))$
VGAMMAP171	3R	$\text{VGAMMAP175} + ((\text{VGAMMAP147} - \text{VGAMMAP175}) * (12R / 84R))$
VGAMMAP172	3R	$\text{VGAMMAP175} + ((\text{VGAMMAP147} - \text{VGAMMAP175}) * (9R / 84R))$
VGAMMAP173	3R	$\text{VGAMMAP175} + ((\text{VGAMMAP147} - \text{VGAMMAP175}) * (6R / 84R))$
VGAMMAP174	3R	$\text{VGAMMAP175} + ((\text{VGAMMAP147} - \text{VGAMMAP175}) * (3R / 84R))$
VGAMMAP175	3R	$\text{VGAMMAP203} + (\text{VGAMMAP52} - \text{VGAMMAP203}) * ((1R + 1R * VP175[3:0]) / 75R) , \text{ else}$ $\text{VGAMMAP203} + (\text{VGAMMAP52} - \text{VGAMMAP203}) * ((1R + 15R / 75R) , VP175[3:0] = 13(\text{Dec})$ $\text{VGAMMAP203} + (\text{VGAMMAP52} - \text{VGAMMAP203}) * ((1R + 17R / 75R) , VP175[3:0] = 14(\text{Dec})$ $\text{VGAMMAP203} + (\text{VGAMMAP52} - \text{VGAMMAP203}) * ((1R + 19R / 75R) , VP175[3:0] = 15(\text{Dec})$
VGAMMAP176	3R	$\text{VGAMMAP203} + ((\text{VGAMMAP175} - \text{VGAMMAP203}) * (81R / 84R))$
VGAMMAP177	3R	$\text{VGAMMAP203} + ((\text{VGAMMAP175} - \text{VGAMMAP203}) * (78R / 84R))$

VGAMMAP178	3R	$VGAMMAP203 + ((VGAMMAP175 - VGAMMAP203) * (75R/84R))$
VGAMMAP179	3R	$VGAMMAP203 + ((VGAMMAP175 - VGAMMAP203) * (72R/84R))$
VGAMMAP180	3R	$VGAMMAP203 + ((VGAMMAP175 - VGAMMAP203) * (69R/84R))$
VGAMMAP181	3R	$VGAMMAP203 + ((VGAMMAP175 - VGAMMAP203) * (66R/84R))$
VGAMMAP182	3R	$VGAMMAP203 + ((VGAMMAP175 - VGAMMAP203) * (63R/84R))$
VGAMMAP183	3R	$VGAMMAP203 + ((VGAMMAP175 - VGAMMAP203) * (60R/84R))$
VGAMMAP184	3R	$VGAMMAP203 + ((VGAMMAP175 - VGAMMAP203) * (57R/84R))$
VGAMMAP185	3R	$VGAMMAP203 + ((VGAMMAP175 - VGAMMAP203) * (54R/84R))$
VGAMMAP186	3R	$VGAMMAP203 + ((VGAMMAP175 - VGAMMAP203) * (51R/84R))$
VGAMMAP187	3R	$VGAMMAP203 + ((VGAMMAP175 - VGAMMAP203) * (48R/84R))$
VGAMMAP188	3R	$VGAMMAP203 + ((VGAMMAP175 - VGAMMAP203) * (45R/84R))$
VGAMMAP189	3R	$VGAMMAP203 + ((VGAMMAP175 - VGAMMAP203) * (42R/84R))$
VGAMMAP190	3R	$VGAMMAP203 + ((VGAMMAP175 - VGAMMAP203) * (39R/84R))$
VGAMMAP191	3R	$VGAMMAP203 + ((VGAMMAP175 - VGAMMAP203) * (36R/84R))$
VGAMMAP192	3R	$VGAMMAP203 + ((VGAMMAP175 - VGAMMAP203) * (33R/84R))$
VGAMMAP193	3R	$VGAMMAP203 + ((VGAMMAP175 - VGAMMAP203) * (30R/84R))$
VGAMMAP194	3R	$VGAMMAP203 + ((VGAMMAP175 - VGAMMAP203) * (27R/84R))$
VGAMMAP195	3R	$VGAMMAP203 + ((VGAMMAP175 - VGAMMAP203) * (24R/84R))$
VGAMMAP196	3R	$VGAMMAP203 + ((VGAMMAP175 - VGAMMAP203) * (21R/84R))$
VGAMMAP197	3R	$VGAMMAP203 + ((VGAMMAP175 - VGAMMAP203) * (18R/84R))$
VGAMMAP198	3R	$VGAMMAP203 + ((VGAMMAP175 - VGAMMAP203) * (15R/84R))$
VGAMMAP199	3R	$VGAMMAP203 + ((VGAMMAP175 - VGAMMAP203) * (12R/84R))$
VGAMMAP200	3R	$VGAMMAP203 + ((VGAMMAP175 - VGAMMAP203) * (9R/84R))$
VGAMMAP201	3R	$VGAMMAP203 + ((VGAMMAP175 - VGAMMAP203) * (6R/84R))$
VGAMMAP202	3R	$VGAMMAP203 + ((VGAMMAP175 - VGAMMAP203) * (3R/84R))$
VGAMMAP203	6R	$VGAMMAP247 + (VGAMMAP8 - VGAMMAP247) * ((8R + 1R * VP203[4:0]) / 90R)$, else $VGAMMAP247 + (VGAMMAP8 - VGAMMAP247) * ((8R + 38R / 90R))$, $VP203[4:0] = 29(Dec)$ $VGAMMAP247 + (VGAMMAP8 - VGAMMAP247) * ((8R + 40R / 90R))$, $VP203[4:0] = 30(Dec)$ $VGAMMAP247 + (VGAMMAP8 - VGAMMAP247) * ((8R + 42R / 90R))$, $VP203[4:0] = 31(Dec)$
VGAMMAP204	6R	$VGAMMAP223 + ((VGAMMAP203 - VGAMMAP223) * (114R/120R))$
VGAMMAP205	6R	$VGAMMAP223 + ((VGAMMAP203 - VGAMMAP223) * (108R/120R))$
VGAMMAP206	6R	$VGAMMAP223 + ((VGAMMAP203 - VGAMMAP223) * (102R/120R))$
VGAMMAP207	6R	$VGAMMAP223 + ((VGAMMAP203 - VGAMMAP223) * (96R/120R))$
VGAMMAP208	6R	$VGAMMAP223 + ((VGAMMAP203 - VGAMMAP223) * (90R/120R))$
VGAMMAP209	6R	$VGAMMAP223 + ((VGAMMAP203 - VGAMMAP223) * (84R/120R))$
VGAMMAP210	6R	$VGAMMAP223 + ((VGAMMAP203 - VGAMMAP223) * (78R/120R))$
VGAMMAP211	6R	$VGAMMAP223 + ((VGAMMAP203 - VGAMMAP223) * (72R/120R))$

VGAMMAP212	6R	$VGAMMAP223 + (VGAMMAP203 - VGAMMAP223) * (66R/120R)$
VGAMMAP213	6R	$VGAMMAP223 + (VGAMMAP203 - VGAMMAP223) * (60R/120R)$
VGAMMAP214	6R	$VGAMMAP223 + (VGAMMAP203 - VGAMMAP223) * (54R/120R)$
VGAMMAP215	6R	$VGAMMAP223 + (VGAMMAP203 - VGAMMAP223) * (48R/120R)$
VGAMMAP216	6R	$VGAMMAP223 + (VGAMMAP203 - VGAMMAP223) * (42R/120R)$
VGAMMAP217	6R	$VGAMMAP223 + (VGAMMAP203 - VGAMMAP223) * (36R/120R)$
VGAMMAP218	6R	$VGAMMAP223 + (VGAMMAP203 - VGAMMAP223) * (30R/120R)$
VGAMMAP219	6R	$VGAMMAP223 + (VGAMMAP203 - VGAMMAP223) * (24R/120R)$
VGAMMAP220	6R	$VGAMMAP223 + (VGAMMAP203 - VGAMMAP223) * (18R/120R)$
VGAMMAP221	6R	$VGAMMAP223 + (VGAMMAP203 - VGAMMAP223) * (12R/120R)$
VGAMMAP222	6R	$VGAMMAP223 + (VGAMMAP203 - VGAMMAP223) * (6R/120R)$
VGAMMAP223	6R	$VGAMMAP247 + (VGAMMAP203 - VGAMMAP247) * ((19R + 1R * VP223[4:0]) / 51R)$
VGAMMAP224	6R	$VGAMMAP239 + (VGAMMAP223 - VGAMMAP239) * (90R/96R)$
VGAMMAP225	6R	$VGAMMAP239 + (VGAMMAP223 - VGAMMAP239) * (84R/96R)$
VGAMMAP226	6R	$VGAMMAP239 + (VGAMMAP223 - VGAMMAP239) * (78R/96R)$
VGAMMAP227	6R	$VGAMMAP239 + (VGAMMAP223 - VGAMMAP239) * (72R/96R)$
VGAMMAP228	6R	$VGAMMAP239 + (VGAMMAP223 - VGAMMAP239) * (66R/96R)$
VGAMMAP229	6R	$VGAMMAP239 + (VGAMMAP223 - VGAMMAP239) * (60R/96R)$
VGAMMAP230	6R	$VGAMMAP239 + (VGAMMAP223 - VGAMMAP239) * (54R/96R)$
VGAMMAP231	6R	$VGAMMAP239 + (VGAMMAP223 - VGAMMAP239) * (48R/96R)$
VGAMMAP232	6R	$VGAMMAP239 + (VGAMMAP223 - VGAMMAP239) * (42R/96R)$
VGAMMAP233	6R	$VGAMMAP239 + (VGAMMAP223 - VGAMMAP239) * (36R/96R)$
VGAMMAP234	6R	$VGAMMAP239 + (VGAMMAP223 - VGAMMAP239) * (30R/96R)$
VGAMMAP235	6R	$VGAMMAP239 + (VGAMMAP223 - VGAMMAP239) * (24R/96R)$
VGAMMAP236	6R	$VGAMMAP239 + (VGAMMAP223 - VGAMMAP239) * (18R/96R)$
VGAMMAP237	6R	$VGAMMAP239 + (VGAMMAP223 - VGAMMAP239) * (12R/96R)$
VGAMMAP238	6R	$VGAMMAP239 + (VGAMMAP223 - VGAMMAP239) * (6R/96R)$
VGAMMAP239	15R	$VGAMMAP247 + (VGAMMAP203 - VGAMMAP247) * ((1R + 1R * VP239[4:0]) / 51R)$
VGAMMAP240	15R	$VGAMMAP247 + (VGAMMAP239 - VGAMMAP247) * (105R/120R)$
VGAMMAP241	15R	$VGAMMAP247 + (VGAMMAP239 - VGAMMAP247) * (90R/120R)$
VGAMMAP242	15R	$VGAMMAP247 + (VGAMMAP239 - VGAMMAP247) * (75R/120R)$
VGAMMAP243	15R	$VGAMMAP247 + (VGAMMAP239 - VGAMMAP247) * (60R/120R)$
VGAMMAP244	15R	$VGAMMAP247 + (VGAMMAP239 - VGAMMAP247) * (45R/120R)$
VGAMMAP245	15R	$VGAMMAP247 + (VGAMMAP239 - VGAMMAP247) * (30R/120R)$
VGAMMAP246	15R	$VGAMMAP247 + (VGAMMAP239 - VGAMMAP247) * (15R/120R)$
VGAMMAP247	30R	$VGSP + \Delta VDHP (3R * VP247[5:0]) / 322R, \Delta VDHP = (VGMP - VGSP)$
VGAMMAP248	30R	$VGAMMAP251 + (VGAMMAP247 - VGAMMAP251) * (90R/120R)$

VGAMMAP249	30R	$VGAMMAP251 + ((VGAMMAP247 - VGAMMAP251) * (60R / 120R))$
VGAMMAP250	30R	$VGAMMAP251 + ((VGAMMAP247 - VGAMMAP251) * (30R / 120R))$
VGAMMAP251	6R	$VGSP + \Delta VDHP (3R * VP251[5:0]) / 322R$, $\Delta VDHP = (VGMP - VGSP)$
VGAMMAP252	12R	$VGAMMAP255 + (VGAMMAP251 - VGAMMAP255) * (RCGPL + 6R + 12R) / (42R + RCGNH)$
VGAMMAP253	24R	$VGAMMAP255 + (VGAMMAP251 - VGAMMAP255) * (RCGPL + 6R) / (42R + RCGNH)$
VGAMMAP254	24R	$VGAMMAP255 + (VGAMMAP251 - VGAMMAP255) * (RCGPL) / (42R + RCGPL)$
VGAMMAP255	0R	$VGSP + \Delta VDHP (3R * VP255[5:0]) / 322R$, $\Delta VDHP = (VGMP - VGSP)$

Negative polarity	Resister stream	Gamma 256 grayscale voltage calculation formula
VGAMMAN255	24R	$VG_{MN} + \Delta V_{DHN} (322R - 2R \cdot VN_{255}[5:0]) / 322R$, $\Delta V_{DHN} = (V_{GSN} - V_{GMN})$
VGAMMAN254	24R	$VG_{AMMAN251} + (VG_{AMMN255} - VG_{AMMAN251}) \cdot (6R + 12R + 24R) / (42R + R_{CGNL} + 24R)$
VGAMMAN253	12R	$VG_{AMMAN251} + (VG_{AMMN255} - VG_{AMMAN251}) \cdot (6R + 12R) / (42R + R_{CGNL} + 24R)$
VGAMMAN252	6R	$VG_{AMMAN251} + (VG_{AMMN255} - VG_{AMMAN251}) \cdot (6R) / (42R + R_{CGNL} + 24R)$
VGAMMAN251	30R	$VG_{MN} + \Delta V_{DHN} (322R - 2R \cdot VN_{251}[5:0]) / 322R$, $\Delta V_{DHN} = (V_{GSN} - V_{GMN})$
VGAMMAN250	30R	$VG_{AMMAN247} + (VG_{AMMAN251} - VG_{AMMAN247}) \cdot (90R / 120R)$
VGAMMAN249	30R	$VG_{AMMAN247} + (VG_{AMMAN251} - VG_{AMMAN247}) \cdot (60R / 120R)$
VGAMMAN248	30R	$VG_{AMMAN247} + (VG_{AMMAN251} - VG_{AMMAN247}) \cdot (30R / 120R)$
VGAMMAN247	15R	$VG_{MN} + \Delta V_{DHN} (322R - 2R \cdot VN_{247}[5:0]) / 322R$, $\Delta V_{DHN} = (V_{GSN} - V_{GMN})$
VGAMMAN246	15R	$VG_{AMMAN239} + (VG_{AMMAN247} - VG_{AMMAN239}) \cdot (105R / 120R)$
VGAMMAN245	15R	$VG_{AMMAN239} + (VG_{AMMAN247} - VG_{AMMAN239}) \cdot (90R / 120R)$
VGAMMAN244	15R	$VG_{AMMAN239} + (VG_{AMMAN247} - VG_{AMMAN239}) \cdot (75R / 120R)$
VGAMMAN243	15R	$VG_{AMMAN239} + (VG_{AMMAN247} - VG_{AMMAN239}) \cdot (60R / 120R)$
VGAMMAN242	15R	$VG_{AMMAN239} + (VG_{AMMAN247} - VG_{AMMAN239}) \cdot (45R / 120R)$
VGAMMAN241	15R	$VG_{AMMAN239} + (VG_{AMMAN247} - VG_{AMMAN239}) \cdot (30R / 120R)$
VGAMMAN240	15R	$VG_{AMMAN239} + (VG_{AMMAN247} - VG_{AMMAN239}) \cdot (15R / 120R)$
VGAMMAN239	6R	$VG_{AMMAN203} + (VG_{AMMAN247} - VG_{AMMAN203}) \cdot (50R - 1R \cdot VN_{239}[4:0]) / 51R$
VGAMMAN238	6R	$VG_{AMMAN232} + (VG_{AMMAN239} - VG_{AMMAN232}) \cdot (90R / 96R)$
VGAMMAN237	6R	$VG_{AMMAN232} + (VG_{AMMAN239} - VG_{AMMAN232}) \cdot (84R / 96R)$
VGAMMAN236	6R	$VG_{AMMAN232} + (VG_{AMMAN239} - VG_{AMMAN232}) \cdot (78R / 96R)$
VGAMMAN235	6R	$VG_{AMMAN232} + (VG_{AMMAN239} - VG_{AMMAN232}) \cdot (72R / 96R)$
VGAMMAN234	6R	$VG_{AMMAN232} + (VG_{AMMAN239} - VG_{AMMAN232}) \cdot (66R / 96R)$
VGAMMAN233	6R	$VG_{AMMAN232} + (VG_{AMMAN239} - VG_{AMMAN232}) \cdot (60R / 96R)$
VGAMMAN232	6R	$VG_{AMMAN232} + (VG_{AMMAN239} - VG_{AMMAN232}) \cdot (54R / 96R)$
VGAMMAN231	6R	$VG_{AMMAN232} + (VG_{AMMAN239} - VG_{AMMAN232}) \cdot (48R / 96R)$
VGAMMAN230	6R	$VG_{AMMAN232} + (VG_{AMMAN239} - VG_{AMMAN232}) \cdot (42R / 96R)$
VGAMMAN229	6R	$VG_{AMMAN232} + (VG_{AMMAN239} - VG_{AMMAN232}) \cdot (36R / 96R)$
VGAMMAN228	6R	$VG_{AMMAN232} + (VG_{AMMAN239} - VG_{AMMAN232}) \cdot (30R / 96R)$
VGAMMAN227	6R	$VG_{AMMAN232} + (VG_{AMMAN239} - VG_{AMMAN232}) \cdot (24R / 96R)$
VGAMMAN226	6R	$VG_{AMMAN232} + (VG_{AMMAN239} - VG_{AMMAN232}) \cdot (18R / 96R)$
VGAMMAN225	6R	$VG_{AMMAN232} + (VG_{AMMAN239} - VG_{AMMAN232}) \cdot (12R / 96R)$
VGAMMAN224	6R	$VG_{AMMAN232} + (VG_{AMMAN239} - VG_{AMMAN232}) \cdot (6R / 96R)$
VGAMMAN223	6R	$VG_{AMMAN203} + (VG_{AMMAN247} - VG_{AMMAN203}) \cdot ((32R - 1R \cdot VN_{223}[4:0]) / 51R)$
VGAMMAN222	6R	$VG_{AMMAN203} + (VG_{AMMAN223} - VG_{AMMAN203}) \cdot (114R / 120R)$
VGAMMAN221	6R	$VG_{AMMAN203} + (VG_{AMMAN223} - VG_{AMMAN203}) \cdot (108R / 120R)$

VGAMMAN220	6R	VGAMMAN203+((VGAMMAN223-VGAMMAN203)*(102R/120R)
VGAMMAN219	6R	VGAMMAN203+((VGAMMAN223-VGAMMAN203)*(96R/120R)
VGAMMAN218	6R	VGAMMAN203+((VGAMMAN223-VGAMMAN203)*(90R/120R)
VGAMMAN217	6R	VGAMMAN203+((VGAMMAN223-VGAMMAN203)*(84R/120R)
VGAMMAN216	6R	VGAMMAN203+((VGAMMAN223-VGAMMAN203)*(78R/120R)
VGAMMAN215	6R	VGAMMAN203+((VGAMMAN223-VGAMMAN203)*(72R/120R)
VGAMMAN214	6R	VGAMMAN203+((VGAMMAN223-VGAMMAN203)*(66R/120R)
VGAMMAN213	6R	VGAMMAN203+((VGAMMAN223-VGAMMAN203)*(60R/120R)
VGAMMAN212	6R	VGAMMAN203+((VGAMMAN223-VGAMMAN203)*(54R/120R)
VGAMMAN211	6R	VGAMMAN203+((VGAMMAN223-VGAMMAN203)*(48R/120R)
VGAMMAN210	6R	VGAMMAN203+((VGAMMAN223-VGAMMAN203)*(42R/120R)
VGAMMAN209	6R	VGAMMAN203+((VGAMMAN223-VGAMMAN203)*(36R/120R)
VGAMMAN208	6R	VGAMMAN203+((VGAMMAN223-VGAMMAN203)*(30R/120R)
VGAMMAN207	6R	VGAMMAN203+((VGAMMAN223-VGAMMAN203)*(24R/120R)
VGAMMAN206	6R	VGAMMAN203+((VGAMMAN223-VGAMMAN203)*(18R/120R)
VGAMMAN205	6R	VGAMMAN203+((VGAMMAN223-VGAMMAN203)*(12R/120R)
VGAMMAN204	6R	VGAMMAN203+((VGAMMAN223-VGAMMAN203)*(6R/120R)
VGAMMAN203	3R	VGAMMAN8+(VGAMMAN247-VGAMMAN8)*((77R-0R)/90R) , VP203[4:0] =0 (Dec) VGAMMAN8+(VGAMMAN247-VGAMMAN8)*((77R-2R)/90R) , VP203[4:0] =1 (Dec) VGAMMAN8+(VGAMMAN247-VGAMMAN8)*((77R-4R)/90R) , VP203[4:0] =2 (Dec) VGAMMAN8+(VGAMMAN247-VGAMMAN8)*((74R-1R*VN203[4:0])/90R) , else
VGAMMAN202	3R	VGAMMAN175+((VGAMMAN203-VGAMMAN175)*(81R/84R)
VGAMMAN201	3R	VGAMMAN175+((VGAMMAN203-VGAMMAN175)*(78R/84R)
VGAMMAN200	3R	VGAMMAN175+((VGAMMAN203-VGAMMAN175)*(75R/84R)
VGAMMAN199	3R	VGAMMAN175+((VGAMMAN203-VGAMMAN175)*(72R/84R)
VGAMMAN198	3R	VGAMMAN175+((VGAMMAN203-VGAMMAN175)*(69R/84R)
VGAMMAN197	3R	VGAMMAN175+((VGAMMAN203-VGAMMAN175)*(66R/84R)
VGAMMAN196	3R	VGAMMAN175+((VGAMMAN203-VGAMMAN175)*(63R/84R)
VGAMMAN195	3R	VGAMMAN175+((VGAMMAN203-VGAMMAN175)*(60R/84R)
VGAMMAN194	3R	VGAMMAN175+((VGAMMAN203-VGAMMAN175)*(57R/84R)
VGAMMAN193	3R	VGAMMAN175+((VGAMMAN203-VGAMMAN175)*(54R/84R)
VGAMMAN192	3R	VGAMMAN175+((VGAMMAN203-VGAMMAN175)*(51R/84R)
VGAMMAN191	3R	VGAMMAN175+((VGAMMAN203-VGAMMAN175)*(48R/84R)
VGAMMAN190	3R	VGAMMAN175+((VGAMMAN203-VGAMMAN175)*(45R/84R)
VGAMMAN189	3R	VGAMMAN175+((VGAMMAN203-VGAMMAN175)*(42R/84R)
VGAMMAN188	3R	VGAMMAN175+((VGAMMAN203-VGAMMAN175)*(39R/84R)
VGAMMAN187	3R	VGAMMAN175+((VGAMMAN203-VGAMMAN175)*(36R/84R)

VGAMMAN186	3R	$VGAMMAN175 + ((VGAMMAN203 - VGAMMAN175) * (33R/84R))$
VGAMMAN185	3R	$VGAMMAN175 + ((VGAMMAN203 - VGAMMAN175) * (30R/84R))$
VGAMMAN184	3R	$VGAMMAN175 + ((VGAMMAN203 - VGAMMAN175) * (27R/84R))$
VGAMMAN183	3R	$VGAMMAN175 + ((VGAMMAN203 - VGAMMAN175) * (24R/84R))$
VGAMMAN182	3R	$VGAMMAN175 + ((VGAMMAN203 - VGAMMAN175) * (21R/84R))$
VGAMMAN181	3R	$VGAMMAN175 + ((VGAMMAN203 - VGAMMAN175) * (18R/84R))$
VGAMMAN180	3R	$VGAMMAN175 + ((VGAMMAN203 - VGAMMAN175) * (15R/84R))$
VGAMMAN179	3R	$VGAMMAN175 + ((VGAMMAN203 - VGAMMAN175) * (12R/84R))$
VGAMMAN178	3R	$VGAMMAN175 + ((VGAMMAN203 - VGAMMAN175) * (9R/84R))$
VGAMMAN177	3R	$VGAMMAN175 + ((VGAMMAN203 - VGAMMAN175) * (6R/84R))$
VGAMMAN176	3R	$VGAMMAN175 + ((VGAMMAN203 - VGAMMAN175) * (3R/84R))$
VGAMMAN175	3R	$VGAMMAN52 + (VGAMMAN203 - VGAMMAN52) * ((68R - 0R)/76R)$, VP175[3:0] =0 (Dec) $VGAMMAN52 + (VGAMMAN203 - VGAMMAN52) * ((68R - 2R)/76R)$, VP175[3:0] =1 (Dec) $VGAMMAN52 + (VGAMMAN203 - VGAMMAN52) * ((68R - 4R)/76R)$, VP175[3:0] =2 (Dec) $VGAMMAN52 + (VGAMMAN203 - VGAMMAN52) * ((65R - 1R * VN175[3:0])/76R)$, else
VGAMMAN174	3R	$VGAMMAN147 + ((VGAMMAN175 - VGAMMAN147) * (81R+/84R))$
VGAMMAN173	3R	$VGAMMAN147 + ((VGAMMAN175 - VGAMMAN147) * (78R/84R))$
VGAMMAN172	3R	$VGAMMAN147 + ((VGAMMAN175 - VGAMMAN147) * (75R/84R))$
VGAMMAN171	3R	$VGAMMAN147 + ((VGAMMAN175 - VGAMMAN147) * (72R/84R))$
VGAMMAN170	3R	$VGAMMAN147 + ((VGAMMAN175 - VGAMMAN147) * (69R/84R))$
VGAMMAN169	3R	$VGAMMAN147 + ((VGAMMAN175 - VGAMMAN147) * (66R/84R))$
VGAMMAN168	3R	$VGAMMAN147 + ((VGAMMAN175 - VGAMMAN147) * (63R/84R))$
VGAMMAN167	3R	$VGAMMAN147 + ((VGAMMAN175 - VGAMMAN147) * (60R/84R))$
VGAMMAN166	3R	$VGAMMAN147 + ((VGAMMAN175 - VGAMMAN147) * (57R/84R))$
VGAMMAN165	3R	$VGAMMAN147 + ((VGAMMAN175 - VGAMMAN147) * (54R/84R))$
VGAMMAN164	3R	$VGAMMAN147 + ((VGAMMAN175 - VGAMMAN147) * (51R/84R))$
VGAMMAN163	3R	$VGAMMAN147 + ((VGAMMAN175 - VGAMMAN147) * (48R/84R))$
VGAMMAN162	3R	$VGAMMAN147 + ((VGAMMAN175 - VGAMMAN147) * (45R/84R))$
VGAMMAN161	3R	$VGAMMAN147 + ((VGAMMAN175 - VGAMMAN147) * (42R/84R))$
VGAMMAN160	3R	$VGAMMAN147 + ((VGAMMAN175 - VGAMMAN147) * (39R/84R))$
VGAMMAN159	3R	$VGAMMAN147 + ((VGAMMAN175 - VGAMMAN147) * (36R/84R))$
VGAMMAN158	3R	$VGAMMAN147 + ((VGAMMAN175 - VGAMMAN147) * (33R/84R))$
VGAMMAN157	3R	$VGAMMAN147 + ((VGAMMAN175 - VGAMMAN147) * (30R/84R))$
VGAMMAN156	3R	$VGAMMAN147 + ((VGAMMAN175 - VGAMMAN147) * (27R/84R))$
VGAMMAN155	3R	$VGAMMAN147 + ((VGAMMAN175 - VGAMMAN147) * (24R/84R))$
VGAMMAN154	3R	$VGAMMAN147 + ((VGAMMAN175 - VGAMMAN147) * (21R/84R))$
VGAMMAN153	3R	$VGAMMAN147 + ((VGAMMAN175 - VGAMMAN147) * (18R/84R))$

VGAMMAN152	3R	$VGAMMAN147 + ((VGAMMAN175 - VGAMMAN147) * (15R/84R))$
VGAMMAN151	3R	$VGAMMAN147 + ((VGAMMAN175 - VGAMMAN147) * (12R/84R))$
VGAMMAN150	3R	$VGAMMAN147 + ((VGAMMAN175 - VGAMMAN147) * (9R/84R))$
VGAMMAN149	3R	$VGAMMAN147 + ((VGAMMAN175 - VGAMMAN147) * (6R/84R))$
VGAMMAN148	3R	$VGAMMAN147 + ((VGAMMAN175 - VGAMMAN147) * (3R/84R))$
VGAMMAN147	3R	$VGAMMAN52 + (VGAMMAN203 - VGAMMAN52) * ((52R - 0R)/76R)$, VP147[3:0] =0 (Dec) $VGAMMAN52 + (VGAMMAN203 - VGAMMAN52) * ((52R - 2R)/76R)$, VP147[3:0] =1 (Dec) $VGAMMAN52 + (VGAMMAN203 - VGAMMAN52) * ((52R - 4R)/76R)$, VP147[3:0] =2 (Dec) $VGAMMAN52 + (VGAMMAN203 - VGAMMAN52) * ((49R - 1R * VN147[3:0])/76R)$, else
VGAMMAN146	3R	$VGAMMAN108 + ((VGAMMAN147 - VGAMMAN108) * (114R/117R))$
VGAMMAN145	3R	$VGAMMAN108 + ((VGAMMAN147 - VGAMMAN108) * (111R/117R))$
VGAMMAN144	3R	$VGAMMAN108 + ((VGAMMAN147 - VGAMMAN108) * (108R/117R))$
VGAMMAN143	3R	$VGAMMAN108 + ((VGAMMAN147 - VGAMMAN108) * (105R/117R))$
VGAMMAN142	3R	$VGAMMAN108 + ((VGAMMAN147 - VGAMMAN108) * (102R/117R))$
VGAMMAN141	3R	$VGAMMAN108 + ((VGAMMAN147 - VGAMMAN108) * (99R/117R))$
VGAMMAN140	3R	$VGAMMAN108 + ((VGAMMAN147 - VGAMMAN108) * (96R/117R))$
VGAMMAN139	3R	$VGAMMAN108 + ((VGAMMAN147 - VGAMMAN108) * (93R/117R))$
VGAMMAN138	3R	$VGAMMAN108 + ((VGAMMAN147 - VGAMMAN108) * (90R/117R))$
VGAMMAN137	3R	$VGAMMAN108 + ((VGAMMAN147 - VGAMMAN108) * (87R/117R))$
VGAMMAN136	3R	$VGAMMAN108 + ((VGAMMAN147 - VGAMMAN108) * (84R/117R))$
VGAMMAN135	3R	$VGAMMAN108 + ((VGAMMAN147 - VGAMMAN108) * (81R/117R))$
VGAMMAN134	3R	$VGAMMAN108 + ((VGAMMAN147 - VGAMMAN108) * (78R/117R))$
VGAMMAN133	3R	$VGAMMAN108 + ((VGAMMAN147 - VGAMMAN108) * (75R/117R))$
VGAMMAN132	3R	$VGAMMAN108 + ((VGAMMAN147 - VGAMMAN108) * (72R/117R))$
VGAMMAN131	3R	$VGAMMAN108 + ((VGAMMAN147 - VGAMMAN108) * (69R/117R))$
VGAMMAN130	3R	$VGAMMAN108 + ((VGAMMAN147 - VGAMMAN108) * (66R/117R))$
VGAMMAN129	3R	$VGAMMAN108 + ((VGAMMAN147 - VGAMMAN108) * (63R/117R))$
VGAMMAN128	3R	$VGAMMAN108 + ((VGAMMAN147 - VGAMMAN108) * (60R/117R))$
VGAMMAN127	3R	$VGAMMAN108 + ((VGAMMAN147 - VGAMMAN108) * (57R/117R))$
VGAMMAN126	3R	$VGAMMAN108 + ((VGAMMAN147 - VGAMMAN108) * (54R/117R))$
VGAMMAN125	3R	$VGAMMAN108 + ((VGAMMAN147 - VGAMMAN108) * (51R/117R))$
VGAMMAN124	3R	$VGAMMAN108 + ((VGAMMAN147 - VGAMMAN108) * (48R/117R))$
VGAMMAN123	3R	$VGAMMAN108 + ((VGAMMAN147 - VGAMMAN108) * (45R/117R))$
VGAMMAN122	3R	$VGAMMAN108 + ((VGAMMAN147 - VGAMMAN108) * (42R/117R))$
VGAMMAN121	3R	$VGAMMAN108 + ((VGAMMAN147 - VGAMMAN108) * (39R/117R))$
VGAMMAN120	3R	$VGAMMAN108 + ((VGAMMAN147 - VGAMMAN108) * (36R/117R))$
VGAMMAN119	3R	$VGAMMAN108 + ((VGAMMAN147 - VGAMMAN108) * (33R/117R))$

VGAMMAN118	3R	$VGAMMAN108 + ((VGAMMAN147 - VGAMMAN108) * (30R/117R))$
VGAMMAN117	3R	$VGAMMAN108 + ((VGAMMAN147 - VGAMMAN108) * (27R/117R))$
VGAMMAN116	3R	$VGAMMAN108 + ((VGAMMAN147 - VGAMMAN108) * (24R/117R))$
VGAMMAN115	3R	$VGAMMAN108 + ((VGAMMAN147 - VGAMMAN108) * (21R/117R))$
VGAMMAN114	3R	$VGAMMAN108 + ((VGAMMAN147 - VGAMMAN108) * (18R/117R))$
VGAMMAN113	3R	$VGAMMAN108 + ((VGAMMAN147 - VGAMMAN108) * (15R/117R))$
VGAMMAN112	3R	$VGAMMAN108 + ((VGAMMAN147 - VGAMMAN108) * (12R/117R))$
VGAMMAN111	3R	$VGAMMAN108 + ((VGAMMAN147 - VGAMMAN108) * (9R/117R))$
VGAMMAN110	3R	$VGAMMAN108 + ((VGAMMAN147 - VGAMMAN108) * (6R/117R))$
VGAMMAN109	3R	$VGAMMAN108 + ((VGAMMAN147 - VGAMMAN108) * (3R/117R))$
VGAMMAN108	3R	$VGAMMAN52 + (VGAMMAN203 - VGAMMAN52) * ((17R + 1R * VN108[3:0]) / 76R)$, else $VGAMMAN52 + (VGAMMAN203 - VGAMMAN52) * ((17R + 31R) / 76R)$, VP108[3:0] =13 (Dec) $VGAMMAN52 + (VGAMMAN203 - VGAMMAN52) * ((17R + 33R) / 76R)$, VP108[3:0] =14 (Dec) $VGAMMAN52 + (VGAMMAN203 - VGAMMAN52) * ((17R + 35R) / 76R)$, VP108[3:0] =15 (Dec)
VGAMMAN107	3R	$VGAMMAN80 + ((VGAMMAN108 - VGAMMAN80) * (81R/84R))$
VGAMMAN106	3R	$VGAMMAN80 + ((VGAMMAN108 - VGAMMAN80) * (78R/84R))$
VGAMMAN105	3R	$VGAMMAN80 + ((VGAMMAN108 - VGAMMAN80) * (75R/84R))$
VGAMMAN104	3R	$VGAMMAN80 + ((VGAMMAN108 - VGAMMAN80) * (72R/84R))$
VGAMMAN103	3R	$VGAMMAN80 + ((VGAMMAN108 - VGAMMAN80) * (69R/84R))$
VGAMMAN102	3R	$VGAMMAN80 + ((VGAMMAN108 - VGAMMAN80) * (66R/84R))$
VGAMMAN101	3R	$VGAMMAN80 + ((VGAMMAN108 - VGAMMAN80) * (63R/84R))$
VGAMMAN100	3R	$VGAMMAN80 + ((VGAMMAN108 - VGAMMAN80) * (60R/84R))$
VGAMMAN99	3R	$VGAMMAN80 + ((VGAMMAN108 - VGAMMAN80) * (57R/84R))$
VGAMMAN98	3R	$VGAMMAN80 + ((VGAMMAN108 - VGAMMAN80) * (54R/84R))$
VGAMMAN97	3R	$VGAMMAN80 + ((VGAMMAN108 - VGAMMAN80) * (51R/84R))$
VGAMMAN96	3R	$VGAMMAN80 + ((VGAMMAN108 - VGAMMAN80) * (48R/84R))$
VGAMMAN95	3R	$VGAMMAN80 + ((VGAMMAN108 - VGAMMAN80) * (45R/84R))$
VGAMMAN94	3R	$VGAMMAN80 + ((VGAMMAN108 - VGAMMAN80) * (42R/84R))$
VGAMMAN93	3R	$VGAMMAN80 + ((VGAMMAN108 - VGAMMAN80) * (39R/84R))$
VGAMMAN92	3R	$VGAMMAN80 + ((VGAMMAN108 - VGAMMAN80) * (36R/84R))$
VGAMMAN91	3R	$VGAMMAN80 + ((VGAMMAN108 - VGAMMAN80) * (33R/84R))$
VGAMMAN90	3R	$VGAMMAN80 + ((VGAMMAN108 - VGAMMAN80) * (30R/84R))$
VGAMMAN89	3R	$VGAMMAN80 + ((VGAMMAN108 - VGAMMAN80) * (27R/84R))$
VGAMMAN88	3R	$VGAMMAN80 + ((VGAMMAN108 - VGAMMAN80) * (24R/84R))$
VGAMMAN87	3R	$VGAMMAN80 + ((VGAMMAN108 - VGAMMAN80) * (21R/84R))$
VGAMMAN86	3R	$VGAMMAN80 + ((VGAMMAN108 - VGAMMAN80) * (18R/84R))$
VGAMMAN85	3R	$VGAMMAN80 + ((VGAMMAN108 - VGAMMAN80) * (15R/84R))$

VGAMMAN84	3R	$VGAMMAN80 + ((VGAMMAN108 - VGAMMAN80) * (12R/84R))$
VGAMMAN83	3R	$VGAMMAN80 + ((VGAMMAN108 - VGAMMAN80) * (9R/84R))$
VGAMMAN82	3R	$VGAMMAN80 + ((VGAMMAN108 - VGAMMAN80) * (6R/84R))$
VGAMMAN81	3R	$VGAMMAN80 + ((VGAMMAN108 - VGAMMAN80) * (3R/84R))$
VGAMMAN80	3R	$VGAMMAN52 + (VGAMMAN203 - VGAMMAN52) * ((1R + 1R * VN80[3:0]) / 76R)$, else $VGAMMAN52 + (VGAMMAN203 - VGAMMAN52) * ((1R + 15R) / 76R)$, VP80[3:0] =13 (Dec) $VGAMMAN52 + (VGAMMAN203 - VGAMMAN52) * ((1R + 17R) / 76R)$, VP80[3:0] =14 (Dec) $VGAMMAN52 + (VGAMMAN203 - VGAMMAN52) * ((1R + 19R) / 76R)$, VP80[3:0] =15 (Dec)
VGAMMAN79	3R	$VGAMMAN52 + ((VGAMMAN80 - VGAMMAN52) * (81R/84R))$
VGAMMAN78	3R	$VGAMMAN52 + ((VGAMMAN80 - VGAMMAN52) * (78R/84R))$
VGAMMAN77	3R	$VGAMMAN52 + ((VGAMMAN80 - VGAMMAN52) * (75R/84R))$
VGAMMAN76	3R	$VGAMMAN52 + ((VGAMMAN80 - VGAMMAN52) * (72R/84R))$
VGAMMAN75	3R	$VGAMMAN52 + ((VGAMMAN80 - VGAMMAN52) * (69R/84R))$
VGAMMAN74	3R	$VGAMMAN52 + ((VGAMMAN80 - VGAMMAN52) * (66R/84R))$
VGAMMAN73	3R	$VGAMMAN52 + ((VGAMMAN80 - VGAMMAN52) * (63R/84R))$
VGAMMAN72	3R	$VGAMMAN52 + ((VGAMMAN80 - VGAMMAN52) * (60R/84R))$
VGAMMAN71	3R	$VGAMMAN52 + ((VGAMMAN80 - VGAMMAN52) * (57R/84R))$
VGAMMAN70	3R	$VGAMMAN52 + ((VGAMMAN80 - VGAMMAN52) * (54R/84R))$
VGAMMAN69	3R	$VGAMMAN52 + ((VGAMMAN80 - VGAMMAN52) * (51R/84R))$
VGAMMAN68	3R	$VGAMMAN52 + ((VGAMMAN80 - VGAMMAN52) * (48R/84R))$
VGAMMAN67	3R	$VGAMMAN52 + ((VGAMMAN80 - VGAMMAN52) * (45R/84R))$
VGAMMAN66	3R	$VGAMMAN52 + ((VGAMMAN80 - VGAMMAN52) * (42R/84R))$
VGAMMAN65	3R	$VGAMMAN52 + ((VGAMMAN80 - VGAMMAN52) * (39R/84R))$
VGAMMAN64	3R	$VGAMMAN52 + ((VGAMMAN80 - VGAMMAN52) * (36R/84R))$
VGAMMAN63	3R	$VGAMMAN52 + ((VGAMMAN80 - VGAMMAN52) * (33R/84R))$
VGAMMAN62	3R	$VGAMMAN52 + ((VGAMMAN80 - VGAMMAN52) * (30R/84R))$
VGAMMAN61	3R	$VGAMMAN52 + ((VGAMMAN80 - VGAMMAN52) * (27R/84R))$
VGAMMAN60	3R	$VGAMMAN52 + ((VGAMMAN80 - VGAMMAN52) * (24R/84R))$
VGAMMAN59	3R	$VGAMMAN52 + ((VGAMMAN80 - VGAMMAN52) * (21R/84R))$
VGAMMAN58	3R	$VGAMMAN52 + ((VGAMMAN80 - VGAMMAN52) * (18R/84R))$
VGAMMAN57	3R	$VGAMMAN52 + ((VGAMMAN80 - VGAMMAN52) * (15R/84R))$
VGAMMAN56	3R	$VGAMMAN52 + ((VGAMMAN80 - VGAMMAN52) * (12R/84R))$
VGAMMAN55	3R	$VGAMMAN52 + ((VGAMMAN80 - VGAMMAN52) * (9R/84R))$
VGAMMAN54	3R	$VGAMMAN52 + ((VGAMMAN80 - VGAMMAN52) * (6R/84R))$
VGAMMAN53	3R	$VGAMMAN52 + ((VGAMMAN80 - VGAMMAN52) * (3R/84R))$
VGAMMAN52	6R	$VGAMMAN8 + (VGAMMAN247 - VGAMMAN8) * ((8R + 1R * VN52[4:0]) / 90R)$, else $VGAMMAN8 + (VGAMMAN247 - VGAMMAN8) * ((8R + 38R) / 90R)$, VP52[4:0] =29 (Dec)

		$VGAMMAN8 + (VGAMMAN247 - VGAMMAN8) * ((8R + 40R) / 90R)$, VP52[4:0] =30 (Dec) $VGAMMAN8 + (VGAMMAN247 - VGAMMAN8) * ((8R + 42R) / 90R)$, VP52[4:0] =31 (Dec)
VGAMMAN51	6R	$VGAMMAN32 + (VGAMMAN52 - VGAMMAN32) * (114R / 120R)$
VGAMMAN50	6R	$VGAMMAN32 + (VGAMMAN52 - VGAMMAN32) * (108R / 120R)$
VGAMMAN49	6R	$VGAMMAN32 + (VGAMMAN52 - VGAMMAN32) * (102R / 120R)$
VGAMMAN48	6R	$VGAMMAN32 + (VGAMMAN52 - VGAMMAN32) * (96R / 120R)$
VGAMMAN47	6R	$VGAMMAN32 + (VGAMMAN52 - VGAMMAN32) * (90R / 120R)$
VGAMMAN46	6R	$VGAMMAN32 + (VGAMMAN52 - VGAMMAN32) * (84R / 120R)$
VGAMMAN45	6R	$VGAMMAN32 + (VGAMMAN52 - VGAMMAN32) * (78R / 120R)$
VGAMMAN44	6R	$VGAMMAN32 + (VGAMMAN52 - VGAMMAN32) * (72R / 120R)$
VGAMMAN43	6R	$VGAMMAN32 + (VGAMMAN52 - VGAMMAN32) * (66R / 120R)$
VGAMMAN42	6R	$VGAMMAN32 + (VGAMMAN52 - VGAMMAN32) * (60R / 120R)$
VGAMMAN41	6R	$VGAMMAN32 + (VGAMMAN52 - VGAMMAN32) * (54R / 120R)$
VGAMMAN40	6R	$VGAMMAN32 + (VGAMMAN52 - VGAMMAN32) * (48R / 120R)$
VGAMMAN39	6R	$VGAMMAN32 + (VGAMMAN52 - VGAMMAN32) * (42R / 120R)$
VGAMMAN38	6R	$VGAMMAN32 + (VGAMMAN52 - VGAMMAN32) * (36R / 120R)$
VGAMMAN37	6R	$VGAMMAN32 + (VGAMMAN52 - VGAMMAN32) * (30R / 120R)$
VGAMMAN36	6R	$VGAMMAN32 + (VGAMMAN52 - VGAMMAN32) * (24R / 120R)$
VGAMMAN35	6R	$VGAMMAN32 + (VGAMMAN52 - VGAMMAN32) * (18R / 120R)$
VGAMMAN34	6R	$VGAMMAN32 + (VGAMMAN52 - VGAMMAN32) * (12R / 120R)$
VGAMMAN33	6R	$VGAMMAN32 + (VGAMMAN52 - VGAMMAN32) * (6R / 120R)$
VGAMMAN32	6R	$VGAMMAN8 + (VGAMMAN52 - VGAMMAN8) * ((19R + 1R * VN32[4:0]) / 51R)$
VGAMMAN31	6R	$VGAMMAN16 + (VGAMMAN32 - VGAMMAN16) * (90R / 96R)$
VGAMMAN30	6R	$VGAMMAN16 + (VGAMMAN32 - VGAMMAN16) * (84R / 96R)$
VGAMMAN29	6R	$VGAMMAN16 + (VGAMMAN32 - VGAMMAN16) * (78R / 96R)$
VGAMMAN28	6R	$VGAMMAN16 + (VGAMMAN32 - VGAMMAN16) * (72R / 96R)$
VGAMMAN27	6R	$VGAMMAN16 + (VGAMMAN32 - VGAMMAN16) * (66R / 96R)$
VGAMMAN26	6R	$VGAMMAN16 + (VGAMMAN32 - VGAMMAN16) * (60R / 96R)$
VGAMMAN25	6R	$VGAMMAN16 + (VGAMMAN32 - VGAMMAN16) * (54R / 96R)$
VGAMMAN24	6R	$VGAMMAN16 + (VGAMMAN32 - VGAMMAN16) * (48R / 96R)$
VGAMMAN23	6R	$VGAMMAN16 + (VGAMMAN32 - VGAMMAN16) * (42R / 96R)$
VGAMMAN22	6R	$VGAMMAN16 + (VGAMMAN32 - VGAMMAN16) * (36R / 96R)$
VGAMMAN21	6R	$VGAMMAN16 + (VGAMMAN32 - VGAMMAN16) * (30R / 96R)$
VGAMMAN20	6R	$VGAMMAN16 + (VGAMMAN32 - VGAMMAN16) * (24R / 96R)$
VGAMMAN19	6R	$VGAMMAN16 + (VGAMMAN32 - VGAMMAN16) * (18R / 96R)$
VGAMMAN18	6R	$VGAMMAN16 + (VGAMMAN32 - VGAMMAN16) * (12R / 96R)$
VGAMMAN17	6R	$VGAMMAN16 + (VGAMMAN32 - VGAMMAN16) * (6R / 96R)$

VGAMMAN16	15R	$VGAMMAN8 + (VGAMMAN52 - VGAMMAN8) * ((1R + 1R * VN16[4:0]) / 51R)$
VGAMMAN15	15R	$VGAMMAN8 + ((VGAMMAN16 - VGAMMAN8) * (105R / 120R))$
VGAMMAN14	15R	$VGAMMAN8 + ((VGAMMAN16 - VGAMMAN8) * (90R / 120R))$
VGAMMAN13	15R	$VGAMMAN8 + ((VGAMMAN16 - VGAMMAN8) * (75R / 120R))$
VGAMMAN12	15R	$VGAMMAN8 + ((VGAMMAN16 - VGAMMAN8) * (60R / 120R))$
VGAMMAN11	15R	$VGAMMAN8 + ((VGAMMAN16 - VGAMMAN8) * (45R / 120R))$
VGAMMAN10	15R	$VGAMMAN8 + ((VGAMMAN16 - VGAMMAN8) * (30R / 120R))$
VGAMMAN9	15R	$VGAMMAN8 + ((VGAMMAN16 - VGAMMAN8) * (15R / 120R))$
VGAMMAN8	30R	$VGMN + \Delta VDHN(3R * VN8[5:0]) / 322R, \Delta VDHN = (VGSN - VGMN)$
VGAMMAN7	30R	$VGAMMAN4 + ((VGAMMAN8 - VGAMMAN4) * (90R / 120R))$
VGAMMAN6	30R	$VGAMMAN4 + ((VGAMMAN8 - VGAMMAN4) * (60R / 120R))$
VGAMMAN5	30R	$VGAMMAN4 + ((VGAMMAN8 - VGAMMAN4) * (30R / 120R))$
VGAMMAN4	6R	$VGMN + \Delta VDHN(3R * VN4[5:0]) / 322R, \Delta VDHN = (VGSN - VGMN)$
VGAMMAN3	12R	$VGAMMAN0 + (VGAMMAN4 - VGAMMAN0) * (RCGNH + 6R + 12R) / (42R + RCGNH)$
VGAMMAN2	24R	$VGAMMAN0 + (VGAMMAN4 - VGAMMAN0) * (RCGNH + 6R) / (42R + RCGNH)$
VGAMMAN1	24R	$VGAMMAN0 + (VGAMMAN4 - VGAMMAN0) * RCGNH / (42R + RCGNH)$
VGAMMAN0		$VGMN + \Delta VDHN(3R * VN0[5:0]) / 322R, \Delta VDHN = (VGSN - VGMN)$

18. Deep Standby Mode Setting

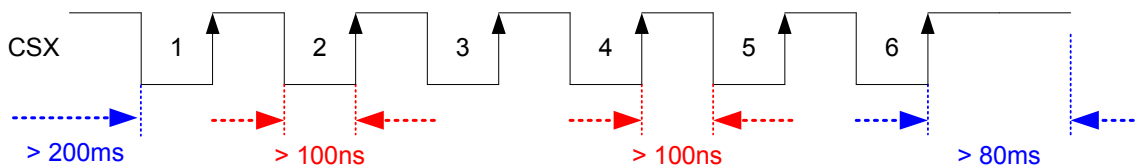
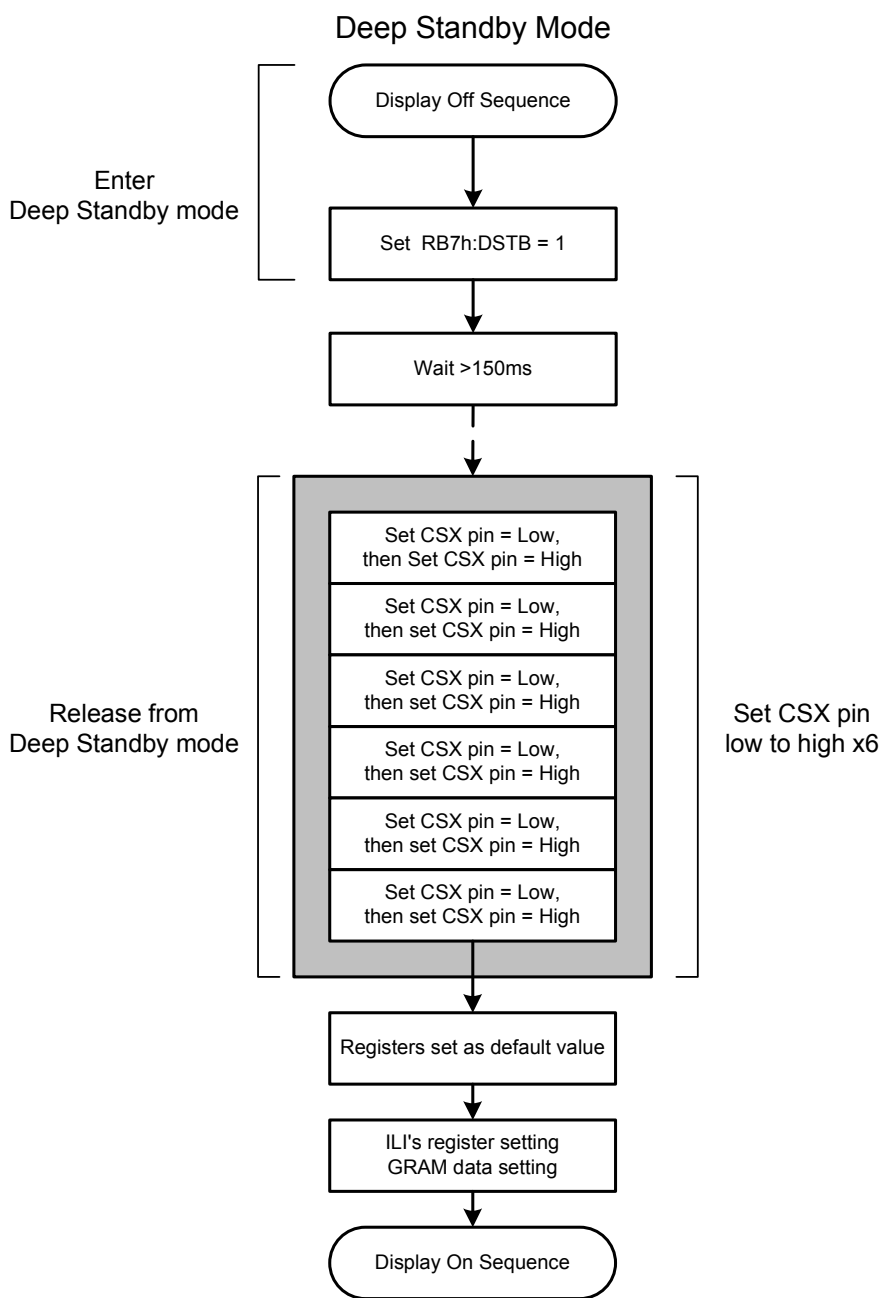


Figure 185: Deep Standby Mode Entry/Exit

19. Electrical Characteristics

19.1. Absolute Maximum Ratings

The absolute maximum rating is listed in Table 49. When the ILI9806G is used beyond the absolute maximum ratings, it may be permanently damaged. It is strongly recommended that use the ILI9806G within the following electrical characteristics limit for normal operation. If these electrical characteristic conditions are exceeded during normal operation, the ILI9806G will malfunction and cause poor reliability.

Table 49: Absolute Maximum Ratings

Item	Symbol	Unit	Value
Supply voltage(Analog)	VDDA ~ VSSA	V	-0.3 ~ +4.6
Supply voltage (I/O)	VDDI ~ VSSI	V	-0.3 ~ +4.6
Supply voltage (DSI I/O)	VDDAM ~ VSSAM	V	-0.3 ~ +4.6
OTP Supply voltage	VPP ~ VSSA	V	7.5
Supply voltage	AVDD ~ DSSA	V	-0.3 ~ +6.6
Supply voltage	AVEE ~ DSSA	V	0.3 ~ -6.6
Supply voltage	VGH ~ DSSA	V	-0.3 ~ +25
Supply voltage	VGL ~ DSSA	V	0.3 ~ -16
Driver supply voltage	VDDA – VCL	V	≤ 6.0V
Driver supply voltage	VGH-VGL	V	≤ 32.0V
Input voltage	V _{IN}	V	-0.3 ~ VDDI + 0.3
HS Input voltage	V _{HSIN}	V	-0.3 ~ + 2
Operating temperature	T _{opr}	°C	-30 ~ +70
Storage temperature	T _{stg}	°C	-55 ~ +110
<p>Note:</p> <p>Even if the absolute maximum rating of one of the above parameters is exceeded only for a short while, the quality of the product may be degraded. Therefore, be sure to use the product within the range of the absolute maximum ratings.</p>			

19.2. DC Characteristics for Panel Driving

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Power & Operation Voltage							
Analog operating voltage	VDDA	-	2.5	2.8	3.3	V	
Logic operating voltage	VDDAM	-	2.5	2.8	3.3	V	
Logic operating voltage	VDDI	-	1.65	1.8	3.3	V	Note1,2
OTP Supply voltage	VPP	-		7.5		V	Note1
Logic High level input voltage	V _{IH}	-	0.7*VDDI		VDDI	V	Note1
Logic Low level input voltage	V _{IL}	-	-0.3		0.3*VDDI	V	Note1
Logic High level output voltage TE, SDO (SDA) , LEDPWM	V _{OH}	I _{OH} = -1.0mA	0.8*VDDI		VDDI	V	Note1
Logic Low level output voltage TE, SDO (SDA) , LEDPWM	V _{OL}	I _{OL} = +1.0mA	0		0.2*VDDI	V	Note1
Gate Driver High Voltage	VGH	-	12.0	-	20	V	
Gate Driver Low Voltage	VGL	-	-15.0	-	-7.0	V	
Driver Supply Voltage	-	VGH-VGL	19	-	32	V	
VCOM Operation							
DC VCOM Amplitude Voltage	VCOM	-	-3.0	-	0	V	Note3
Source Driver							
Source Output Range	V _{SOUT}	-	0.1	-	VGMP-0.1	V	Note4
Positive Gamma Reference Voltage	VGMP	-	3.0	-	6.1875	V	
Negative Gamma Reference Voltage	VGMN	-	-6.1875	-	-3.0	V	
Source Output Setting Time	T _r	Below with 99% precision	-	15	20	us	Note3.4
Output Deviation Voltage (Source Output channel)	V _{dev}	S _{out} ≥ 4.2V	-	-	20	mV	Note3
		4.2V > S _{out} > 0.8V	-	-	15	mV	-
Output Offset Voltage	V _{OFFSET}	-	-	-	35	mV	Note3
Booster Operation							
Booster (VDDbX2.5) Voltage	AVDD	-			6.5	V	
Booster (VDDbX-2.5) Voltage	AVEE	-	-6.5			V	
Booster (VDDbX2 Drop Voltage)	VDDbX2 drop	loading=1mA	-	-	5	%	
Gate Driver High Voltage	VGH	-	10.0	-	20	V	
Gate Driver Low Voltage	VGL	-	-15.0	-	-6.0	V	

Notes:

1. Ta = -30 to 70 °C (no damage up to 85 °C), VDDI=1.65V to 3.3V, VDDA=2.5V to 3.3V, VSSAM=GND =0V.
2. Supply the digital VDDI voltage equal to or less than the analog VDDA voltage.
3. Source channel loading = 10pF/channel, Gate channel loading = 50pF/channel
4. The Max. Value is between with Note 3 measure point and the Gamma setting value

19.3. DSI DC Characteristics

The DSI uses different state codes which depend on DC voltage levels of the clock and data lanes. The meaning of the state codes is defined on the following table.

State Code	Line DC Voltage Levels	
	CLOCK_P or DATA_P	CLOCK_N or DATA_N
HS-0	Low (HS)	High (HS)
HS-1	High (HS)	Low (HS)
LP-00	Low (LP)	Low (LP)
LP-01	Low (LP)	High (LP)
LP-10	High (LP)	Low (LP)
LP-11	High (LP)	Low (LP)

Note: Ta = -30°C to 70°C (no damage up to 85°C)

19.3.1. DC characteristics for Power Lines

Parameter	Symbol	Condition	Specification			Unit
			Min.	Typ.	Max.	
Analog power supply voltage	VDDA	Operating voltage	2.5	2.8	3.3	V
Digital power supply voltage	VDDI	I/O supply voltage	1.65	1.8	3.3	V
Analog power supply voltage noise	VVDDA_NOISE	Noise Range, 0 to 100MHz, Sinusoidal Wave (peak-to-peak)	-	-	100	mV
		Noise Range, 0 to 30kHz, Pulse Wave with Duty Cycle (50%/50%)	-	-	500	mV
I/O power supply voltage noise	VVDDI_NOISE	Noise Range, 0 to 100MHz, Sinusoidal Wave (peak-to-peak)	-	-	100	mV

Notes:

1. Ta = -30°C to 70°C (no damage up to 85°C)
2. These values are not symmetric amplitude, which center points are VDDI or VDDA. See examples, when VVDDA_NOISE and VVDDI_NOISE are maximums, below for reference.

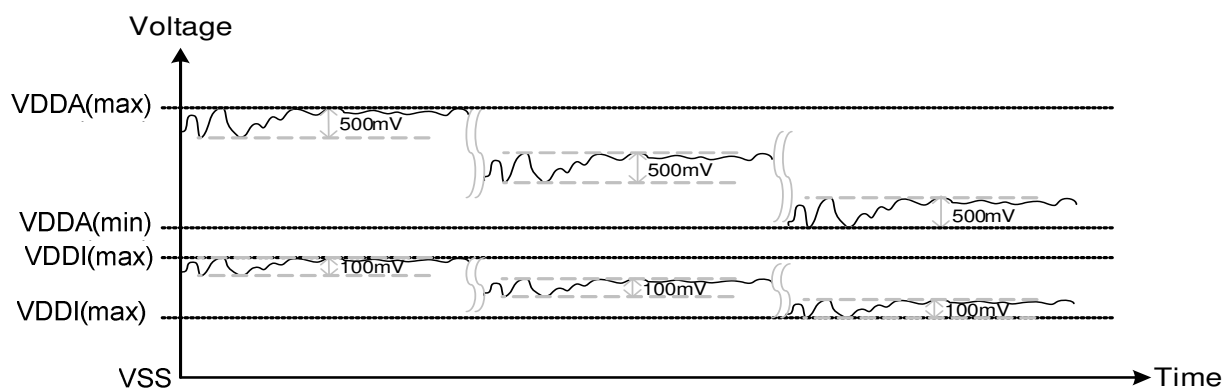


Figure 186: Noise on Power Supply Lines

19.3.2. DC Characteristics for DSI LP Mode

DC levels of the LP-00, LP-01, LP-10, and LP-11 are defined in the table below: DC Characteristics for DSI LP mode when LP-RX, LP-CD, or LP-TX is mentioned in the condition column. Other logical levels of the table are for the MPU interface.

Parameter	Symbol	Condition	Specification			Unit
			Min.	Typ.	Max.	
Logic High level output voltage	V_{OH}	$I_{OUT} = -1\text{mA}$, Note 2	$0.8 V_{DDAM}$	-	V_{DDAM}	V
Logic Low level output voltage	V_{OL}	$I_{OUT} = 1\text{Ma}$, Note 2	0.0	-	$0.2V_{DDAM}$	V
Logic High level input voltage	V_{IHLPCD}	LP-CD, Note 3	450	-	1350	mV
Logic Low level input voltage	V_{ILLPCD}	LP-CD, Note 3	0.0	-	200	mV
Logic High level input voltage	V_{IHLPRX}	LP-RX (CLK, D0 ,D1), Note 3	880	-	1350	mV
Logic Low level input voltage	V_{ILLPRX}	LP-RX (CLK, D0 ,D1), Note 3	0.0	-	550	mV
Logic Low level input voltage	$V_{ILLPRXULP}$	LP-RX (CLK ULP mode), Note 3	0.0	-	300	mV
Logic high level output voltage	V_{OHLPTX}	LP-TX (D0), Note 3	1.1	-	1.3	V
Logic Low level output voltage	V_{OLLPTX}	LP-TX (D0), Note 3	-50	-	50	mV
Logic High level input current	I_{IH}	LP-CD, LP-RX, Note 3	-	-	10	uA
Logic Low level input current	I_{IL}	LP-CD, LP-RX, Note 3	-10	-	-	uA

Notes:

1. $T_a = -30^{\circ}\text{C}$ to 70°C (no damage up to 85°C)
2. LEDPWM, TE_ENABLE
3. The DSI High Speed mode is Off.

19.3.3. Spike/Glitch Rejection

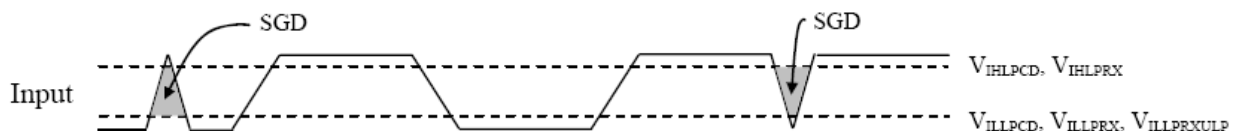


Figure 187: Spike/Glitch Rejection

Notes:

1. A spike/glitch can be rejected when the Peak Interference Amplitude is 200mV (at maximum) and the Interference Frequency is 450 MHz (at the very least).
2. $n = 0$ and 1.

Table 50: Spike/Glitch Rejection

Spike/Glitch Rejection – DSI					
Signal	Symbol	Parameter	Min	Max	Unit
DSI-CLK+/-, DSI-Dn+/-	SGD	Input pulse rejection for DSI	-	300	Vps

19.3.4. DC Characteristics for DSI HS Mode

Parameter	Symbol	Condition	Specification			Unit
Input Common Mode Voltage for Clock	V_{CMCLK}	DSI-CLK+/- Note 2, Note 3	70	-	330	mV
Input Common Mode Voltage for Data	V_{CMDATA}	DSI-Dn+/- Note 2, Note 3, Note 5	70	-	330	mV
Common Mode Ripple for Clock Equal or Less than 450MHz	$V_{CMRCLKL450}$	DSI-CLK+/- Note 4	-50	-	50	mV
Common Mode Ripple for Data Equal or Less than 450MHz	$V_{CMRDATAL450}$	DSI-Dn+/- Note 4, Note 5	-50	-	50	mV
Common Mode Ripple for Clock More than 450MHz (peak sine wave)	$V_{CMRCLKM450}$	DSI-CLK+/-	-	-	100	mV
Common Mode Ripple for Data More than 450MHz (peak sine wave)	$V_{CMRDATAM450}$	DSI-Dn+/- Note 5	-	-	100	mV
Differential Input Low Level Threshold Voltage for Clock	$V_{THLCLK-}$	DSI-CLK+/-	-70	-	-	mV
Differential Input Low Level Threshold Voltage for Data	$V_{THLDATA-}$	DSI-Dn+/- Note 5	-70	-	-	mV
Differential Input High Level Threshold Voltage for Clock	$V_{THHCLK+}$	DSI-CLK+/-	-	-	70	mV
Differential Input High Level Threshold Voltage for Data	$V_{THHDATA+}$	DSI-Dn+/- Note 5	-	-	70	mV
Single-ended Input Low Voltage	V_{ILHS}	DSI-CLK+/-, DSI-Dn+/- Note 3, Note 5	-40	-	-	mV
Single-ended Input High Voltage	V_{IHHS}	DSI-CLK+/-, DSI-Dn+/- Note 3, Note 5	-	-	460	mV
Differential Termination Resistor	R_{TERM}	DSI-CLK+/-, DSI-Dn+/- Note 5	80	100	125	Ω
Single-ended Threshold Voltage for Termination Enable	$V_{TERM-EN}$	DSI-CLK+/-, DSI-Dn+/- Note 5	-	-	450	mV
Termination Capacitor	C_{TERM}	DSI-CLK+/-, DSI-Dn+/- Note 5, Note 6	-	-	60	pF

Notes:

1. $T_a = -30^{\circ}\text{C}$ to 70°C (no damage up to 85°C), $V_{DDI} = 1.65$ to 1.95V , $\text{GND} = 0\text{V}$.
2. Includes 50mV (-50mV to 50mV) ground difference
3. Without $V_{CMRCLKM450}/V_{CMRDATAM450}$
4. Without 50mV (-50mV to 50mV) ground difference
5. $n = 0$ or 1
6. For higher bit rates, a 14pF capacitor will be needed to meet the common-mode return loss specification.

The DSI receiver (HS mode) is understanding that there is logical '1' (HS-1) when a differential voltage is more than V_{THH} (CLK+/DATA+) and the DSI receiver (HS mode) is understanding that there is logical '0' (HS-0) when a differential voltage is more than V_{THL} (CLK-/DATA-). There is undefined state if the differential voltage is less than V_{THH} (CLK+/DATA+) and less than V_{THL} (CLK-/DATA-). A reference figure is below.

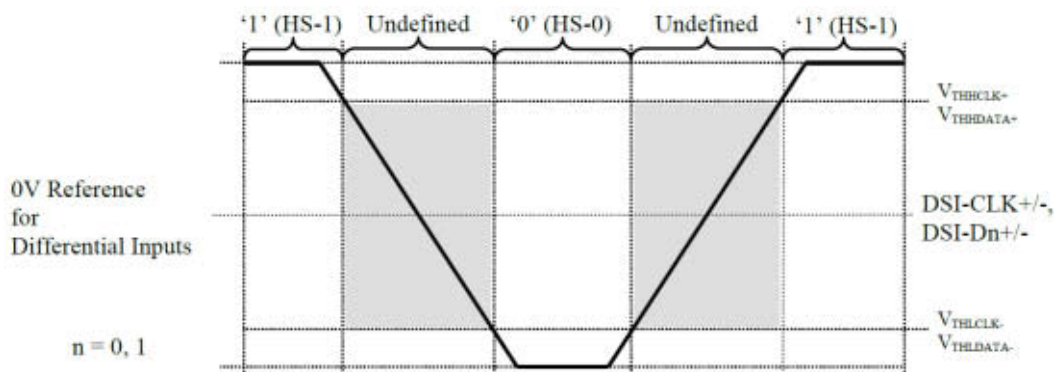
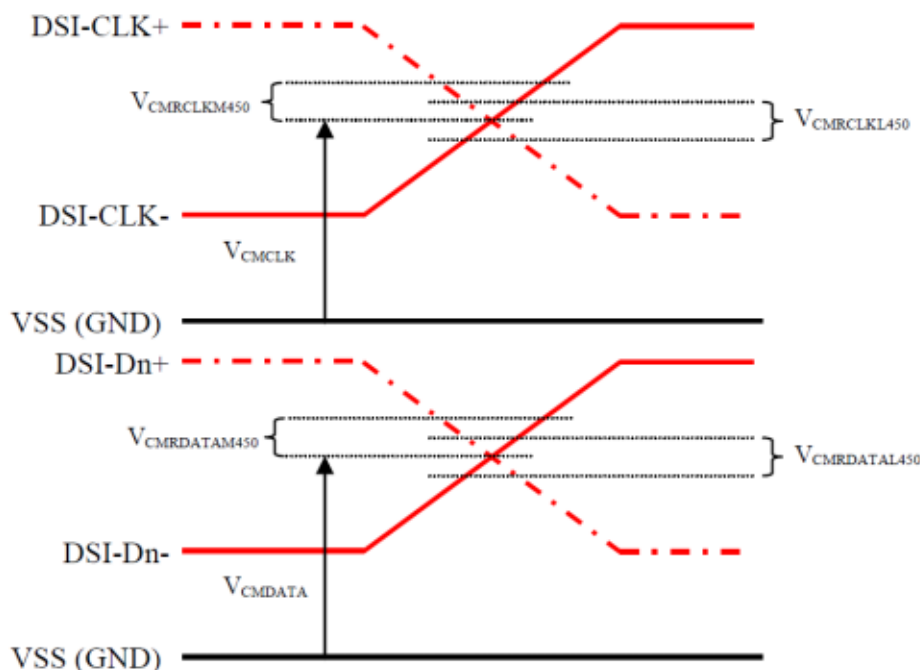


Figure 188: Differential Inputs Logical 0 and 1, Threshold High/Low, Differential Voltage Range



Note: $n = 0$ or 1

Figure 189: Common Mode Voltage on Clock and Data Channels

The termination resistor (R_{TERM}) of the differential DSI receiver can be driven to two different states by the receiver:

- Low Power (LP) mode when the termination resistor is not connected between differential inputs (DSI-CLK+ \Leftrightarrow DSI-CLK- or DSI-D0+ \Leftrightarrow DSI-D0- or DSI-D1+ \Leftrightarrow DSI-D1-)
- High Speed (HS) mode when the termination resistor is connected between differential inputs (DSI-CLK+ \Leftrightarrow DSI-CLK- or DSI-D0+ \Leftrightarrow DSI-D0- or DSI-D1+ \Leftrightarrow DSI-D1-)

The termination switch (HS/LP), when the termination resistor is not connected, is illustrated below.

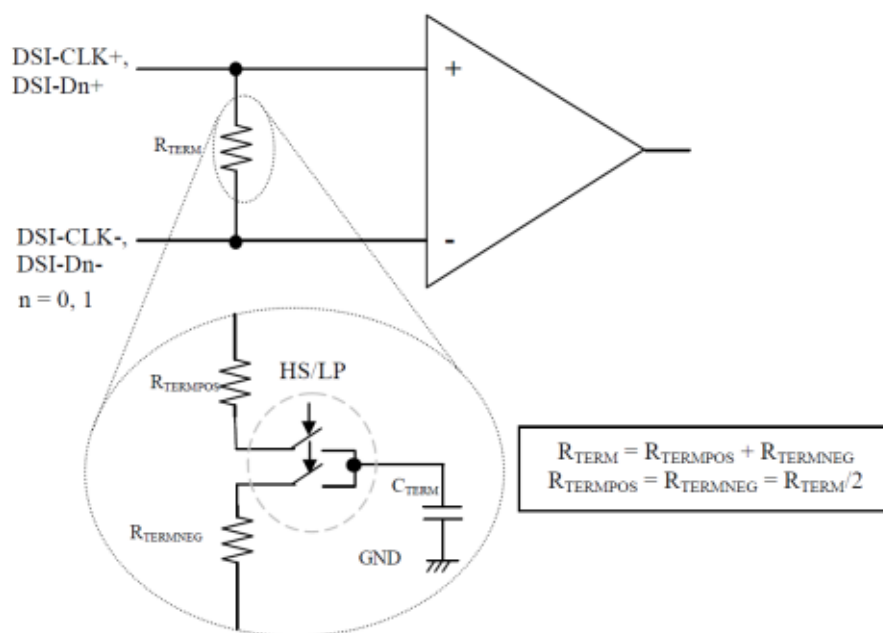


Figure 190: Differential Pair Termination Resistor on the Receiver Side

19.3.5. DC Characteristics for MDDI

Client Receiver Electrical Specifications

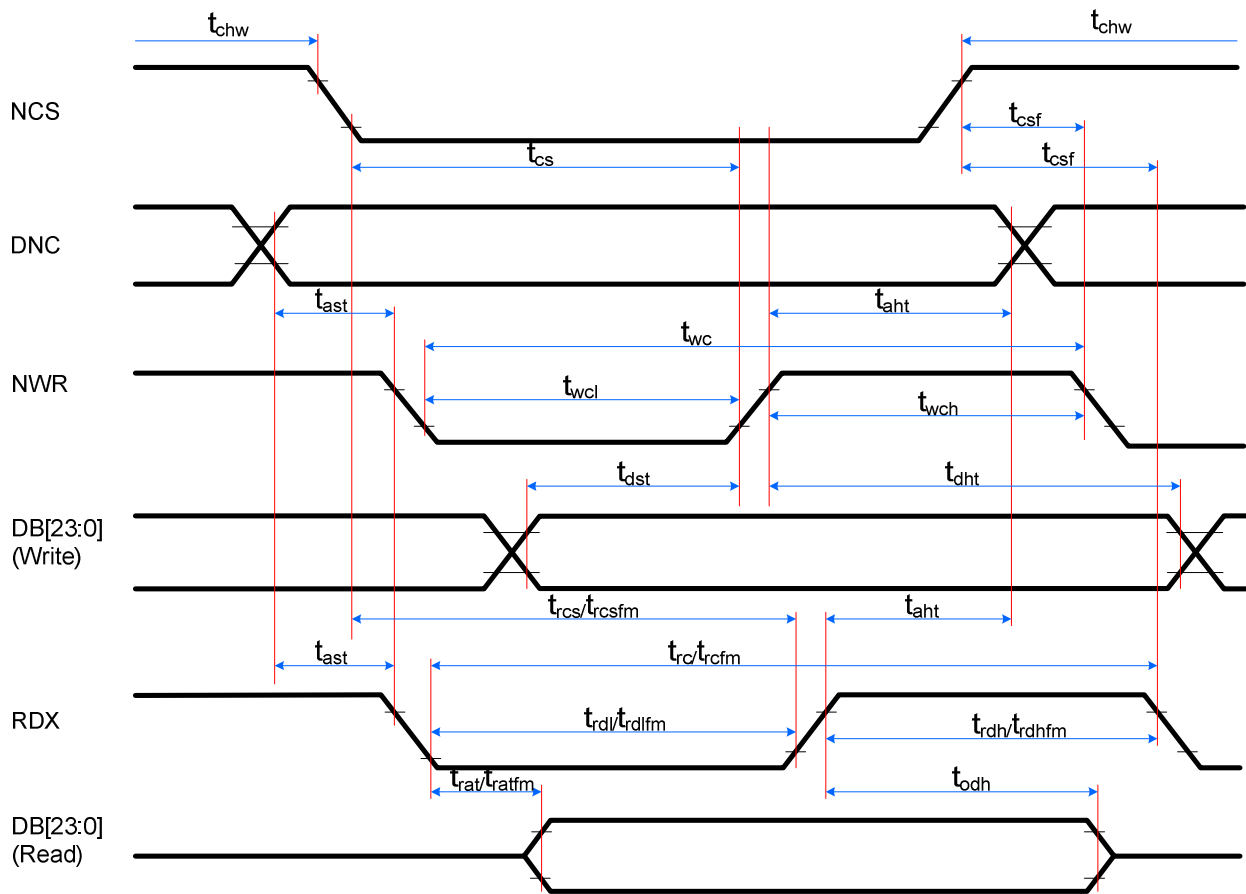
Parameter	Description	Min	Typ	Max	Unit
V _{IT+}	Receiver differential input high threshold voltage. Above this differential voltage the input signal must be interpreted as a logic-one level.		0	50	mV
V _{IT-}	Receiver differential input low threshold voltage. Below this differential voltage the input signal must be interpreted as a logic-zero level.	-50	0		mV
V _{IT+}	Receiver differential input high threshold voltage (offset for hibernation wake-up). Above this differential voltage the input signal must be interpreted as a logic-one level.		100	125	mV
V _{IT-}	Receiver differential input low threshold voltage (offset for hibernation wake-up). Below this differential voltage the input signal must be interpreted as a logic-zero level.	75	100		mV
V _{Input-Range}	Allowable receiver input voltage range with respect to client ground.	0.5		1.2	V
R _{term}	Parallel termination resistance value	98	100	102	Ω

MDDI V1.2 Client Transmitter Electrical Specifications

Parameter	Description	Min	Typ	Max	Unit
V _{output-Range-In}	Allowable client driver output voltage range with respect to client ground.	0.6		1.1	V
I _{OD+}	Driver differential output high current corresponding to a logic-one level (while driving the equivalent of the pull-up and pull-down circuits that exist at the host and client)	1.5		2.5	mA
I _{OD-}	Driver differential output low current corresponding to a logic-zero level (while driving the equivalent of the pull-up and pull-down circuits that exist at the host and client)	-2.5		-1.5	mA

AC Characteristics

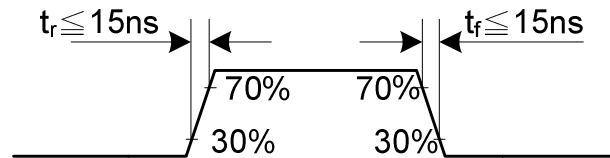
19.3.6. Display Parallel 24/18/16/9/8-bit Interface Timing Characteristics (8080-series)



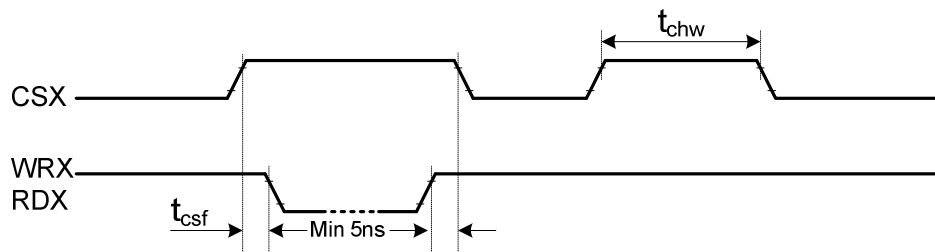
Signal	Symbol	Parameter	min	max	Unit	Description
DCX	tast	Address setup time	0	-	ns	-
	taht	Address hold time (Write/Read)	10	-	ns	-
CSX	tchw	CSX "H" pulse width	0	-	ns	-
	tcs	Chip Select setup time (Write)	10	-	ns	-
	trcs	Chip Select setup time (Read ID)	45	-	ns	-
	trcsfm	Chip Select setup time (Read FM)	355	-	ns	-
	tcsf	Chip Select Wait time (Write/Read)	10	-	ns	-
WRX	twc	Write cycle	30	-	ns	-
	twrh	Write Control pulse H duration	10	-	ns	-
	twrl	Write Control pulse L duration	10	-	ns	-
RDX (FM)	trcfm	Read Cycle (FM)	450	-	ns	When read from the Frame Memory
	trdhfm	Read Control H duration (FM)	90	-	ns	
	trdlfm	Read Control L duration (FM)	355	-	ns	
RDX (ID)	trc	Read cycle (ID)	160	-	ns	When read ID data
	trdh	Read Control pulse H duration	90	-	ns	
	trdl	Read Control pulse L duration	45	-	ns	
DB[17:0], DB[15:0], DB[8:0] DB[7:0]	tdst	Write data setup time	10	-	ns	CL = 30pF (maximum) CL = 8pF (minimum)
	tdht	Write data hold time	10	-	ns	
	trat	Read access time	-	40	ns	
	tratfm	Read access time	-	340	ns	
	trodh	Read output disable time	20	80	ns	

Notes:

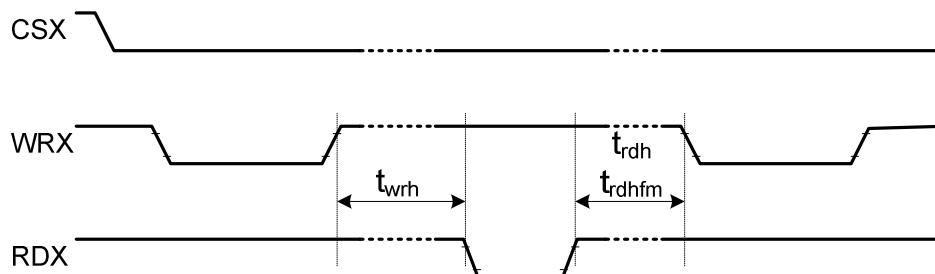
1. $T_a = -30$ to 70°C , $V_{DDI} = 1.65\text{V}$ to 3.3V , $V_{DDA} = 2.6\text{V}$ to 4.8V , $V_{SSAM} = \text{GND} = 0\text{V}$
2. Logic high and low levels are specified as 30% and 70% of V_{DDI} for input signals.
3. Input signal rising and falling time:



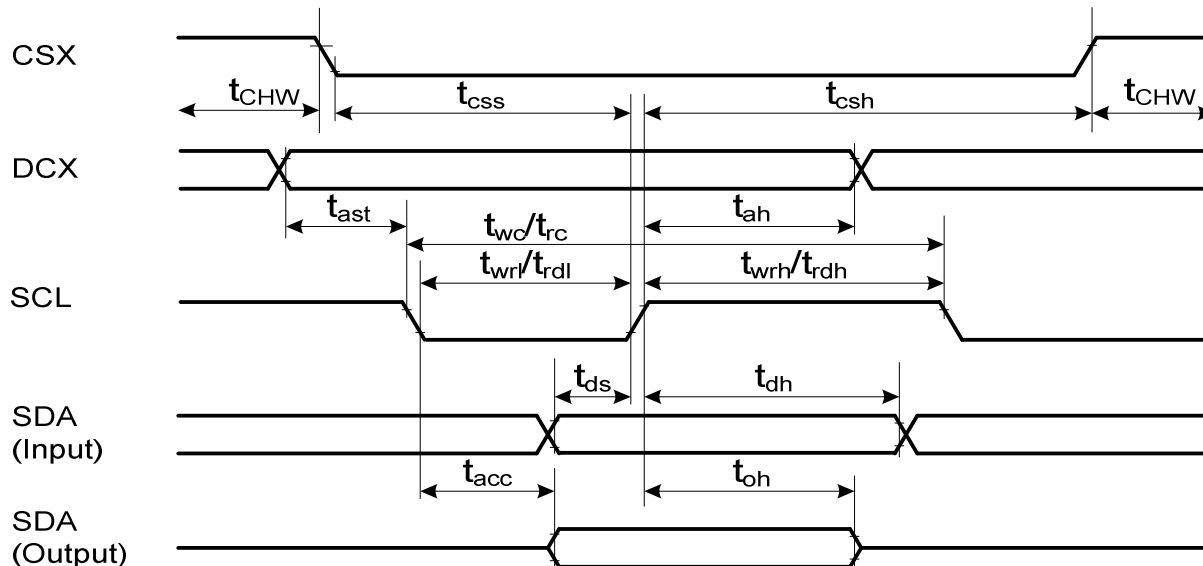
4. The CSX timing:



5. The Write-to-Read or the Read-to-Write timing:



19.3.7. Display Serial Interface Timing Characteristics (3-line SPI system)

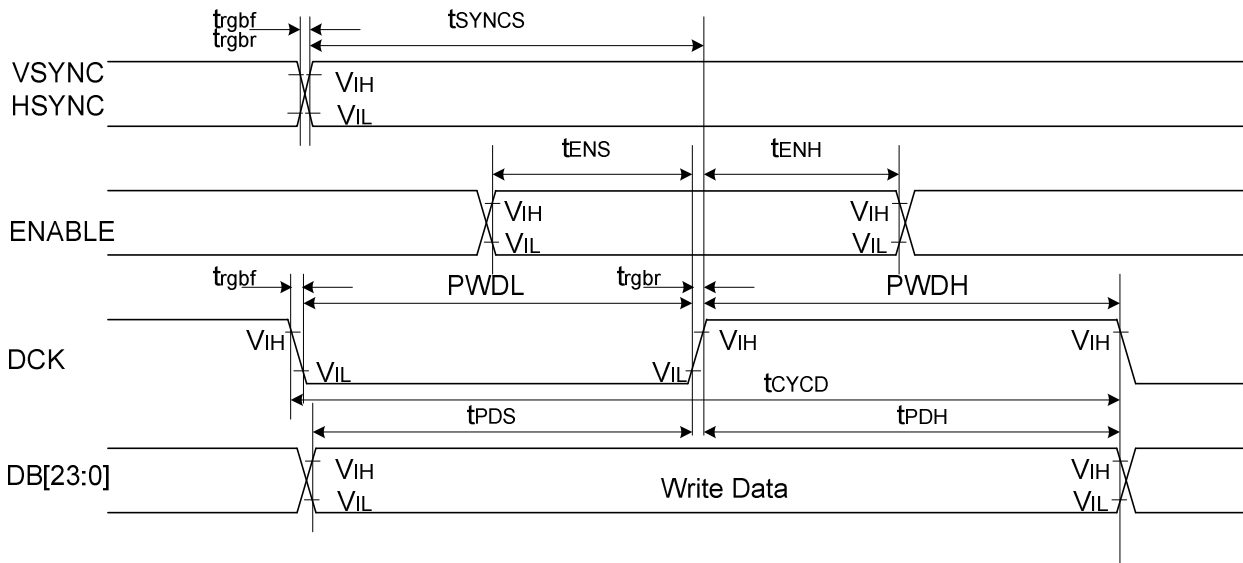


Signal	Symbol	Parameter	min	max	Unit	Description
CSX	tcss	Chip select time (Write)	15	-	ns	
	tcsh	Chip select hold time (Read)	15	-	ns	
	tCHW	CS "H" pulse width	40	-	ns	
SCL	twc	Serial clock cycle (Write)	30	-	ns	
	twrh	SCL "H" pulse width (Write)	10	-	ns	
	twrl	SCL "L" pulse width (Write)	10	-	ns	
	trc	Serial clock cycle (Read)	150	-	ns	
	trdh	SCL "H" pulse width (Read)	60	-	ns	
	trdl	SCL "L" pulse width (Read)	60	-	ns	
DCX	tas	DCX setup time	10	-	ns	
	tah	DCX hold time (Write/Read)	10	-	ns	
SDA (Input)	tds	Data setup time (Write)	10	-	ns	
	tdh	Data hold time (Write)	10	-	ns	
SDA (Output)	tacc	Access time (Read)	10	50	ns	CL = 30pF (maximum) CL = 8pF (minimum)
	toh	Output disable time (Read)	15	50	ns	

Notes:

1. $T_a = -30$ to 70°C , $V_{DDI} = 1.65\text{V}$ to 3.3V , $V_{DDA} = 2.6\text{V}$ to 4.8V , $V_{SSAM} = \text{GND} = 0\text{V}$, $T = 10\pm 0.5\text{ns}$.
2. Does not include signal rising and falling times.

19.3.8. Parallel 24/18/16-bit RGB Interface Timing Characteristics



Signal	Symbol	Parameter	min	max	Unit	Description
VSYNC/ HSYNC	tSYNCS	VSYNC/HSYNC setup time	5	-	ns	24/18/16-bit bus RGB interface mode
	tSYNCH	VSYNC/HSYNC hold time	5	-	ns	
ENABLE	tENS	ENABLE setup time	5	-	ns	
	tENH	ENABLE hold time	5	-	ns	
DB [23:0]	tPOS	Data setup time	5	-	ns	
	tPDH	Data hold time	5	-	ns	
DCK	PWDH	DCK high-level period	13	-	ns	
	PWDL	DCK low-level period	13	-	ns	
	tCYCD	DCK cycle time	28	-	ns	
	trgbbr, trgbfr	DCK, HSYNC, VSYNC rise/fall time	-	15	ns	

Note: Ta = -30 to 70°C, VDDI = 1.65V to 3.3V, VDDA = 2.6V to 4.8V, VSSAM = GND = 0V

19.3.9. DSI Timing Characteristics

19.3.10. High Speed Mode – Clock Channel Timing

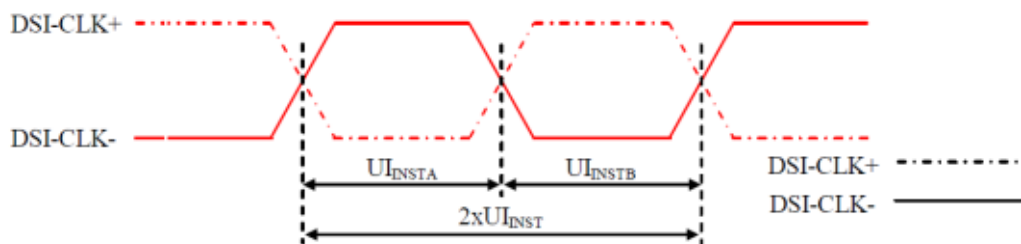


Figure 191: DSI Clock Channel Timing

Table 51: DSI Clock Channel Timing

Signal	Symbol	Parameter	Min	Max	Unit
DSI-CLK+/-	$2xUI_{INST}$	Double UI instantaneous	4	25	ns
DSI-CLK+/-	UI_{INSTA}, UI_{INSTB}	UI instantaneous Half	2	12.5	ns

Note: $UI = UI_{INSTA} = UI_{INSTB}$

19.3.11. High Speed Mode – Data Clock Channel Timing

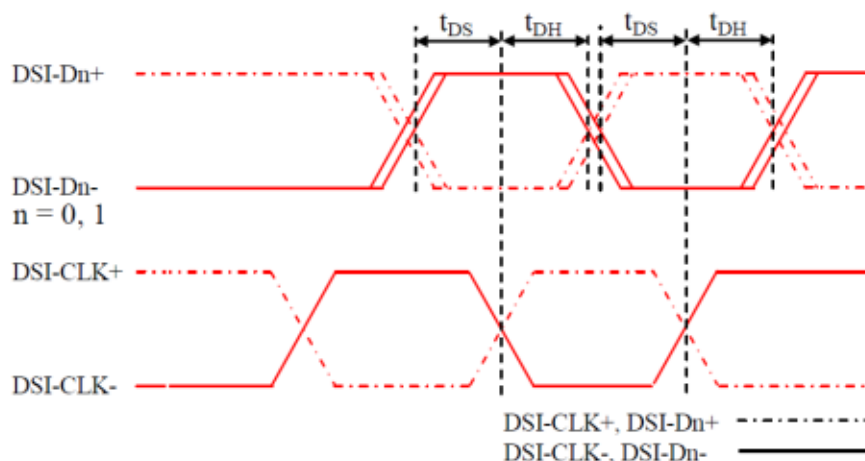


Figure 192: DSI Data to Clock Channel Timings

Table 52: DSI Data to Clock Channel Timings

Signal	Symbol	Parameter	Min	Max
DSI-Dn+/- , n=0 or 1	t_{DS}	Data to Clock Setup time	$0.15xUI$	-
	t_{DH}	Clock to Data Hold Time	$0.15xUI$	-

19.3.12. High Speed Mode – Rising and Falling Timings

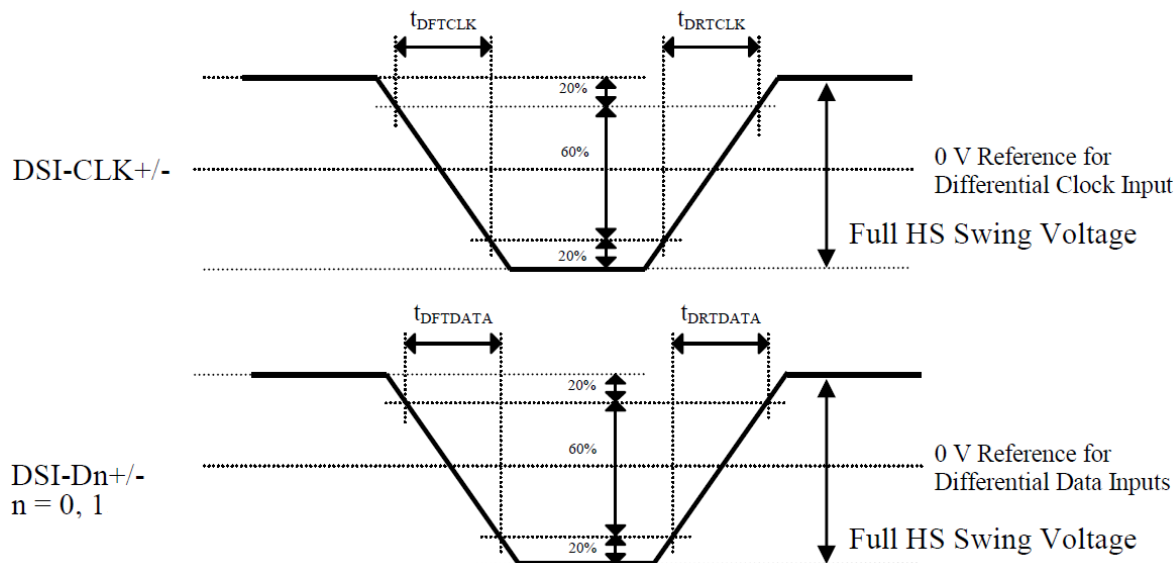


Figure 193: Rising and Falling Timings on Clock and Data Channels

Table 53: Rising and Falling Timings on Clock and Data Channels

Parameter	Symbol	Condition	Specification			Unit
			Min	Typ	Max	
Differential Rising Time for Clock	t_{DRTCLK}	DSI-CLK+/-	-	-	150 (Note 1)	ps
Differential Rising Time for Data	$t_{DRTDATA}$	DSI-Dn+/- n=0 and 1	-	-	150 (Note 1)	ps
Differential Falling Time for Clock	t_{DFTCLK}	DSI-CLK+/-	-	-	150 (Note 1)	ps
Differential Falling Time for Data	$t_{DFTDATA}$	DSI-Dn+/- n=0 and 1	-	-	150 (Note 1)	ps

Note: The display module has to meet timing requirements, what are defined for the transmitter (MPU) on MIPI D-Phy standard.

19.3.13. Low Speed Mode – Bus Turn Around

Lower Power Mode and its State Periods on the Bus Turnaround (BTA) from the MPU to the Display Module (ILI9806G) sequence are illustrated below for reference purposes.

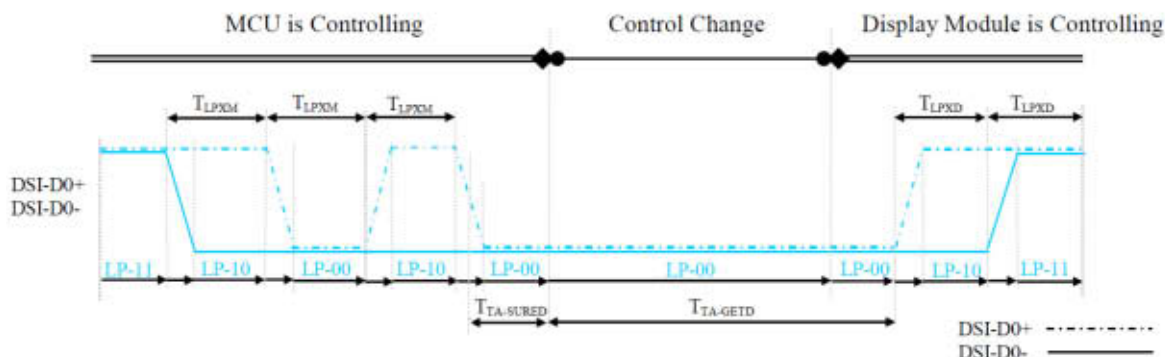


Figure 194: BTA from the MPU to the Display Module

Lower Power Mode and its State Periods on the Bus Turnaround (BTA) from the Display Module (ILI9806G) to the MPU sequence are illustrated below for reference purposes.

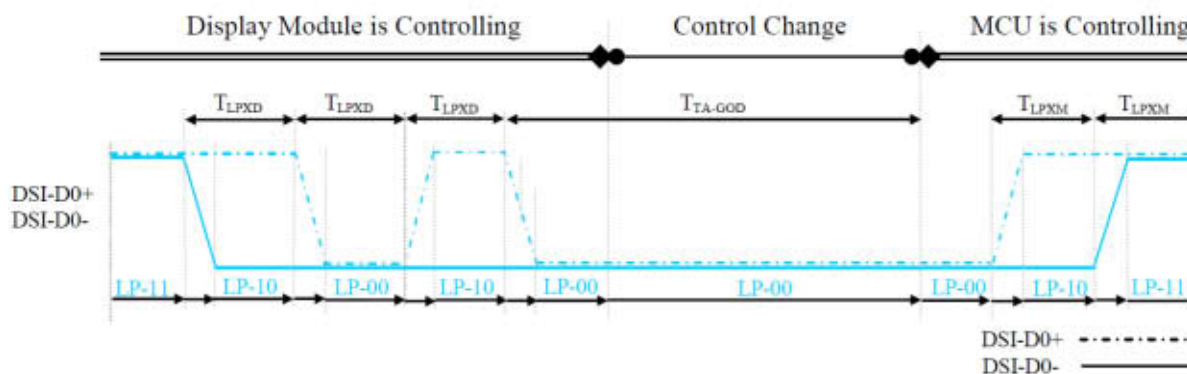


Figure 195: BTA from the Display Module to the MPU

Table 54: Low Power State Period Timings – A

Signal	Symbol	Description	Min	Max	Unit
DSI-D0+/-	T_{LPXM}	Length of LP-00, LP-01, LP-10 or LP-11 periods MPU → Display Module (ILI9806G)	50	75	ns
DSI-D0+/-	T_{LPXD}	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module (ILI9806G) → MPU	50	75	ns
DSI-D0+/-	$T_{TA-SURED}$	Time-out before the Display Module (ILI9806G) starts driving	T_{LPXD}	$2 \times T_{LPXD}$	ns

Table 55: Low Power State Period Timings – B

Signal	Symbol	Description	Time	Unit
DSI-D0+/-	$T_{TA-GETD}$	Time to drive LP-00 by Display Module (ILI9806G)	$5 \times T_{LPXD}$	ns
DSI-D0+/-	T_{TA-GOD}	Time to drive LP-00 after turnaround request - MPU	$4 \times T_{LPXD}$	ns

19.3.14. Data Lanes from Low Power Mode to High Speed Mode

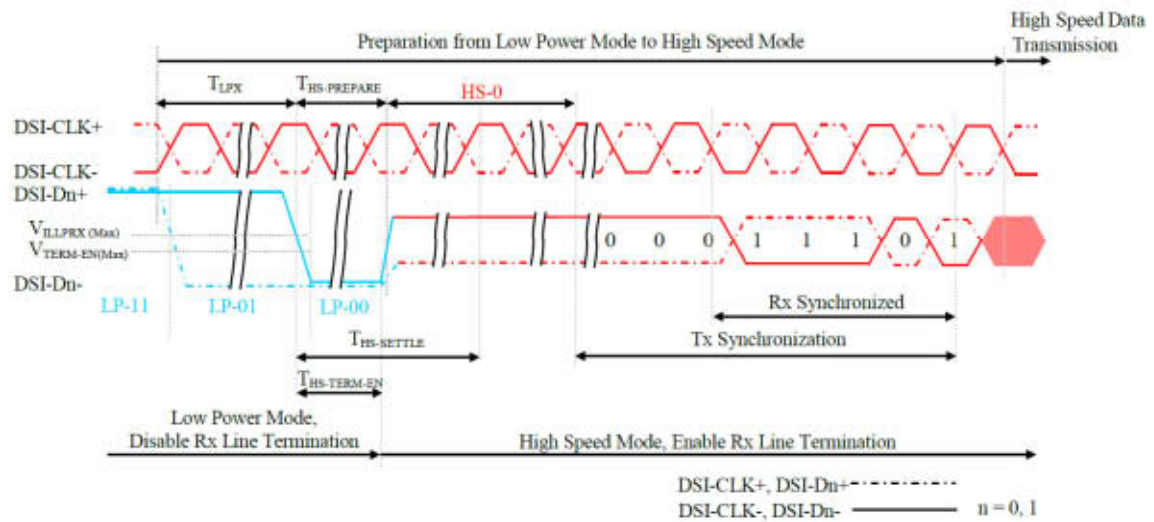


Figure 196: Data Lanes - Low Power Mode to High Speed Mode Timings

Table 56: Data Lanes - Low Power Mode to High Speed Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DSI-Dn+/-, n=0 or 1	T _{LPX}	Length of any Low Power State Period	50	-	ns
DSI-Dn+/-, n=0 or 1	T _{HS-PREPARE}	Time to drive LP-00 to prepare for HS Transmission	40+4xUI	85+6xUI	ns
DSI-Dn+/-, n=0 or 1	T _{HS-TERM-EN}	Time to enable Data Lane Receiver line termination measured from when Dn crosses VILMAX	-	35+4xUI	ns

19.3.15. Data Lanes from High Speed Mode to Low Power Mode

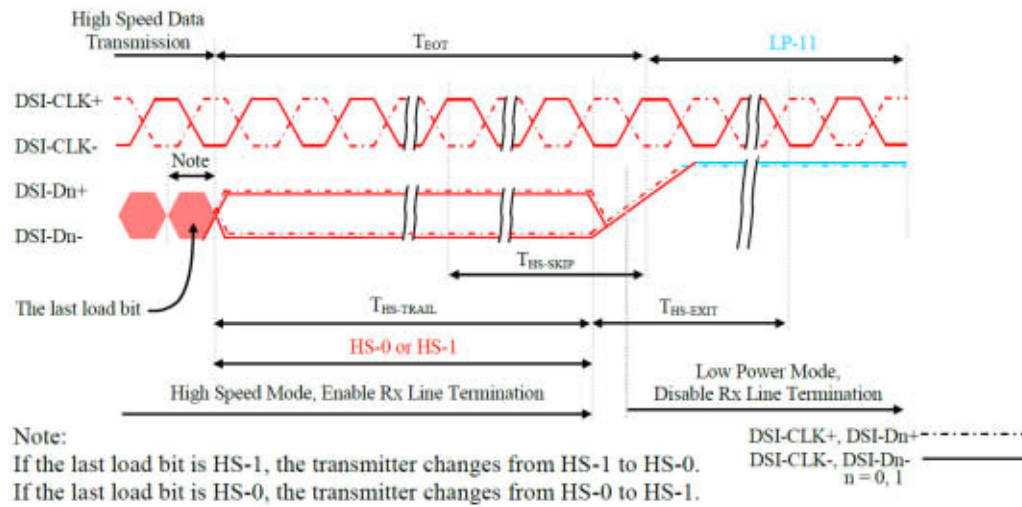


Figure 197: Data Lanes - High Speed Mode to Low Power Mode Timings

Table 57: Data Lanes - High Speed Mode to Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DSI-Dn+/-, n=0 or 1	$T_{HS-SKIP}$	Time-Out at Display Module (ILI9806G) to ignore transition period of EoT	40	$55+4 \times UI$	ns
DSI-Dn+/-, n=0 or 1	$T_{HS-EXIT}$	Time to driver LP-11 after HS burst	100	-	ns

19.3.16. DSI Clock Burst – High Speed Mode to/from Low Power Mode

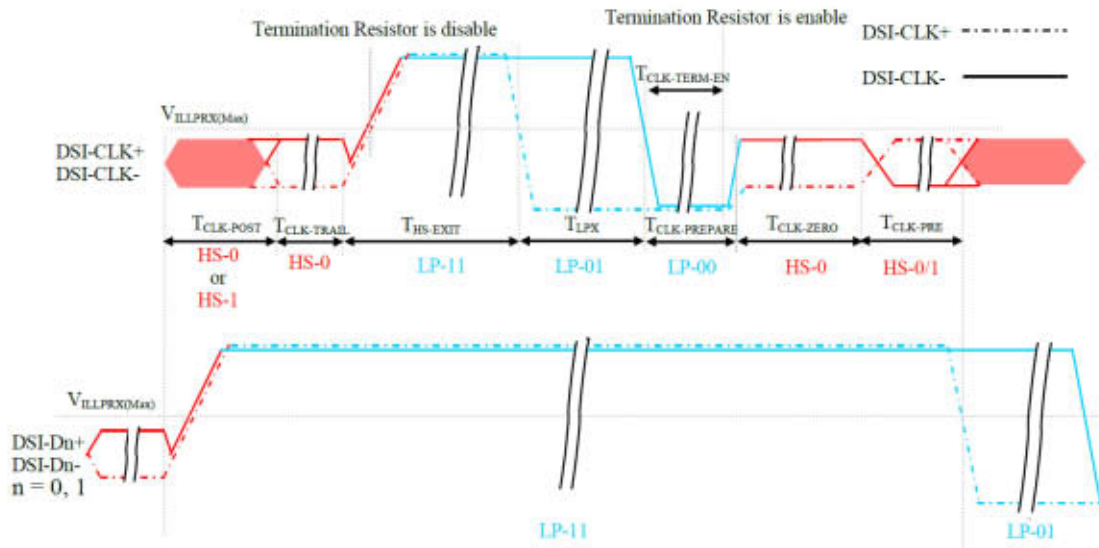


Figure 198: Clock Lanes - High Speed Mode to/from Low Power Mode Timings

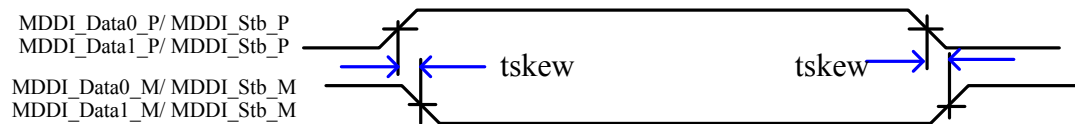
Table 58: Clock Lanes - High Speed Mode to/from Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DSI-CLK+/-	$T_{CLK-POST}$	Time that the MPU shall continue sending HS clock after the last associated Data Lanes has transitioned to LP mode	60+52xUI	-	ns
DSI-CLK+/-	$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	ns
DSI-CLK+/-	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100	-	ns
DSI-CLK+/-	$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	38	95	ns
DSI-CLK+/-	$T_{CLK-TERM-EN}$	Time-out at Clock Lane to enable HS termination	-	38	ns
DSI-CLK+/-	$T_{CLK-PREPARE}$	Minimum lead HS-0 drive period before starting Clock	300	-	ns
DSI-CLK+/-	$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8xUI	-	ns

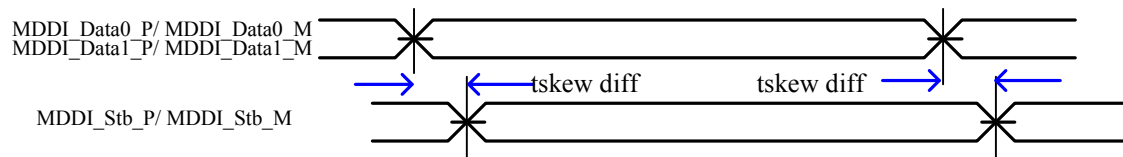
19.3.17. MDDI Timing Characteristics

Item	Symbol	Rating			Unit
		Min	Typ	Max	
Data transfer rate	1/t Bit	-	-	400	Mbps
Differential Transfer Input Skew	$ \pm \text{tskew} $	-	-	50	ps
Data_ Strobe Input Skew	$ \pm \text{tskew diff} $	-	-	$0.45 \cdot \text{tBIT}$	

Skew between positive and negative



Skew between Data and Strobe



20. Application Circuit

20.1. Reference Circuit

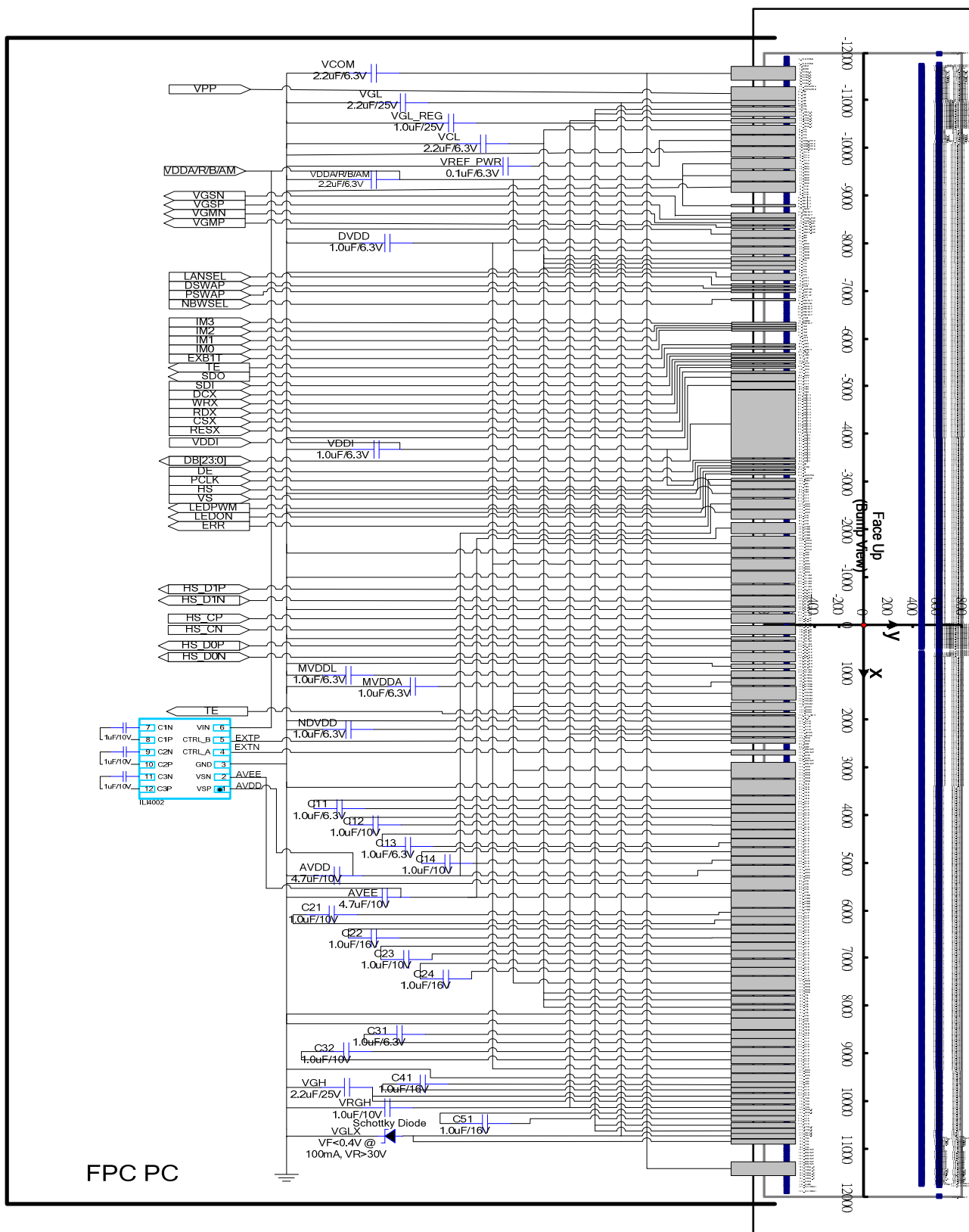


Figure 199: Reference Circuit

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20.2. External Component

Table 59 shows specifications of external elements connected to the power supply circuit of the ILI9806G.

Table 59: External Component Table

Pad Name	Connection	Typical Value
VDDI	Stable Capacitor to GND	1.0 μ F (Max 6.3V)
VDDA, VDDR, Vddb, VDDAM	Stable Capacitor to GND	2.2 μ F (Max 6.3V)
DVDD	Stable Capacitor to GND	1.0 μ F (Max 6.3V)
NDVDD	Stable Capacitor to GND	1.0 μ F (Max 6.3V)
MVDDA	Stable Capacitor to GND	1.0 μ F (Max 6.3V)
MVDDL	Stable Capacitor to GND	1.0 μ F (Max 6.3V)
C11P, C11N	Flying Capacitor	1.0 μ F (Max 6.3V)
C12P, C12N	Flying Capacitor	1.0 μ F (Max 10V)
C13P, C13N	Flying Capacitor	1.0 μ F (Max 6.3V)
C14P, C14N	Flying Capacitor	1.0 μ F (Max 10V)
C21P, C21N	Flying Capacitor	1.0 μ F (Max 10V)
C22P, C22N	Flying Capacitor	1.0 μ F (Max 16V)
C23P, C23N	Flying Capacitor	1.0 μ F (Max 10V)
C24P, C24N	Flying Capacitor	1.0 μ F (Max 16V)
C31P, C31N	Flying Capacitor	1.0 μ F (Max 6.3V)
C32P, C32N	Flying Capacitor	1.0 μ F (Max 10V)
C41P, C41N	Flying Capacitor	1.0 μ F (Max 16V)
C51P, C51N	Flying Capacitor	1.0 μ F (Max 16V)
AVDD	Stable Capacitor to GND	4.7 μ F (Max 10V)
AVEE	Stable Capacitor to GND	4.7 μ F (Max 10V)
VCL	Stable Capacitor to GND	2.2 μ F (Max 6.3V)
VGH	Stable Capacitor to GND	2.2 μ F (Max 25V)
VGL	Stable Capacitor to GND	2.2 μ F (Max 25V)
	Schottky Diode to GND	VF=0.52V / IF=1A , at TA=25°C Rated Current= 1A, VR=40V (optional)
LVGL	Stable Capacitor to GND	1.0 μ F (Max 25V)
VRGH	Stable Capacitor to GND	1.0 μ F (Max 10V)
VCOM	Stable Capacitor to GND	2.2 μ F (Max 6.3V)
VREF_PWR	Stable Capacitor to GND	0.1 μ F (Max 6.3V)

21. Revision History

Version No.	Date	Page	Description
V100	2014/04/17	—	New Creative